National Semiconductor

54F/74F552
Octal Registered Transceiver with Parity and Flags

General Description

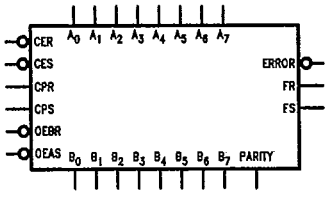
The 'F552 octal transceiver contains two 8-bit registers for temporary storage of data flowing in either direction. Each register has its own clock pulse and clock enable input as well as a flag flip-flop that is set automatically as the register is loaded. The flag output will be reset when the output enable returns to HIGH after reading the output port. Each register has a separate output enable control for its TRI-STATE® buffer. The separate Clocks, Flags, and Enables provide considerable flexibility as I/O ports for demand-response data transfer. When data is transferred from the A-port to the B-port, a parity bit is generated. On the other hand, when data is transferred from the B-port to the A-port, the parity of input data on B_0–B_7 is checked.

Features

- 8-Bit bidirectional I/O Port with handshake
- Register status flag flip-flops
- Separate clock enable and output enable
- Parity generation and parity check
- B-outputs sink 64 mA
- TRI-STATE outputs

Ordering Code: See Section 5

Logic Symbols



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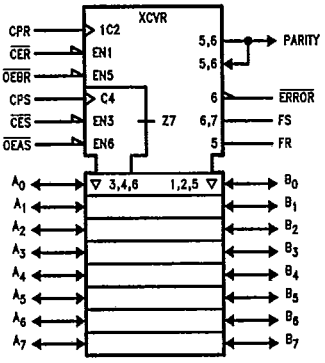
IEEE/IEC



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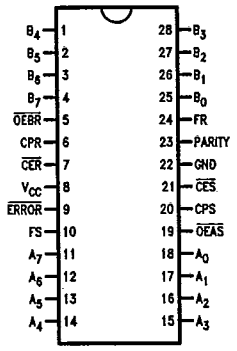
Connection Diagrams

Pin Assignment for DIP, SOIC and Flatpak



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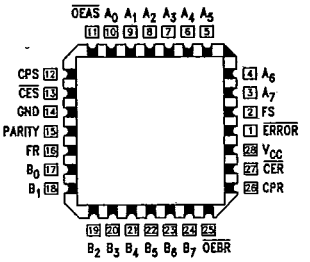
Pin Assignment for LCC and PCC



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Unit Loading/Fan Out: See Section 2 for U.L. definitions

Pin Names	Description	54F/74F	
		U.L. HIGH/LOW	Input I_{IH}/I_{IL} Output I_{OH}/I_{OL}
A_0–A_7	A-to-B Port Data Inputs or	3.5/1.083	70 μA/−0.65 mA
	B-to-A TRI-STATE	150/40 (33.3)	−3 mA/24 mA (20 mA)
B_0–B_7	B-to-A Transceiver Inputs or	3.5/1.083	70 μA/−0.65 mA
	A-to-B TRI-STATE Output	600/106.6 (80)	−12 mA/64 mA (48 mA)
FR	B Port Flag Output	50/33.3	−1 mA/20 mA
FS	A Port Flag Output	50/33.3	−1 mA/20 mA
PARITY	Parity Bit Transceiver Input or Output	3.5/1.083	70 μA/−0.65 mA
		600/106.6 (50)	−12 mA/64 mA (48 mA)
$\overline{ERROR}$	Parity Check Output (Active LOW)	50/33.3	−1 mA/20 mA
$\overline{CER}$	R Registers Clock Enable Input (Active LOW)	1.0/1.0	20 μA/−0.6 mA
$\overline{CES}$	S Registers Clock Enable Input (Active LOW)	1.0/1.0	20 μA/−0.6 mA
CPR	R Registers Clock Pulse Input (Active Rising Edge)	1.0/1.0	20 μA/−0.6 mA
CPS	S Registers Clock Pulse Input (Active Rising Edge)	1.0/1.0	20 μA/−0.6 mA
$\overline{OEBR}$	B Port and PARITY Output Enable (Active LOW) and Clear FR Input (Active Rising Edge)	1.0/2.0	20 μA/−1.2 mA
$\overline{OEAS}$	A Port Output Enable (Active LOW) and Clear FS Input (Active Rising Edge)	1.0/2.0	20 μA/−1.2 mA

Functional Description

Data applied to the A-inputs are entered and stored in the R register on the rising edge of the CPR Clock Pulse, provided that the Clock Enable ($\overline{CER}$) is LOW; simultaneously, the status flip-flop is set and the flag (FR) output goes HIGH. As the Clock Enable ($\overline{CER}$) returns to HIGH, the data will be held in the R register. These data entered from the A-inputs will appear at the B-port I/O pins after the Output Enable ($\overline{OEBR}$) has gone LOW. When $\overline{OEBR}$ is LOW, a parity bit appears at the PARITY pin, which will be set HIGH when there is an even number of 1s or all 0s at the Q outputs of the R register. After the data is assimilated, the receiving system clears the flag FR by changing the signal at the $\overline{OEBR}$ pin from LOW to HIGH.

Data flow from B-to-A proceeds in the same manner described for A-to-B flow. A LOW at the $\overline{CES}$ pin and a LOW-to-HIGH transition at CPS pin enters the B-input data and the parity-input data into the S registers and the parity register respectively and set the flag output FS to HIGH. A LOW signal at the $\overline{OEAS}$ pin enables the A-port I/O pins and a LOW-to-HIGH transition of the $\overline{OEAS}$ signal clears the FS flag. When $\overline{OEAS}$ is LOW, the parity check output $\overline{ERROR}$ will be HIGH if there is an odd number of 1s at the Q outputs of the S registers and the parity register. The flag FS can be cleared by a LOW-to-HIGH transition of the $\overline{OEAS}$ signal.

Register Function Table

(Applies to R or S Register)

Inputs			Internal Q	Function
D	CP	$\overline{CE}$		
X	X	H	NC	Hold Data
L	↗	L	L	Load Data
H	↗	L	H	
X	†	L	NC	Keep Old Data

H = HIGH Voltage Level
L = LOW Voltage Level
X = Immaterial
↗ = LOW-to-HIGH Transition
† = Not LOW-to-HIGH Transition
NC = No Change

Output Control

$\overline{OE}$	Internal Q	A or B Outputs	Function
H	X	Z	Disable Output
L	L	L	Enable Output
L	H	H	Enable Output

H = HIGH Voltage Level
L = LOW Voltage Level
X = Immaterial
Z = High Impedance

Flag Flip-Flop Function Table

(Applies to R or S Flag Flip-Flop)

Inputs			Flag Output	Function
$\overline{CE}$	CP	$\overline{OE}$		
H	X	†	NC	Hold Flag
L	↗	†	H	Set Flag
X	X	↗	L	Clear Flag

H = HIGH Voltage Level
L = LOW Voltage Level
X = Immaterial
↗ = LOW-to-HIGH Transition
† = Not LOW-to-HIGH Transition
NC = No Change

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Functional Description

Parity Generation Function

$\overline{OEBR}$	Number of HIGHs in the Q Outputs of the R Register	Parity Output
H	X	Z
L	0, 2, 4, 6, 8	H
L	1, 3, 5, 7	L

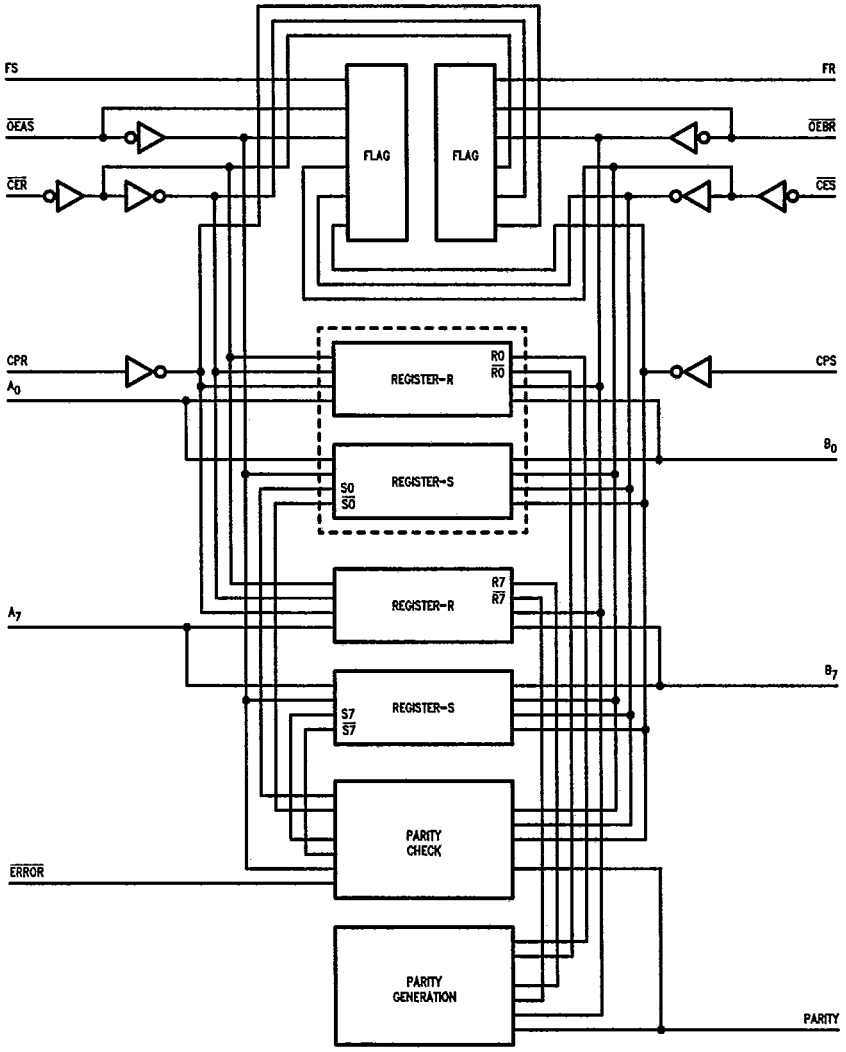
H = HIGH Voltage Level
L = LOW Voltage Level
X = Immaterial
Z = High Impedance

Parity Check Function

$\overline{OEAS}$	Number of HIGHs in the Q Outputs of the S Register	Parity Input	$\overline{ERROR}$ Output
H	X	X	H
L	0, 2, 4, 6, 8	L	L
L	1, 3, 5, 7	L	H
L	0, 2, 4, 6, 8	H	H
L	1, 3, 5, 7	H	L

H = HIGH Voltage Level
L = LOW Voltage Level
X = Immaterial

Block Diagram



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Absolute Maximum Ratings (Note 1)

If Military/Aerospace specified devices are required, contact the National Semiconductor Sales Office/ Distributors for availability and specifications.

Storage Temperature	−65°C to +150°C
Ambient Temperature under Bias	−55°C to +125°C
Junction Temperature under Bias	−55°C to +175°C
V_{CC} Pin Potential to Ground Pin	−0.5V to +7.0V
Input Voltage (Note 2)	−0.5V to +7.0V
Input Current (Note 2)	−30 mA to +5.0 mA
Voltage Applied to Output in HIGH State (with V_{CC} = 0V)	
Standard Output	−0.5V to V_{CC}
TRI-STATE Output	−0.5V to +5.5V
Current Applied to Output in LOW State (Max)	twice the rated I_{OL} (mA)

Note 1: Absolute maximum ratings are values beyond which the device may be damaged or have its useful life impaired. Functional operation under these conditions is not implied.

Note 2: Either voltage limit or current limit is sufficient to protect inputs.

Recommended Operating Conditions

Free Air Ambient Temperature	
Military	−55°C to +125°C
Commercial	0°C to +70°C
Supply Voltage	
Military	+4.5V to +5.5V
Commercial	+4.5V to +5.5V

DC Electrical Characteristics

Symbol	Parameter		54F/74F Min	54F/74F Typ	54F/74F Max	Units	V_{CC}	Conditions
V_{IH}	Input HIGH Voltage		2.0			V		Recognized as a HIGH Signal
V_{IL}	Input LOW Voltage				0.8	V		Recognized as a LOW Signal
V_{CD}	Input Clamp Diode Voltage				−1.2	V	Min	I_{IN} = −18 mA ($\overline{CER}$, $\overline{CES}$, CPR, CPS, $\overline{OEBR}$, $\overline{OEAS}$)
V_{OH}	Output HIGH Voltage	54F 10% V_{CC}	2.5			V	Min	I_{OH} = −1 mA (FR, FS, $\overline{ERROR}$, A_n)
		54F 10% V_{CC}	2.4					I_{OH} = −3 mA (A_n, B_n, PARITY)
		54F 10% V_{CC}	2.0					I_{OH} = −12 mA (B_n, PARITY)
		74F 10% V_{CC}	2.5					I_{OH} = −1 mA (FR, FS, $\overline{ERROR}$, A_n)
		74F 10% V_{CC}	2.4					I_{OH} = −3 mA (A_n, B_n PARITY)
		74F 10% V_{CC}	2.0					I_{OH} = −12 mA (B_n, PARITY)
		74F 5% V_{CC}	2.7					I_{OH} = −1 mA (FR, FS, $\overline{ERROR}$, A_n)
		74F 5% V_{CC}	2.7					I_{OH} = −3 mA (A_n, B_n, PARITY)
		74F 5% V_{CC}	2.0					I_{OH} = −15 mA (B_n, PARITY)
V_{OL}	Output LOW Voltage	54F 10% V_{CC}			0.5	V	Min	I_{OL} = 20 mA (FR, FS, $\overline{ERROR}$, A_n)
		54F 10% V_{CC}			0.55			I_{OL} = 48 mA (B_n, PARITY)
		74F 10% V_{CC}			0.5			I_{OL} = 20 mA (FR, FS, $\overline{ERROR}$)
		74F 10% V_{CC}			0.5			I_{OL} = 24 mA (A_n)
		74F 10% V_{CC}			0.55			I_{OL} = 64 mA (B_n, PARITY)
I_{IH}	Input HIGH Current				20	μA	Max	V_{IN} = 2.7V ($\overline{CER}$, $\overline{CES}$, CPR, CPS, $\overline{OEBR}$, $\overline{OEAS}$)
I_{BVI}	Input HIGH Current Breakdown Test				100	μA	Max	V_{IN} = 7.0V ($\overline{CER}$, $\overline{CES}$, CPR, CPS, $\overline{OEBR}$, $\overline{OEAS}$)
I_{BVIT}	Input HIGH Current Breakdown Test (I/O)				1.0	mA	Max	V_{IN} = 5.5V (A_n, B_n, PARITY)
I_{IL}	Input LOW Current				−0.6	mA	Max	V_{IN} = 0.5V ($\overline{CER}$, $\overline{CES}$, CPR, CPS)
					−1.2			V_{IN} = 0.5V ($\overline{OEBR}$, $\overline{OEAS}$)
I_{IH} + I_{OZH}	Output Leakage Current				70	μA	Max	V_{OUT} = 2.7V (A_n, B_n, PARITY)
I_{IL} + I_{OZL}	Output Leakage Current				−650	μA	Max	V_{OUT} = 0.5V (A_n, B_n, PARITY)
I_{OS}	Output Short-Circuit Current		−60		−150	mA	Max	V_{OUT} = 0V (FR, FS, $\overline{ERROR}$, A_n)
			−100		−225			V_{OUT} = 0V (B_n, PARITY)
I_{CEX}	Output HIGH Leakage Current				250	μA	Max	V_{OUT} = V_{CC} (FR, FS, $\overline{ERROR}$, A_n, B_n, PARITY)
I_{ZZ}	Buss Drainage Test				500	μA	0.0V	V_{OUT} = V_{CC} (A_n, B_n, PARITY)
I_{CCH}	Power Supply Current			100	150	mA	Max	V_O = HIGH
I_{CCL}	Power Supply Current			100	150	mA	Max	V_O = LOW
I_{CCZ}	Power Supply Current			110	165	mA	Max	V_O = HIGH Z

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AC Electrical Characteristics: See Section 2 for Waveforms and Load Configurations

Symbol	Parameter	74F $T_A = +25°C$, $V_{CC} = +5.0V$, $C_L = 50$ pF			54F T_A, V_{CC} = Mil, $C_L = 50$ pF		74F T_A, V_{CC} = Com, $C_L = 50$ pF		Units	Fig No
		Min	Typ	Max	Min	Max	Min	Max		
t_{PLH} t_{PHL}	Propagation Delay CPS or CPR to A_n or B_n	3.5 4.0	6.0 7.0	8.0 9.5			3.0 3.5	9.0 10.5	ns	2–3
t_{PLH}	Propagation Delay CPS or CPR to FS or FR	3.0	5.5	7.5			2.5	8.5	ns	2–3
t_{PHL}	Propagation Delay $\overline{OEAS}$ to FS	3.5	6.0	8.0			3.0	9.0	ns	2–3
t_{PLH} t_{PHL}	Propagation Delay CPS to Parity	8.0 8.5	14.0 14.5	18.0 18.5			7.0 7.5	20.0 20.5	ns	2–3
t_{PLH} t_{PHL}	Propagation Delay CPR to $\overline{ERROR}$	8.0 7.5	13.5 13.0	17.5 16.5			7.0 6.5	19.5 18.5	ns	2–3
t_{PLH} t_{PHL}	Propagation Delay $\overline{OEAS}$ to $\overline{ERROR}$	3.5 3.0	6.0 5.0	8.0 7.0			3.0 2.5	9.0 8.0	ns	2–3
t_{PZH} t_{PZL}	Enable Time $\overline{OEAS}$ or $\overline{OEBR}$ to B_n or A_n	3.0 3.5	5.5 7.0	7.5 9.5			2.5 3.0	8.5 10.5	ns	2–5
t_{PHZ} t_{PLZ}	Disable Time $\overline{OEAS}$ or $\overline{OEBR}$ to B_n or A_n	3.0 3.0	6.5 5.5	8.5 7.5			2.5 2.5	9.5 8.5		
t_{PZH} t_{PZL}	Enable Time $\overline{OEBR}$ to Parity	3.0 3.5	4.5 6.0	7.5 9.5			2.5 3.0	8.5 10.5	ns	2–5
t_{PHZ} t_{PLZ}	Disable Time $\overline{OEBR}$ to Parity	3.0 3.0	5.5 6.5	8.5 7.5			2.5 2.5	9.5 8.5		

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AC Operating Requirements: See Section 2 for Waveforms

Symbol	Parameter	74F $T_A = +25°C$ $V_{CC} = +5.0V$		54F T_A, V_{CC} = Mil		74F T_A, V_{CC} = Com		Units	Fig No
		Min	Max	Min	Max	Min	Max		
$t_s(H)$ $t_s(L)$	Setup Time, HIGH or LOW A_n or B_n or Parity to CPS or CPR	7.5 4.5				8.5 5.0		ns	2–6
$t_h(H)$ $t_h(L)$	Hold Time, HIGH or LOW A_n or B_n or Parity to CPS or CPR	0 0				0 0			
$t_s(H)$ $t_s(L)$	Setup, Time HIGH or LOW $\overline{CES}$ or $\overline{CER}$ to CPS or CPR	6.0 10.0				7.0 11.5		ns	2–6
$t_h(H)$ $t_h(L)$	Hold Time, HIGH or LOW $\overline{CES}$ or $\overline{CER}$ to CPS or CPR	0 0				0 0			
$t_w(H)$ $t_w(L)$	Pulse Width, HIGH or LOW CPS or CPR	4.0 6.0				4.5 7.0		ns	2–4

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