Document No.	853-0055
ECN No.	99494
Date of issue	April 27, 1990
Status	Product Specification
FAST Products	

FAST 74F85 Comparator

4-Bit Magnitude Comparator

TYPE	TYPICAL PROPAGATION DELAY	TYPICAL SUPPLY CURRENT (TOTAL)
74F85	7.0ns	40mA

FEATURES

- **High-impedance NPN base inputs for reduced loading (20μA in High and Low states)**
- **Magnitude comparison of any binary words**
- **Serial of parallel expansion without extra gating**

ORDERING INFORMATION

PACKAGES	COMMERCIAL RANGE V_{CC} = 5V±10%; T_A = 0°C to +70°C
16-Pin Plastic DIP	N74F85N
16-Pin Plastic SOL	N74F85D

DESCRIPTION

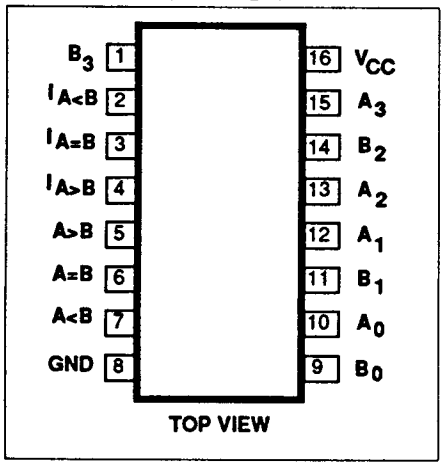
The 74F85 is a 4-bit magnitude comparator that can be expanded to almost any length. It compares two 4-bit binary, BCD, or other monotonic codes and presents the three possible magnitude results at the outputs. The 4-bit inputs are weighted (A_0-A_3) and (B_0-B_3) where A_3 and B_3 are the most significant bits. The operation of the 74F85 is described in the Function Table, showing all possible logic conditions. The upper part of the table describes the normal operation under all conditions that will occur in a single device or in a series expansion scheme. In the upper part of the table the three outputs are mutually exclusive. In the lower part of the table, the outputs reflect the feed-forward conditions that exists in the parallel expansion scheme. The expansion inputs $I_{A>B}$, $I_{A=B}$ and $I_{A<B}$ are the least significant bit positions. When used for series expansion, the A>B, A=B and A<B outputs of the least significant word are connected to thecorresponding $I_{A>B}$, $I_{A=B}$ and $I_{A<B}$ inputs of the next higher stage. Stages can be added in this manner to any length, but a propagation delay penalty of about 15ns is added with each additional stage. For proper operation the expansion inputs of the least significant word should be tied as follows: $I_{A>B}$=Low, $I_{A=B}$=High and $I_{A<B}$=Low.

INPUT AND OUTPUT LOADING AND FAN-OUT TABLE

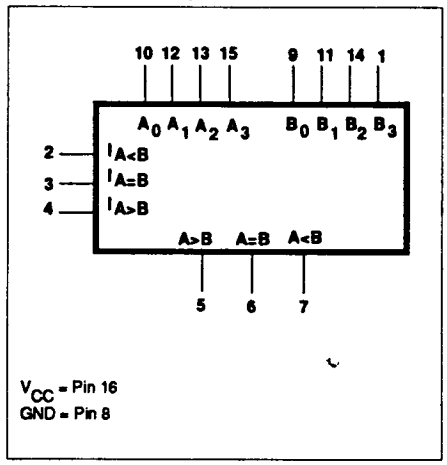
PINS	DESCRIPTION	74F(U.L.) HIGH/LOW	LOAD VALUE HIGH/LOW
A_0- A_3	Comparing inputs	1.0/0.033	20μA/20μA
B_0- B_3	Comparing inputs	1.0/0.033	20μA/20μA
$I_{A<B}$, $I_{A=B}$, $I_{A>B}$	Expansion inputs (active High)	1.0/0.033	20μA/20μA
A<B, A=B, A>B	Data outputs (active High)	50/33	1.0mA/20mA

NOTE:
One (1.0) FAST Unit Load is defined as: 20μA in the High state and 0.6mA in the Low state.

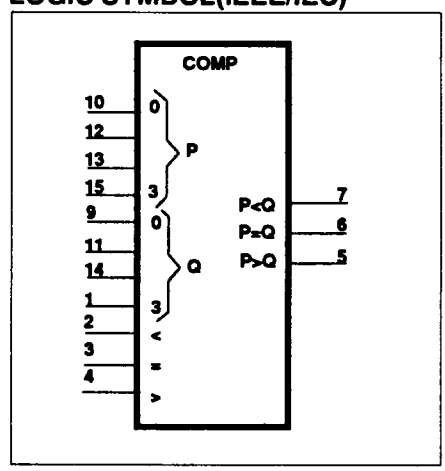
PIN CONFIGURATION



LOGIC SYMBOL

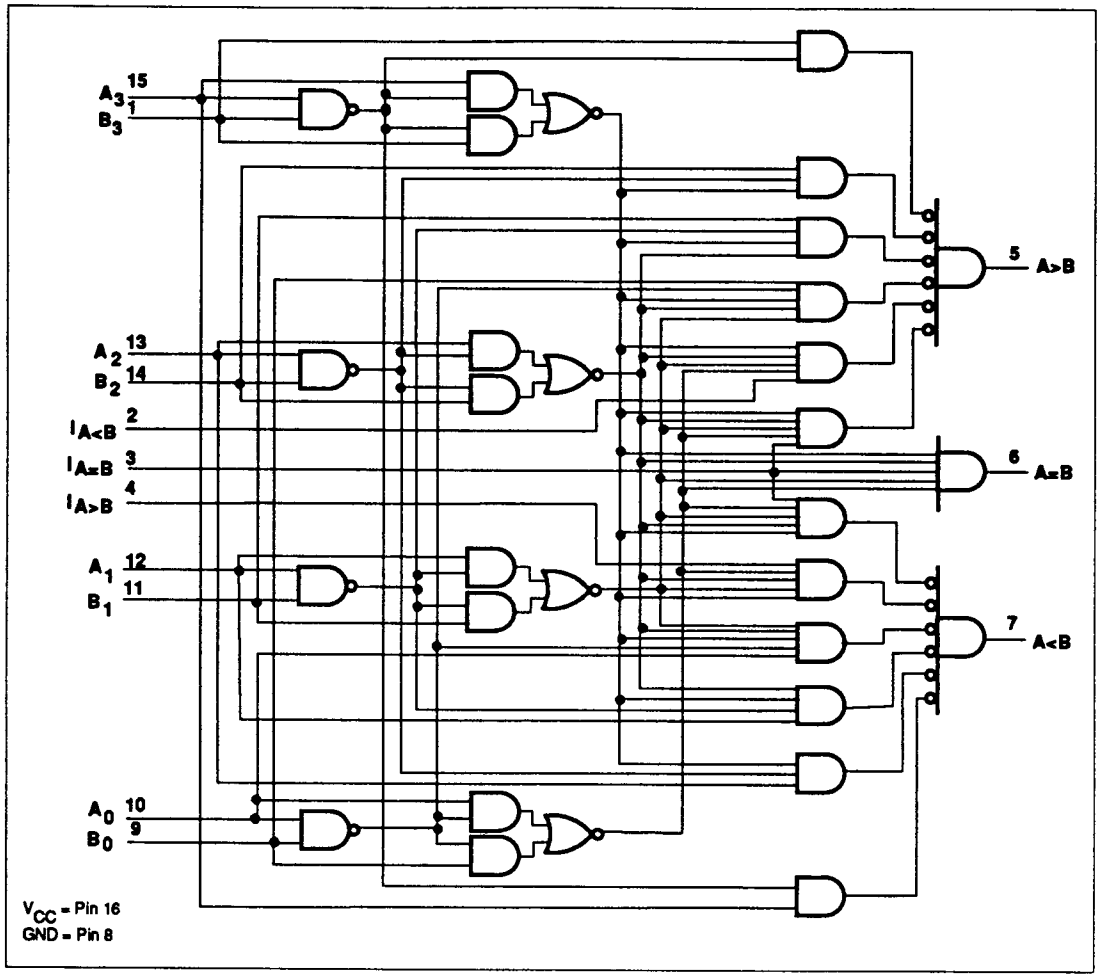


LOGIC SYMBOL(IEEE/IEC)



Comparator | FAST 74F85

LOGIC DIAGRAM



FUNCTION TABLE

COMPARING INPUTS				EXPANSION INPUTS			OUTPUTS		
A_3,B_3	A_2,B_2	A_1,B_1	A_0,B_0	$I_{A>B}$	$I_{A<B}$	$I_{A=B}$	A>B	A<B	A=B
$A_3>B_3$	X	X	X	X	X	X	H	L	L
$A_3<B_3$	X	X	X	X	X	X	L	H	L
$A_3=B_3$	$A_2>B_2$	X	X	X	X	X	H	L	L
$A_3=B_3$	$A_2<B_2$	X	X	X	X	X	L	H	L
$A_3=B_3$	$A_2=B_2$	$A_1>B_1$	X	X	X	X	H	L	L
$A_3=B_3$	$A_2=B_2$	$A_1<B_1$	X	X	X	X	L	H	L
$A_3=B_3$	$A_2=B_2$	$A_1=B_1$	$A_0>B_0$	X	X	X	H	L	L
$A_3=B_3$	$A_2=B_2$	$A_1=B_1$	$A_0<B_0$	X	X	X	L	H	L
$A_3=B_3$	$A_2=B_2$	$A_1=B_1$	$A_0=B_0$	H	L	L	H	L	L
$A_3=B_3$	$A_2=B_2$	$A_1=B_1$	$A_0=B_0$	L	H	L	L	H	L
$A_3=B_3$	$A_2=B_2$	$A_1=B_1$	$A_0=B_0$	L	L	H	L	L	H
$A_3=B_3$	$A_2=B_2$	$A_1=B_1$	$A_0=B_0$	X	X	H	L	L	H
$A_3=B_3$	$A_2=B_2$	$A_1=B_1$	$A_0=B_0$	H	H	L	L	L	L
$A_3=B_3$	$A_2=B_2$	$A_1=B_1$	$A_0=B_0$	L	L	L	H	H	L

H = High voltage level
L = Low voltage level
X = Don't care

APPLICATION

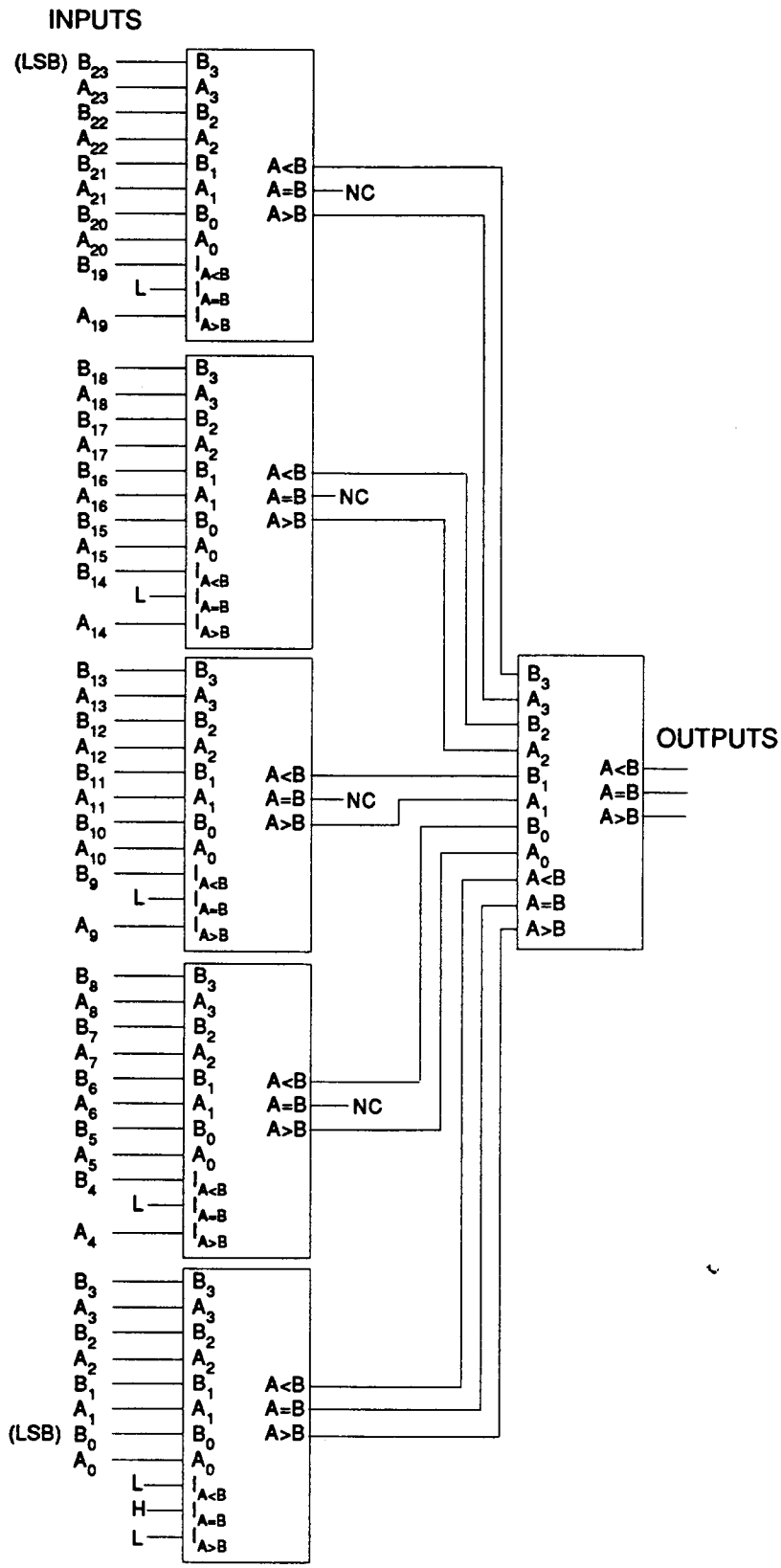


Figure 1. Comparison Of Two 24-Bit Words

The parallel expansion scheme shown in Figure 1 demonstrates the most efficient general use of these comparators. The expansion inputs can be used as a fifth input bit position except on the least significant device which must be connected as in the serial scheme.The expansion inputs used by labeling $I_{A>B}$ as an "A" input, $I_{A<B}$ as an "B" input and setting $I_{A=B}$=Low. The 'F85 can be used as 5-bit comparator only when the outputs are used to drive the (A_0-A_3) and (B_0-B_3) inputs of another 'F85 device. The parallel technique can be expanded to any number of bits as shown in Table 1.

Table1

WORD LENGTH	NUMBER OF PACKAGES	TYPICAL SPEEDS 74F
1-4 Bits	1	12ns
5-24 Bits	2-6	22ns
25-120 Bits	8-31	34ns

ABSOLUTE MAXIMUM RATINGS

(Operation beyond the limits set forth in this table may impair the useful life of the device. Unless otherwise noted these limits are over the operating free-air temperature range.)

SYMBOL	PARAMETER	RATING	UNIT
V_{CC}	Supply voltage	-0.5 to +7.0	V
V_{IN}	Input voltage	-0.5 to +7.0	V
I_{IN}	Input current	-30 to +5	mA
V_{OUT}	Voltage applied to output in High output state	-0.5 to +V_{CC}	V
I_{OUT}	Current applied to output in Low output state	40	mA
T_A	Operating free-air temperature range	0 to +70	°C
T_{STG}	Storage temperature	-65 to +150	°C

RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	LIMITS			UNIT
		Min	Nom	Max	
V_{CC}	Supply voltage	4.5	5.0	5.5	V
V_{IH}	High-level input voltage	2.0			V
V_{IL}	Low-level input voltage			0.8	V
I_{IK}	Input clamp current			-18	mA
I_{OH}	High-level output current			-1	mA
I_{OL}	Low-level output current			20	mA
T_A	Operating free-air temperature range	0		70	°C

DC ELECTRICAL CHARACTERISTICS

(Over recommended operating free-air temperature range unless otherwise noted.)

SYMBOL	PARAMETER		TEST CONDITIONS[1]		LIMITS			UNIT
					Min	Typ[2]	Max	
V_{OH}	High-level output voltage		V_{CC} = MIN, V_{IL} = MAX	±10%V_{CC}	2.5			V
			V_{IH} = MIN, I_{OH} = MAX	±5%V_{CC}	2.7	3.4		V
V_{OL}	Low-level output voltage		V_{CC} = MIN, V_{IL} = MAX	±10%V_{CC}		0.30	0.50	V
			V_{IH} = MIN, I_{OL} = MAX	±5%V_{CC}		0.30	0.50	V
V_{IK}	Input clamp voltage		V_{CC} = MIN, I_I = I_{IK}			-0.73	-1.2	V
I_I	Input current at maximum input voltage		V_{CC} =0.0V, V_I = 7.0V				100	µA
I_{IH}	High-level input current		V_{CC} = MAX, V_I = 2.7V				20	µA
I_{ILL}	Low-level input current		V_{CC} = MAX, V_I = 0.5V				-20	µA
I_{OS}	Short-circuit output current[3]		V_{CC} = MAX		-60		-150	mA
I_{CC}	Supply current (total)	I_{CCH}	V_{CC} = MAX	V_{IN}=GND		36	50	mA
		I_{CCL}		A_n=B_n=$I_{A=B}$=GND, $I_{A>B}$=$I_{A<B}$=4.5V		40	54	mA

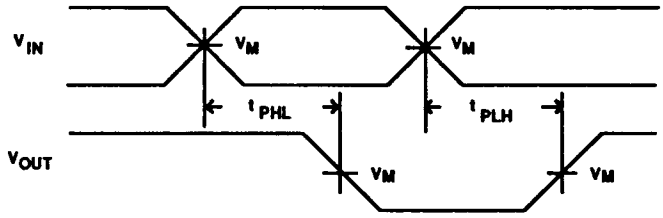
NOTES:

1. For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable type.
2. All typical values are at V_{CC} = 5V, T_A = 25°C.
3. Not more than one output should be shorted at a time. For testing I_{OS}, the use of high-speed test apparatus and/or sample-and-hold techniques are preferable in order to minimize internal heating and more accurately reflect operational values. Otherwise, prolonged shorting of a High output may raise the chip temperature well above normal and thereby cause invalid readings in other parameter tests. In any sequence of parameter tests, I_{OS} tests should be performed last.

AC ELECTRICAL CHARACTERISTICS

SYMBOL	PARAMETER	TEST CONDITION	LIMITS					UNIT
			T_A = +25°C, V_{CC} = 5V, C_L = 50pF, R_L = 500Ω			T_A = 0°C to +70°C, V_{CC} = 5V ±10%, C_L = 50pF, R_L = 500Ω		
			Min	Typ	Max	Min	Max	
t_{PLH} t_{PLH}	Propagation delay A or B to A<B, A>B	Waveform 1 3 logic levels	6.0 7.0	8.5 9.5	11.0 14.0	5.5 6.5	13.0 15.5	ns
t_{PLH} t_{PLH}	Propagation delay A or B to A=B	Waveform 1 4 logic levels	6.5 7.0	9.0 9.5	11.5 14.0	6.0 6.5	14.0 14.5	ns
t_{PLH} t_{PLH}	Propagation delay $I_{A<B}$ and $I_{A=B}$ to A>B	Waveform 1 1 logic level	3.0 3.0	5.0 6.0	7.5 9.0	2.5 2.5	9.0 10.0	ns
t_{PLH} t_{PLH}	Propagation delay $I_{A=B}$ to A=B	Waveform 1 2 logic levels	2.5 3.5	4.5 7.5	7.0 10.0	2.0 2.5	9.0 12.0	ns
t_{PLH} t_{PLH}	Propagation delay $I_{A>B}$ and $I_{A=B}$ to A<B	Waveform 1 1 logic level	3.0 3.0	5.0 6.0	8.0 9.0	3.0 2.0	9.5 9.5	ns

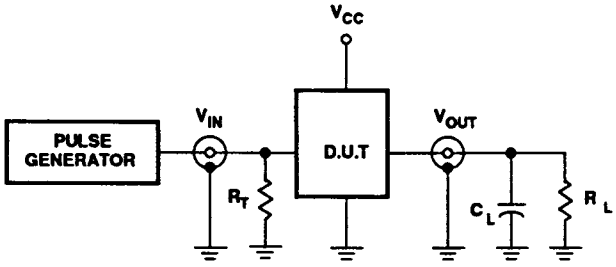
AC WAVEFORMS



Waveform 1. Propagation Delay Input To Output

NOTE: For all waveforms, V_M = 1.5V

TEST CIRCUIT AND WAVEFORMS



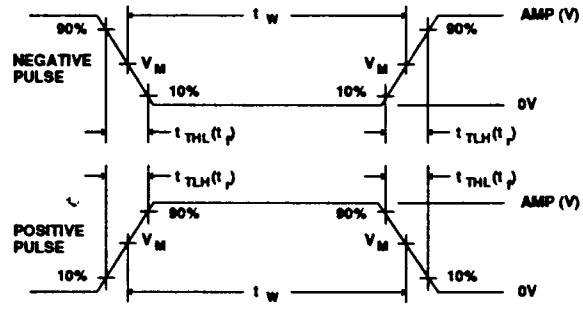
Test Circuit For Totem-Pole Outputs

DEFINITIONS

R_L = Load resistor; see AC CHARACTERISTICS for value.

C_L = Load capacitance includes jig and probe capacitance; see AC CHARACTERISTICS for value.

R_T = Termination resistance should be equal to Z_{OUT} of pulse generators.



V_M = 1.5V

Input Pulse Definition

FAMILY	INPUT PULSE REQUIREMENTS				
	Amplitude	Rep. Rate	t_W	t_{TLH}	t_{THL}
74F	3.0V	1MHz	500ns	2.5ns	2.5ns

VI. COMMERCIAL PRODUCT SPECIAL PROCESSING T-90-20

SUPR II LEVEL B

Signetics Upgraded Product Reliability (SUPR) program is designed to provide customers whose systems require an infant mortality level less than that of our non-burned-in products (which is typically below 1000 PPM).

DEVICE AVAILABILITY

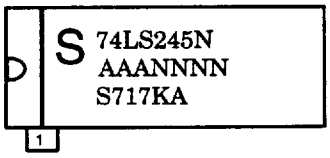
Products available for Level B processing are identified in the Price Book with a "B" suffix to the basic part number.

SUPR II LEVEL B PRICING ADDERS

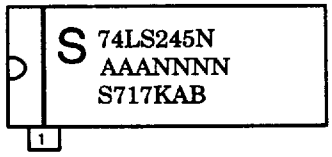
PRODUCT FAMILY	SUGGESTED RESALE ADDERS 1–99	100–999	OVER 1000
LIN	.14	.14	.11
LOG (TTL)			
(SSI)	.12	.10	.08
(MSI)	.16	.14	.11
(OCT)	.16	.14	.11
(CTM)	.16	.14	.11
LOG (ECL)			
(SSI)	.25	.23	.20
(MSI)	.25	.23	.20
LOG (LSI) (RAM) MIC (8X)	Consult Factory for Pricing		
PLD	Consult Factory for Pricing		
MCG	Consult Factory for Pricing		
DAT MIC	Not Available		

MARKING FORMAT EXAMPLES

Standard (no Burn-In) Products (Dual-in-line)



SUPR II (Burned-In) Products (Dual-in-line)



NOTE: The "B" in the 7th position on the 3rd line, when present, is the SUPR II Burn-In indicator.

TAPE AND REEL PACKAGING

SPECIFICATIONS

Tape and Reel specifications conform to Electronic Industries Association (EIA) Proposed Specification #EIA-481-A using 13 inch reels. Current incremental quantities reflect the quantities per reel. As more customers are able to handle a larger quantity per reel, this quantity will be increased.

DEVICE AVAILABILITY

Products available in tape and reel packaging are identified in the Price Book with a "T" suffix to the basic part number and are only offered as a product for sale by the reel. Return of product is limited to full reels with unbroken quality seals.

TAPE AND REEL PRICING ADDERS

PRODUCT FAMILY	SUGGESTED RESALE ADDER
MCG	.07
LIN	.07
LOG	.07
DAT MIC	PACKAGE A28 = .20 A44 = .25 A52 = .30 A68 = .40 A84 = .45 D24 = .17

VII. PACKING QUANTITY INFORMATION

T-90-20

CERAMIC DUAL IN-LINE (CERDIP)

PACKAGE CODE	PIN COUNT	QUANTITIES	
		DEVICES PER TUBE	DEVICES PER BOX
F/FE, BPA, PA	8-pin (300-mil)	48	1920
F, BCA, CA	14-pin (300-mil)	25	1000
F, BEA, EA	16-pin (300-mil)	25	1000
F, BVA, MVA	18-pin (300-mil)	21	840
F/FA, BRA, RA	20-pin (300-mil)	20	800
F, BWA, WA	22-pin (400-mil)	17	544
F/FA/F6, BJA, JA	24-pin (600-mil)	15	360
F/FA/F3/F24, BLA, LA	24-pin (300-mil)	15	600
F, BXA, XA	24-pin (400-mil)	15	480
F/FA/F28, BXA, XA	28-pin (600-mil)	13	312
FA	32-pin (600-mil)	11	264
F/FA/F40, BQA, MQA, QA	40-pin (600-mil)	9	216

CERPAC

PACKAGE CODE	PIN COUNT	QUANTITIES
		DEVICES PER TUBE
BDA/DA/W	14-pin	145
BFA/FA/W	16-pin	145
BXA/BYA/W	18-pin	100
BSA/SA/W/WB	20-pin	100
BKA/KA/W	24-pin	120
BYA/YA/W	28-pin	50

CERQUAD

PACKAGE CODE	PIN COUNT	QUANTITIES	
		DEVICES PER TRAY	DEVICES PER BOX
KA/K44	44-pin	6	6
KA/K68	68-pin	4	4
KA	84-pin	42	210

LEADLESS CHIP CARRIER

PACKAGE CODE	PIN COUNT	QUANTITIES
		DEVICES PER TUBE
B2A/2A/GA	20-pin	55
B3A/3A/GA/GC1	28-pin	43
YA/YA/GC2	32-pin	35
BUA/MXA/MUA/UA/XA/GA/GC	44-pin	27
BZA/BUA/UA/ZA/GA/GC	68-pin	19

QUANTITIES SHOWN IN GRAY REQUIRE PURCHASE TO BE MADE IN EXACT MULTIPLES OF THAT QUANTITY.

VII. PACKING QUANTITY INFORMATION

T-90-20

PLASTIC DUAL IN-LINE

PACKAGE CODE	PIN COUNT	QUANTITIES	
		DEVICES PER TUBE	DEVICES PER BOX
N/N8	8-pin (300-mil)	50	2000
N/N14/N16	14- 16-pin (300-mil)	25	1000
N	18-pin (300-mil)	20	800
N/N20	20-pin (300-mil)	18	720
N	22-pin (400-mil)	17	544
N/N6	24-pin (600-mil)	15	360
N/N3/N24	24-pin (300-mil)	15	600
N/N24	24-pin (400-mil)	15	480
N/N28	28-pin (600-mil)	13	312
N/N3	28-pin (300-mil)	13	520
N	32-pin (600-mil)	11	264
N/N40	40-pin (600-mil)	9	216
NB (Shrink)	42-pin (600-mil)	12	288
N/N48	48-pin (600-mil)	7	168
N	50-pin (900-mil)	7	112
N/N64	64-pin (900-mil)	5	80

PLASTIC LEADED CHIP CARRIER (PLCC)

PACKAGE CODE	PIN COUNT	QUANTITIES		
		DEVICES PER TUBE	DEVICES PER BOX	DEVICES PER REEL
A	20-pin	46	3680	1000
A/A28	28-pin	37	2368	750
A	32-pin	31	2232	750
A/A44	44-pin	26	1248	500
A/A52	52-pin	23	1012	500
A/A68	68-pin	18	648	250
A/A84	84-pin	15	420	250

QUANTITIES SHOWN IN GRAY REQUIRE PURCHASE TO BE MADE IN EXACT MULTIPLES OF THAT QUANTITY.

VII. PACKING QUANTITY INFORMATION

T-90-20

PLASTIC SMALL OUTLINE (SO)

PACKAGE CODE	PIN COUNT	QUANTITIES		
		DEVICES PER TUBE	DEVICES PER BOX	DEVICES PER REEL
D/D8	8-pin (150-mil)	100	10000	2500
D	8-pin (300-mil)	64	2560	1000 – 13" 700 – 7"
D/D14	14-pin (150-mil)	57	5700	2500
D	16-pin (150-mil)	50	5000	2500
D	16-pin (300-mil)	48	1920	1000
DK(SSOP)	20-pin (170-mil)	75	6750	2500
D	20-pin (300-mil)	38	1520	1000
D/D24	24-pin (300-mil)	32	1280	1000
D	28-pin (300-mil)	27	1080	1000
D	40-pin (VSO-40)	31	1240	1000 – 13" 300 – 7"
D	56-pin (VSO-56)	22	616	1000

QUAD FLAT PACK*

PACKAGE CODE	PIN COUNT	QUANTITIES	
		DEVICES PER TRAY	DEVICES PER BOX
B/B44	44-pin	50	500
B/B44	44-pin	96	480
B	52-pin	119	595
B	80-pin	66	330
B	100-pin	50	250
B	120-pin	24	120
B	120-pin (Philips source)	30	150

* Quad Flat Pack parts require dry pack handling according to EIA Standard - 583. These parts are identified in part list section with DRY PACK in the Cross Ref Part No field.

QUANTITIES SHOWN IN GRAY REQUIRE PURCHASE TO BE MADE IN EXACT MULTIPLES OF THAT QUANTITY.

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