ADVANCE INFORMATION



54FCT/74FCT646 Octal Transceiver/Register with TRI-STATE® Outputs

General Description

The 'FCT646 consist of registered bus transceiver circuits, with outputs, D-type flip-flops and control circuitry providing multiplexed transmission of data directly from the input bus or from the internal storage registers. Data on the A or B bus will be loaded into the respective registers on the LOW-to-HIGH transition of the appropriate clock pin (CPAB or CPBA).

FACTTM FCT utilizes NSC quiet series technology to provide improved quiet output switching and dynamic threshold performance.

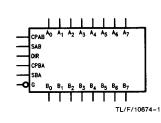
FACT FCT features GTO™ output control and undershoot corrector in addition to a split ground bus for superior performance.

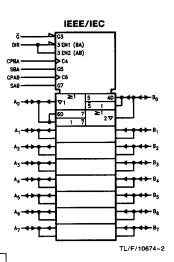
Features

- NSC 54FCT/74FCT646 is pin and functionally equivalent to IDT 54FCT/74FCT646
- Independent registers for A and B buses multiplexed real time and stored time
- Input clamp diodes to limit bus reflections
- TTL/CMOS input and output level compatible
- I_{OL} = 64 mA (Com), 48 mA (Mil)
- CMOS power levels
- 4 kV minimum ESD immunity
- Military product compliant to MIL-STD-883

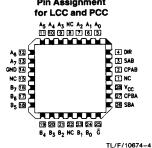
Logic Symbols

Connection Diagrams





Pin Assignment					
for DIP, Flatpak and SOIC					
1					
CPAB-	1	24	–v _{cc}		
SAB-	2	23	CPBA		
DIR-	3	22	— SBA		
- 40−	4	21	- ē		
A1-	5	20	_ в₀		
A2-	6	19	—B₁		
A3-	7	18	— в ₂		
44-	8	17	− 8 ₃		
45-	9	16	—8 ₄		
A6-	10	15	—8 ₅		
A7-	11	14	— В ₆		
GND-	12	13	— В ₇		
	<u> </u>				
			TL/F/10674-3		
Pin Assignment					
for LCC and PCC					



Pin Names	Description
A ₀ -A ₇	Data Register A Inputs
1	Data Register A Outputs
B ₀ -B ₇	Data Register B Inputs
	Data Register B Outputs
CPAB, CPBA	Clock Pulse Inputs
SAB, SBA	Transmit/Receive Inputs
G	Output Enable Input
DIR	Direction Control Input