DS3594-3.3

54HSC/T Series

RADIATION HARD HIGH SPEED CMOS/SOS LOGIC

The CMOS/SOS HSC/T Series offer the combined benefits of low power, high speed CMOS with the inherent latch up immunity, Single Event Upset (SEU) immunity and the high level of radiation hardness of Silicon on Sapphire technology. The 54HSC/T Series of circuits are pin for pin compatible with the 54LS series range.

HSC and HST devices have CMOS and TTL compatible inputs/outputs respectively.

FEATURES

- Radiation Hard to 1MRad (Si)
- High SEU Immunity, Latch Up Free
- Low Power CMOS/SOS Technology
- Plug In Replacement for 54/74LS, HC and HCT
- Dual In Line or Flatpack Packages

Gates and Buffers

54HSC/T00	Quadruple 2-input positive NAND gates
54HSC/T02	Quadruple 2-input positive NOR gates
54HSC/TO3	Quadruple 2-input positive NAND gates with open collector outputs
54HSC/T04	Hex Inverters
54HSC/T08	Quadruple 2-input positive AND gates
54HSC/T10	Triple 3-input positive NAND gates
54HSC14	Hex schmitt-trigger inverters
54HSC/T21	Dual 4-input positive AND gates
54HSC/T27	Triple 3-input positive NOR gates
54HSC/T32	Quadruple 2-input positive OR gates
54HSC/T86	Quadruple 2-input Exclusive OR gates
54HSC/T125	Quadruple bus buffer gates with tri-state outputs (Active low enable)
54HSC/T126	Quadruple bus buffer gates with tri-state outputs (Active high enable)

Flip-Flops

54HSC/T74	Dual D-type flip-flops with preset and clear
54HSC/T109	Dual J-KB flip-flop with preset and clear
54HSC/T273	Octal D-type flip-flops
54HSC/T374	Octal D-type edge triggered flip-flops
54HSC/T574	Octal D-type edge triggered flip-flops

Adders

54HSC/T283	4-bit binary full adders with fast carry

Counters

54HSC/T161	4-bit synchronous binary counter
54HSC/T163	Synchronous 4-bit counter
54HSC/T191	Synchronous 4-bit counter

Decoders/Demultiplexers

54HSC/T138	3-line to 8-line decoder/multiplexer
54HSC/T139	Dual 2 to 4 decoders/multiplexers
54HSC/T148	8-line to 3-line octal priority encoders
54HSC/T151	1 of 8 data selectors/multiplexers
54HSC/T154	4 to 16-line decoders/demultiplexers
54HSC/T157	Quad 2-line to 1-line data selectors/multiplexers
54HSC/T238	3 to 8 decoder/demultiplexer
54HSC/T253	Dual 4 to 1 data selectors/multiplexers

Registers

54HSC/T164	8-bit parallel output serial shift register
54HSC/T165	Parallel load 8-bit shift register
54H5C/T166	8-bit shift register

Comparators

54HSC/T521	8-bit magnitude comparator

Line Drivers

54HSC/T240	Octal 3-state driver inverting
54HSC/T241	Octal 3-state driver complementary enable
54HSC/T244	Octal 3-state driver
54HSC/T540	Octal 3-state driver/buffer inverting
54HSC/T541	Octal 3-state driver/buffer

Transceivers

54HSC/T245	Octal bus transceiver

Latches

54HSC/T373	Octal transparent latch, 3-state outputs
54HSC/T573	Octal transparent latch, 3-state outputs

Miscellaneous

54HSC/T670	4 x 4 register files with tri-state outputs

DC CHARACTERISTICS AND RATINGS

Parameter	Min.	Max.	Units
Supply Voltage	-0.5	10	V
Input Voltage	-0.3	V_{DD}+0.3	V
Current Through Any Pin	-25	+25	mA
Operating Temperature	-55	125	°C
Storage Temperature	-65	150	°C

Figure 1: Absolute Maximum Ratings

Note: Stresses above those listed may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these conditions, or at any other condition above those indicated in the operations section of this specification, is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Symbol	Parameter	Conditions	Total dose radiation not exceeding 3x10^5 Rad(Si)			Units
			Min.	Typ.	Max.	
V_{DD}	Supply Voltage	-	4.5	5.0	5.5	V
V_{IH1}	HST Input High Voltage	-	2.0	-	-	V
V_{IL1}	HST Input Low Voltage	-	-	-	0.8	V
V_{IH2}	HSC Input High Voltage	-	3.5	-	-	V
V_{IL2}	HSC Input Low Voltage	-	-	-	1.5	V
V_{OH}	Output High Voltage	V_{IN} = V_{IH} or V_{IL}				
		I_{OH} = -20µA*	V_{DD}-0.1	-	-	V
		I_{OH} = 6mA*	3.7	-	-	V
		I_{OH} = -11mA	2.5	-	-	V
V_{OL}	Output Low Voltage	V_{IN} = V_{IH} or V_{IL}				
		I_{OL} = -20µA*	-	-	0.1	V
		I_{OL} = 6mA*	-	-	0.2	V
		I_{OL} = 9mA	-	-	0.4	V
I_{IL}	Input Leakage Current	V_{IN} = V_{DD} or V_{SS} All inputs	-	1	5	µA
I_{OL}	Output Leakage Current	V_{OUT} = V_{DD} or V_{SS} Outputs disabled	-	20	50	µA
I_{DD}	Quiescent Current	V_{IN} = V_{DD} Outputs unloaded	-	†	†	µA

V_{DD} = 5V±10%, over full operating temperature range.
* Guaranteed but not tested.
† Refer to individual device types (-55°C / +125°C).

Figure 2: Electrical Characteristics

54HSC/T00 : Quadruple 2-Input Positive NAND Gates

The 54HSC/T00 is a Quadruple 2-Input Positive NAND gate.

Inputs		Outputs
A	B	Y
L	L	H
L	H	H
H	L	H
H	H	L

H = high level, L = low level

Figure 1: Function Table

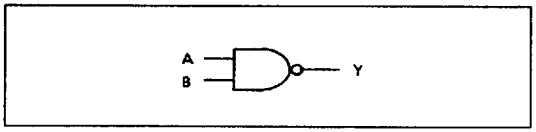


Figure 2: Logic Diagram

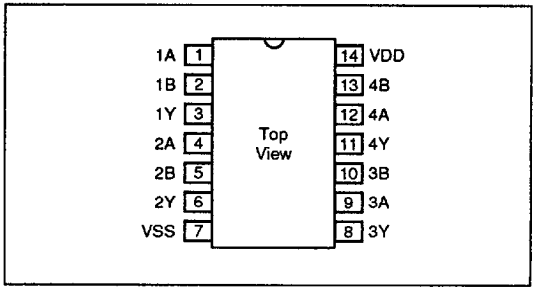


Figure 3: Pin Out

Symbol	Parameter	+25°C		-55°C / +125°C		Units
		Typ.	Max.	Typ.	Max.	
t_{PLH}	Propagation delay time, low to high level output	11	20	17	22	ns
t_{PHL}	Propagation delay time, high to low level output	10	18	18	20	ns

Figure 4: Switching Characteristics

Symbol	Parameter	Test Conditions	Limits				Units
			+25°C		-55°C / +125°C		
			Min.	Max.	Min.	Max.	
I_{DD}	Quiescent Current	V_{IN} = 0V or V_{DD}	-	10	-	300	µA
V_{OL}	Output Voltage Low Level	I_{OL} = 9mA	-	0.4	-	0.4	V
V_{OH}	Output Voltage High Level	I_{OH} = -11mA	2.5	-	2.5	-	V
V_{IL1}	Voltage Input Low (CMOS)	-	-	1.5	-	1.5	V
V_{IH1}	Voltage Input High (CMOS)	-	3.5	-	3.5	-	V
V_{IL2}	Voltage Input Low (TTL)	-	-	0.8	-	0.8	V
V_{IH2}	Voltage Input High (TTL)	-	2.0	-	2.0	-	V
I_{IN}	Input Leakage Current	V_{IN} = V_{DD} or V_{SS}	-	±0.5	-	±5.0	µA

Figure 5: DC Characteristics

54HSC/T02 : Quadruple 2-Input Positive NOR Gates

The 54HSC/T02 is a Quadruple 2-Input Positive NOR gate.

Inputs		Outputs
A	B	Y
L	L	H
L	H	L
H	L	L
H	H	L

H = high level, L = low level

Figure 1: Function Table

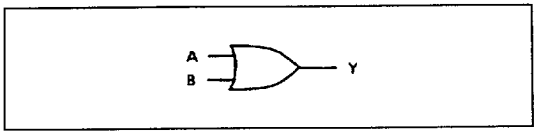


Figure 2: Logic Diagram

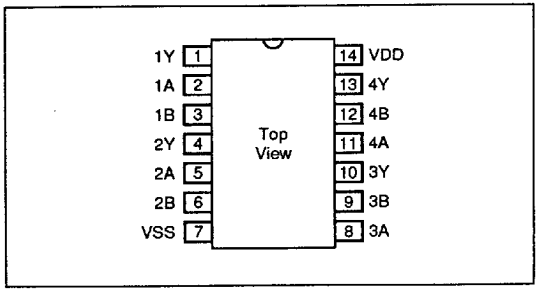


Figure 3: Pin Out

Symbol	Parameter	+25°C		-55°C / +125°C		Units
		Typ.	Max.	Typ.	Max.	
t_{PLH}	Propagation delay time, low to high level output	11	20	17	22	ns
t_{PHL}	Propagation delay time, high to low level output	10	18	18	20	ns

Figure 4: Switching Characteristics

Symbol	Parameter	Test Conditions	Limits				Units
			+25°C		-55°C / +125°C		
			Min.	Max.	Min.	Max.	
I_{DD}	Quiescent Current	V_{IN} = 0V or V_{DD}	-	10	-	300	µA
V_{OL}	Output Voltage Low Level	I_{OL} = 9mA	-	0.4	-	0.4	V
V_{OH}	Output Voltage High Level	I_{OH} = -11mA	2.5	-	2.5	-	V
V_{IL1}	Voltage Input Low (CMOS)	-	-	1.5	-	1.5	V
V_{IH1}	Voltage Input High (CMOS)	-	3.5	-	3.5	-	V
V_{IL2}	Voltage Input Low (TTL)	-	-	0.8	-	0.8	V
V_{IH2}	Voltage Input High (TTL)	-	2.0	-	2.0	-	V
I_{IN}	Input Leakage Current	V_{IN} = V_{DD} or V_{SS}	-	±0.5	-	±5.0	µA

Figure 5: DC Characteristics

54HSC/T03 : Quadruple 2-Input Positive NAND Gates With Open Collector Outputs

The 54HSC/T03 is a Quadruple 2-Input Positive NAND gate with open collector output.

Inputs		Outputs
A	B	Y
L	L	H
L	H	H
H	L	H
H	H	L

H = high level, L = low level

Figure 1: Function Table

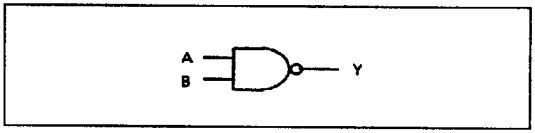


Figure 2: Logic Diagram

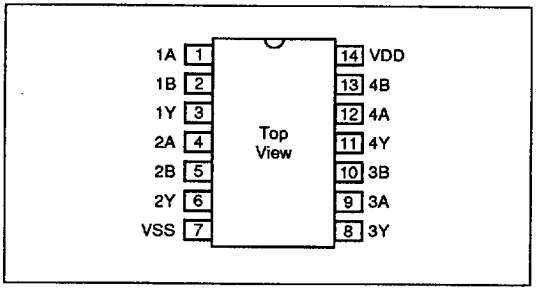


Figure 3: Pin Out

Symbol	Parameter	+25°C		-55°C / +125°C		Units
		Typ.	Max.	Typ.	Max.	
t_{PLH}	Propagation delay time, low to high level output	11	20	17	22	ns
t_{PHL}	Propagation delay time, high to low level output	10	18	18	20	ns

Figure 4: Switching Characteristics

Symbol	Parameter	Test Conditions	Limits				Units
			+25°C		-55°C / +125°C		
			Min.	Max.	Min.	Max.	
I_{DD}	Quiescent Current	V_{IN} = 0V or V_{DD}	-	10	-	300	µA
V_{OL}	Output Voltage Low Level	I_{OL} = 9mA	-	0.4	-	0.4	V
V_{OH}	Output Voltage High Level	I_{OH} = -11mA	2.5	-	2.5	-	V
V_{IL1}	Voltage Input Low (CMOS)	-	-	1.5	-	1.5	V
V_{IH1}	Voltage Input High (CMOS)	-	3.5	-	3.5	-	V
V_{IL2}	Voltage Input Low (TTL)	-	-	0.8	-	0.8	V
V_{IH2}	Voltage Input High (TTL)	-	2.0	-	2.0	-	V
I_{IN}	Input Leakage Current	V_{IN} = V_{DD} or V_{SS}	-	±0.5	-	±0.5	µA

Figure 5: DC Characteristics

54HSC/T04 : Hex Inverters

The 54HSC/T04 consists of six Hex Inverters.

Inputs	Outputs
A	Y
H	L
L	H

H = high level, L = low level

Figure 1: Function Table

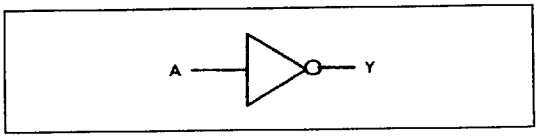


Figure 2: Logic Diagram

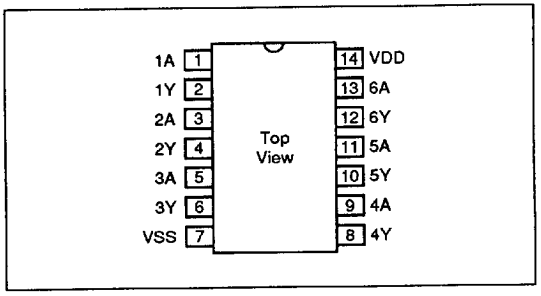


Figure 3: Pin Out

Symbol	Parameter	+25°C		-55°C / +125°C		Units
		Typ.	Max.	Typ.	Max.	
t_{PLH}	Propagation delay time, low to high level output	11	20	17	22	ns
t_{PHL}	Propagation delay time, high to low level output	10	18	18	20	ns

Figure 4: Switching Characteristics

Symbol	Parameter	Test Conditions	Limits				Units
			+25°C		-55°C / +125°C		
			Min.	Max.	Min.	Max.	
I_{DD}	Quiescent Current	V_{IN} = 0V or V_{DD}	-	10	-	300	µA
V_{OL}	Output Voltage Low Level	I_{OL} = 9mA	-	0.4	-	0.4	V
V_{OH}	Output Voltage High Level	I_{OH} = -11mA	2.5	-	2.5	-	V
V_{IL1}	Voltage Input Low (CMOS)	-	-	1.5	-	1.5	V
V_{IH1}	Voltage Input High (CMOS)	-	3.5	-	3.5	-	V
V_{IL2}	Voltage Input Low (TTL)	-	-	0.8	-	0.8	V
V_{IH2}	Voltage Input High (TTL)	-	2.0	-	2.0	-	V
I_{IN}	Input Leakage Current	V_{IN} = V_{DD} or V_{SS}	-	±0.5	-	±5.0	µA

Figure 5: DC Characteristics

54HSC/T08 : Quadruple 2-Input Positive AND Gates

The 54HSC/T08 is a Quadruple 2-Input Positive AND gate.

Inputs		Outputs
A	B	Y
L	L	L
L	H	L
H	L	L
H	H	H

H = high level, L = low level

Figure 1: Function Table

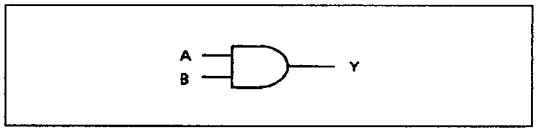


Figure 2: Logic Diagram

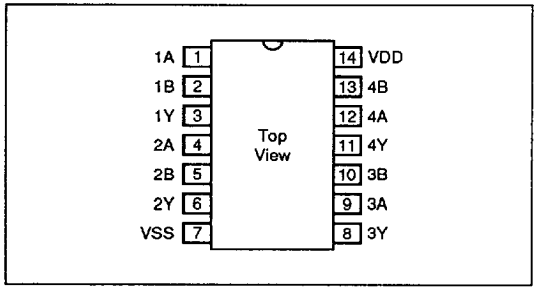


Figure 3: Pin Out

Symbol	Parameter	+25°C		-55°C / +125°C		Units
		Typ.	Max.	Typ.	Max.	
t_{PLH}	Propagation delay time, low to high level output	11	20	17	22	ns
t_{PHL}	Propagation delay time, high to low level output	10	18	18	20	ns

Figure 4: Switching Characteristics

Symbol	Parameter	Test Conditions	Limits				Units
			+25°C		-55°C / +125°C		
			Min.	Max.	Min.	Max.	
I_{DD}	Quiescent Current	V_{IN} = 0V or V_{DD}	-	10	-	300	µA
V_{OL}	Output Voltage Low Level	I_{OL} = 9mA	-	0.4	-	0.4	V
V_{OH}	Output Voltage High Level	I_{OH} = -11mA	2.5	-	2.5	-	V
V_{IL1}	Voltage Input Low (CMOS)	-	-	1.5	-	1.5	V
V_{IH1}	Voltage Input High (CMOS)	-	3.5	-	3.5	-	V
V_{IL2}	Voltage Input Low (TTL)	-	-	0.8	-	0.8	V
V_{IH2}	Voltage Input High (TTL)	-	2.0	-	2.0	-	V
I_{IN}	Input Leakage Current	V_{IN} = V_{DD} or V_{SS}	-	±0.5	-	±5.0	µA

Figure 5: DC Characteristics

54HSC/T10 : Triple 3-Input Positive NAND Gates

The 54HSC/T10 is a Triple 3-Input Positive NAND gate.

Inputs			Outputs
A	B	C	Y
L	X	X	H
X	L	X	H
X	X	L	H
H	H	H	L

H = high level, L = low level, X = irrelevant

Figure 1: Function Table

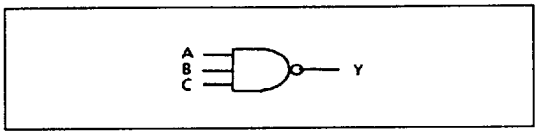


Figure 2: Logic Diagram

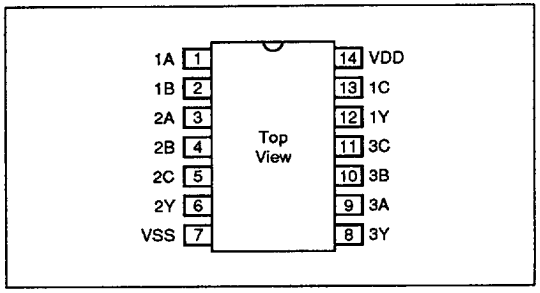


Figure 3: Pin Out

Symbol	Parameter	+25°C		-55°C / +125°C		Units
		Typ.	Max.	Typ.	Max.	
t_{PLH}	Propagation delay time, low to high level output	11	20	17	22	ns
t_{PHL}	Propagation delay time, high to low level output	10	18	18	20	ns

Figure 4: Switching Characteristics

Symbol	Parameter	Test Conditions	Limits				Units
			+25°C		-55°C / +125°C		
			Min.	Max.	Min.	Max.	
I_{DD}	Quiescent Current	V_{IN} = 0V or V_{DD}	-	10	-	300	µA
V_{OL}	Output Voltage Low Level	I_{OL} = 9mA	-	0.4	-	0.4	V
V_{OH}	Output Voltage High Level	I_{OH} = -11mA	2.5	-	2.5	-	V
V_{IL1}	Voltage Input Low (CMOS)	-	-	1.5	-	1.5	V
V_{IH1}	Voltage Input High (CMOS)	-	3.5	-	3.5	-	V
V_{IL2}	Voltage Input Low (TTL)	-	-	0.8	-	0.8	V
V_{IH2}	Voltage Input High (TTL)	-	2.0	-	2.0	-	V
I_{IN}	Input Leakage Current	V_{IN} = V_{DD} or V_{SS}	-	±0.5	-	±5.0	µA

Figure 5: DC Characteristics

54HSC14 : Hex Schmitt-Trigger Inverters

The 54HSC/T14 consists of six Hex Schmitt-Trigger Inverters.

Inputs	Outputs
A	Y
L	H
H	L

H = high level, L = low level

Figure 1: Function Table

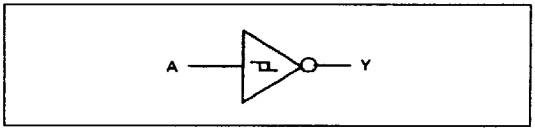


Figure 2: Logic Diagram

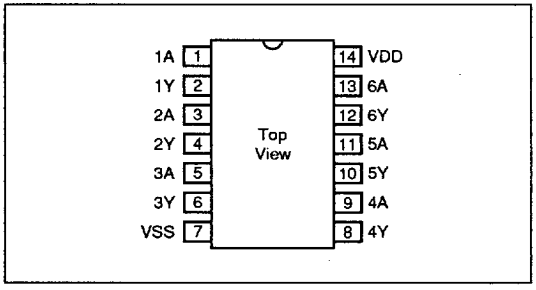


Figure 3: Pin Out

Symbol	Parameter	+25°C		-55°C / +125°C		Units
		Typ.	Max.	Typ.	Max.	
t_{PLH}	Propagation delay time, low to high level output	11	20	17	22	ns
t_{PHL}	Propagation delay time, high to low level output	10	18	18	20	ns

Figure 4: Switching Characteristics

Symbol	Parameter	Test Conditions	Limits				Units
			+25°C		-55°C / +125°C		
			Min.	Max.	Min.	Max.	
I_{DD}	Quiescent Current	V_{IN} = 0V or V_{DD}	-	10	-	300	µA
V_{OL}	Output Voltage Low Level	I_{OL} = 9mA	-	0.4	-	0.4	V
V_{OH}	Output Voltage High Level	I_{OH} = -11mA	2.5	-	2.5	-	V
V_{IL1}	Voltage Input Low (CMOS)	-	-	1.5	-	1.5	V
V_{IH1}	Voltage Input High (CMOS)	-	3.5	-	3.5	-	V
V_{IL2}	Voltage Input Low (TTL)	-	-	0.8	-	0.8	V
V_{IH2}	Voltage Input High (TTL)	-	2.0	-	2.0	-	V
I_{IN}	Input Leakage Current	V_{IN} = V_{DD} or V_{SS}	-	±0.5	-	±5.0	µA

Figure 5: DC Characteristics

54HSC/T21 : Dual 4-Input Positive AND Gates

The 54HSC/T21 is a Dual 4-Input Positive AND gate.

Inputs				Outputs
A	B	C	D	Y
L	L	L	L	L
L	L	L	H	L
L	L	H	L	L
L	L	H	H	L
L	H	L	L	L
L	H	L	H	L
L	H	H	L	L
L	H	H	H	L
H	L	L	L	L
H	L	L	H	L
H	L	H	L	L
H	L	H	H	L
H	H	L	L	L
H	H	L	H	L
H	H	H	L	L
H	H	H	H	H

H = high level, L = low level

Figure 1: Function Table

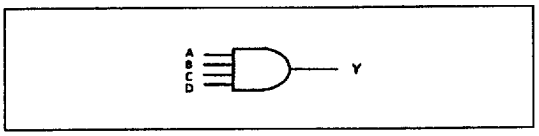


Figure 2: Logic Diagram

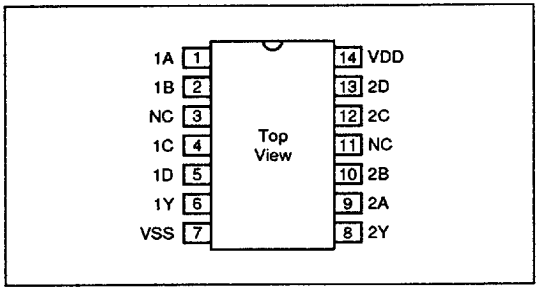


Figure 3: Pin Out

Symbol	Parameter	+25°C		-55°C / +125°C		Units
		Typ.	Max.	Typ.	Max.	
t_{PLH}	Propagation delay time, low to high level output	11	20	17	22	ns
t_{PHL}	Propagation delay time, high to low level output	10	18	18	20	ns

Figure 4: Switching Characteristics

Symbol	Parameter	Test Conditions	Limits				Units
			+25°C		-55°C / +125°C		
			Min.	Max.	Min.	Max.	
I_{DD}	Quiescent Current	V_{IN} = 0V or V_{DD}	-	10	-	300	µA
V_{OL}	Output Voltage Low Level	I_{OL} = 9mA	-	0.4	-	0.4	V
V_{OH}	Output Voltage High Level	I_{OH} = -11mA	2.5	-	2.5	-	V
V_{IL1}	Voltage Input Low (CMOS)	-	-	1.5	-	1.5	V
V_{IH1}	Voltage Input High (CMOS)	-	3.5	-	3.5	-	V
V_{IL2}	Voltage Input Low (TTL)	-	-	0.8	-	0.8	V
V_{IH2}	Voltage Input High (TTL)	-	2.0	-	2.0	-	V
I_{IN}	Input Leakage Current	V_{IN} = V_{DD} or V_{SS}	-	±0.5	-	±5.0	µA

Figure 5: DC Characteristics

54HSC/T27 : Triple 3-Input Positive NOR Gates

The 54HSC/T27 is a Triple 3-Input Positive NOR gate.

Inputs			Outputs
A	B	C	Y
L	L	L	H
L	L	H	L
L	H	L	L
L	H	H	L
H	L	L	L
H	L	H	L
H	H	L	L
H	H	H	L

H = high level, L = low level

Figure 1: Function Table

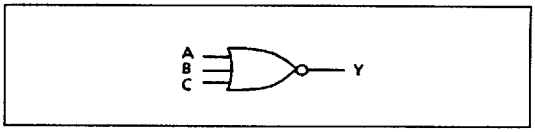


Figure 2: Logic Diagram

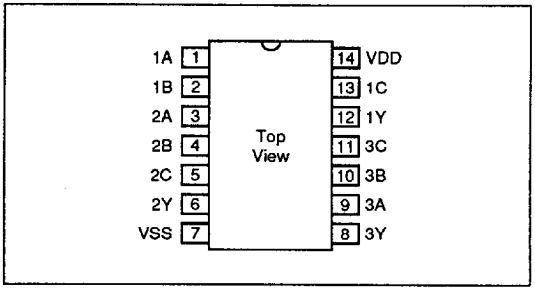


Figure 3: Pin Out

Symbol	Parameter	+25°C		-55°C / +125°C		Units
		Typ.	Max.	Typ.	Max.	
t_{PLH}	Propagation delay time, low to high level output	11	20	17	22	ns
t_{PHL}	Propagation delay time, high to low level output	10	18	18	20	ns

Figure 4: Switching Characteristics

Symbol	Parameter	Test Conditions	Limits				Units
			+25°C		-55°C / +125°C		
			Min.	Max.	Min.	Max.	
I_{DD}	Quiescent Current	V_{IN} = 0V or V_{DD}	-	10	-	300	µA
V_{OL}	Output Voltage Low Level	I_{OL} = 9mA	-	0.4	-	0.4	V
V_{OH}	Output Voltage High Level	I_{OH} = -11mA	2.5	-	2.5	-	V
V_{IL1}	Voltage Input Low (CMOS)	-	-	1.5	-	1.5	V
V_{IH1}	Voltage Input High (CMOS)	-	3.5	-	3.5	-	V
V_{IL2}	Voltage Input Low (TTL)	-	-	0.8	-	0.8	V
V_{IH2}	Voltage Input High (TTL)	-	2.0	-	2.0	-	V
I_{IN}	Input Leakage Current	V_{IN} = V_{DD} or V_{SS}	-	±0.5	-	±5.0	µA

Figure 5: DC Characteristics

54HSC/T32 : Quadruple 2-Input Positive OR Gates

The 54HSC/T32 is a Quadruple 2-Input Positive OR gate.

Inputs		Outputs
A	B	Y
L	L	L
L	H	H
H	L	H
H	H	H

H = high level, L = low level

Figure 1: Function Table

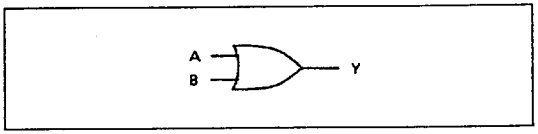


Figure 2: Logic Diagram

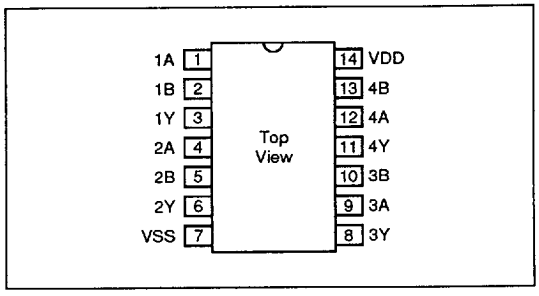


Figure 3: Pin Out

Symbol	Parameter	+25°C		-55°C / +125°C		Units
		Typ.	Max.	Typ.	Max.	
t_{PLH}	Propagation delay time, low to high level output	11	20	17	22	ns
t_{PHL}	Propagation delay time, high to low level output	10	18	18	20	ns

Figure 4: Switching Characteristics

Symbol	Parameter	Test Conditions	Limits				Units
			+25°C		-55°C / +125°C		
			Min.	Max.	Min.	Max.	
I_{DD}	Quiescent Current	V_{IN} = 0V or V_{DD}	-	10	-	300	µA
V_{OL}	Output Voltage Low Level	I_{OL} = 9mA	-	0.4	-	0.4	V
V_{OH}	Output Voltage High Level	I_{OH} = -11mA	2.5	-	2.5	-	V
V_{IL1}	Voltage Input Low (CMOS)	-	-	1.5	-	1.5	V
V_{IH1}	Voltage Input High (CMOS)	-	3.5	-	3.5	-	V
V_{IL2}	Voltage Input Low (TTL)	-	-	0.8	-	0.8	V
V_{IH2}	Voltage Input High (TTL)	-	2.0	-	2.0	-	V
I_{IN}	Input Leakage Current	V_{IN} = V_{DD} or V_{SS}	-	±0.5	-	±5.0	µA

Figure 5: DC Characteristics

54HSC/T86 : Quadruple 2-Input Exclusive OR Gates

The 54HSC/T86 is a Quadruple 2-Input Exclusive OR gate.

Inputs		Outputs
A	B	Y
L	L	L
L	H	H
H	L	H
H	H	L

H = high level, L = low level

Figure 1: Function Table

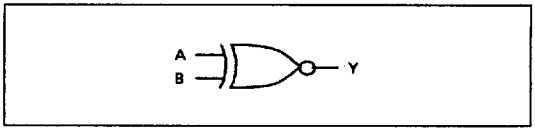


Figure 2: Logic Diagram

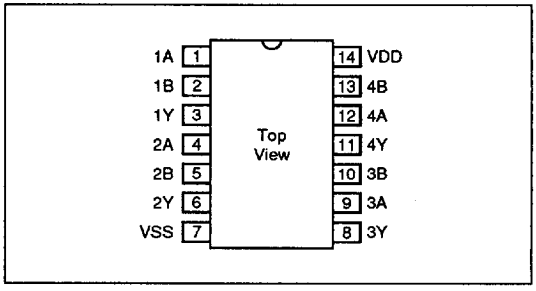


Figure 3: Pin Out

Symbol	Parameter	+25°C		-55°C / +125°C		Units
		Typ.	Max.	Typ.	Max.	
t_{PLH}	Propagation delay time, low to high level output	11	20	17	22	ns
t_{PHL}	Propagation delay time, high to low level output	10	18	18	20	ns

Figure 4: Switching Characteristics

Symbol	Parameter	Test Conditions	Limits				Units
			+25°C		-55°C / +125°C		
			Min.	Max.	Min.	Max.	
I_{DD}	Quiescent Current	V_{IN} = 0V or V_{DD}	-	10	-	300	µA
V_{OL}	Output Voltage Low Level	I_{OL} = 9mA	-	0.4	-	0.4	V
V_{OH}	Output Voltage High Level	I_{OH} = -11mA	2.5	-	2.5	-	V
V_{IL1}	Voltage Input Low (CMOS)	-	-	1.5	-	1.5	V
V_{IH1}	Voltage Input High (CMOS)	-	3.5	-	3.5	-	V
V_{IL2}	Voltage Input Low (TTL)	-	-	0.8	-	0.8	V
V_{IH2}	Voltage Input High (TTL)	-	2.0	-	2.0	-	V
I_{IN}	Input Leakage Current	V_{IN} = V_{DD} or V_{SS}	-	±0.5	-	±5.0	µA

Figure 5: DC Characteristics

54HSC/T125 : Quadruple Bus Buffer Gates with Tri-State Outputs (Active Low Enable)

The 54HSC/T125 is a Quadruple Bus Buffer Gate. When G is low the A input is transferred to the Y output. When G is high the output is in a high impedance state.

Inputs		Outputs
$\overline{G}$	A	Y
L	L	L
L	H	H
H	L	Z
H	H	Z

H = high level, L = low level, Z = high impedance

Figure 1: Function Table

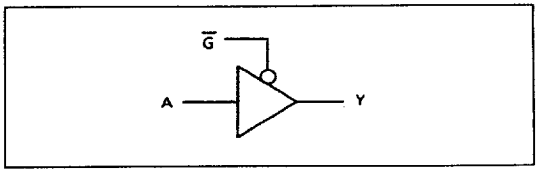


Figure 2: Logic Diagram

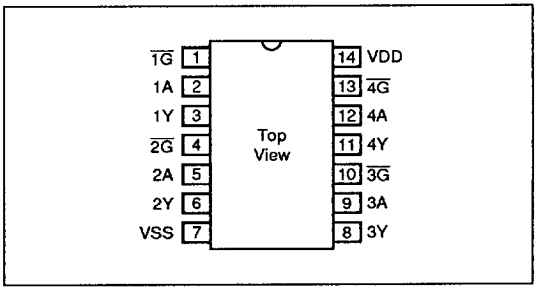


Figure 3: Pin Out

Symbol	Parameter	+25°C		-55°C / +125°C		Units
		Typ.	Max.	Typ.	Max.	
t_{PLH}	Propagation delay A to Y	15	18	18	28	ns
t_{PHL}	Propagation delay A to Y	15	20	18	28	ns
t_{PZH}	Propagation delay G to Y	12	25	15	28	ns
t_{PZL}	Propagation delay G to Y	12	25	15	28	ns
t_{PHZ}	Propagation delay Y to Tri-State	12	25	15	28	ns
t_{PLZ}	Propagation delay Y to Tri-State	12	25	15	28	ns

Figure 4: Switching Characteristics

54HSC/T125 : Quadruple Bus Buffer Gates with Tri-State Outputs (Active Low Enable)

Symbol	Parameter	Test Conditions	Limits				Units
			+25°C		-55°C / +125°C		
			Min.	Max.	Min.	Max.	
I_{DD}	Quiescent Current	V_{IN} = 0V or V_{DD}	-	10	-	400	µA
V_{OL}	Output Voltage Low Level	I_{OL} = 9mA	-	0.4	-	0.4	V
V_{OH}	Output Voltage High Level	I_{OH} = -11mA	2.5	-	2.5	-	V
V_{IL1}	Voltage Input Low (CMOS)	-	-	1.5	-	1.5	V
V_{IH1}	Voltage Input High (CMOS)	-	3.5	-	3.5	-	V
V_{IL2}	Voltage Input Low (TTL)	-	-	0.8	-	0.8	V
V_{IH2}	Voltage Input High (TTL)	-	2.0	-	2.0	-	V
I_{IN}	Input Leakage Current	V_{IN} = V_{DD} or V_{SS}	-	±0.5	-	±5.0	µA

Figure 5: DC Characteristics

54HSC/T126 : Quadruple Bus Buffer Gates with Tri-State Outputs (Active High Enable)

The 54HSC/T126 is a Quadruple Bus Buffer Gate. When G is high the A input is transferred tp the Y output. When G is low the output is in a high impedance state.

Inputs		Outputs
G	A	Y
H	L	L
H	H	H
L	L	Z
L	H	Z

H = high level, L = low level, Z = high impedance

Figure 1: Function Table

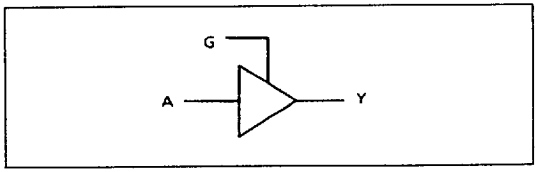


Figure 2: Logic Diagram

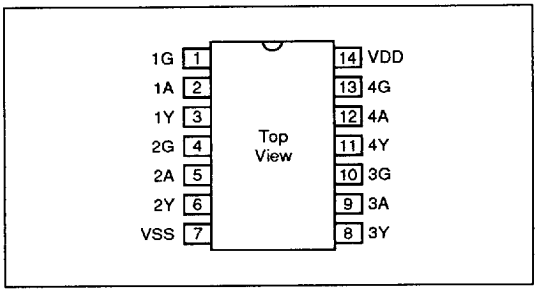


Figure 3: Pin Out

Symbol	Parameter	+25°C		-55°C / +125°C		Units
		Typ.	Max.	Typ.	Max.	
t_{PLH}	Propagation delay A to Y	14	25	17	28	ns
t_{PHL}	Propagation delay A to Y	15	25	19	28	ns
t_{PZH}	Propagation delay G to Y	15	25	18	28	ns
t_{PZL}	Propagation delay G to Y	17	25	19	28	ns
t_{PHZ}	Propagation delay Y to Tri-State	17	25	20	28	ns
t_{PLZ}	Propagation delay Y to Tri-State	15	25	19	28	ns

Figure 4: Switching Characteristics

54HSC/T126 : Quadruple Bus Buffer Gates with Tri-State Outputs (Active High Enable)

Symbol	Parameter	Test Conditions	Limits				Units
			+25°C		-55°C / +125°C		
			Min.	Max.	Min.	Max.	
I_{DD}	Quiescent Current	V_{IN} = 0V or V_{DD}	-	10	-	400	µA
V_{OL}	Output Voltage Low Level	I_{OL} = 9mA	-	0.4	-	0.4	V
V_{OH}	Output Voltage High Level	I_{OH} = -11mA	2.5	-	2.5	-	V
V_{IL1}	Voltage Input Low (CMOS)	-	-	1.5	-	1.5	V
V_{IH1}	Voltage Input High (CMOS)	-	3.5	-	3.5	-	V
V_{IL2}	Voltage Input Low (TTL)	-	-	0.8	-	0.8	V
V_{IH2}	Voltage Input High (TTL)	-	2.0	-	2.0	-	V
I_{IN}	Input Leakage Current	V_{IN} = V_{DD} or V_{SS}	-	±0.5	-	±5.0	µA

Figure 5: DC Characteristics

54HSC/T74 : Dual D-Type Flip-Flops with Preset and Clear

The 54HSC/T74 is a Dual D-Type Flip-Flop. The D inputs are transferred to the Q outputs on the positive going edge of the clock pulse. The clear is active low.

Inputs				Output	
$\overline{PRESET}$	$\overline{CLEAR}$	CLOCK	D	Q	$\overline{Q}$
L	H	X	X	H	L
H	L	X	X	L	H
L	L	X	X	H*	H*
H	H	L-H	H	H	L
H	H	L-H	L	L	H
H	H	L	X	Q_0	$\overline{Q}_0$

H = high level, L = low level, X = irrelevant, * = unknown return state

Figure 1: Function Table

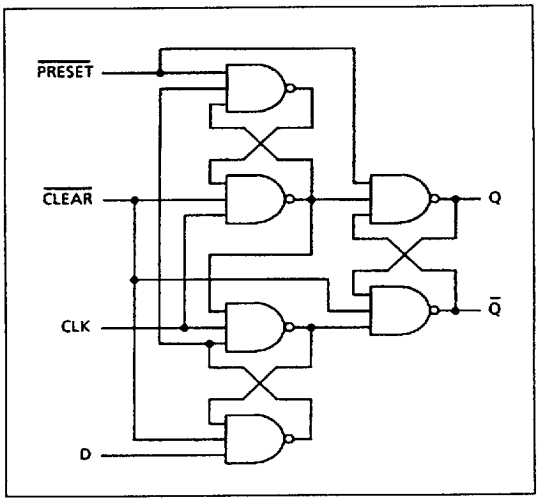


Figure 2: Logic Diagram

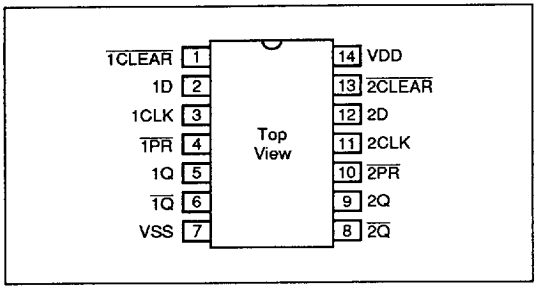


Figure 3: Pin Out

Symbol	Parameter	+25°C		-55°C / +125°C		Units
		Typ.	Max.	Typ.	Max.	
t_{PLH}	Propagation delay. Preset to Q or $\overline{Q}$.	15	20	18	24	ns
t_{PHL}	Propagation delay. Preset to Q or $\overline{Q}$.	16	20	10	24	ns
t_{PLH}	Propagation delay. Clear to Q or $\overline{Q}$.	18	20	15	24	ns
t_{PHL}	Propagation delay. Clear to Q or $\overline{Q}$.	15	20	15	24	ns
t_{PLH}	Propagation delay. Clock to Q or $\overline{Q}$.	17	25	15	25	ns
t_{PHL}	Propagation delay. Clock to Q or $\overline{Q}$.	18	25	15	25	ns

Figure 4: Switching Characteristics

54HSC/T74 : Dual D-Type Flip-Flops with Preset and Clear

Symbol	Parameter	Test Conditions	Limits				Units
			+25°C		-55°C / +125°C		
			Min.	Max.	Min.	Max.	
I_{DD}	Quiescent Current	V_{IN} = 0V or V_{DD}	-	10	-	400	µA
V_{OL}	Output Voltage Low Level	I_{OL} = 9mA	-	0.4	-	0.4	V
V_{OH}	Output Voltage High Level	I_{OH} = -11mA	2.5	-	2.5	-	V
V_{IL1}	Voltage Input Low (CMOS)	-	-	1.5	-	1.5	V
V_{IH1}	Voltage Input High (CMOS)	-	3.5	-	3.5	-	V
V_{IL2}	Voltage Input Low (TTL)	-	-	0.8	-	0.8	V
V_{IH2}	Voltage Input High (TTL)	-	2.0	-	2.0	-	V
I_{IN}	Input Leakage Current	V_{IN} = V_{DD} or V_{SS}	-	±0.5	-	±5.0	µA

Figure 5: DC Characteristics

54HSC/T109 : Dual J-KB Flip-Flops with Preset and Clear

The 54HSC/T109 is a Dual Positive-Edge-Triggered J-KB Flip-Flop with preset and clear.

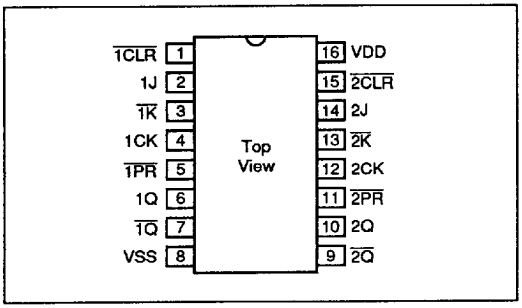


Figure 1: Pin Out

Inputs					Output	
PRESET	CLEAR	CLOCK	J	KB	Q	Q
L	H	X	X	X	H	L
H	L	X	X	X	L	H
L	L	X	X	X	H*	H*
H	H	↑	L	L	L	H
H	H	↑	H	L	Toggle	Toggle
H	H	↑	L	H	Q_0	$\overline{Q}_0$
H	H	↑	H	H	H	L
H	H	L	X	X	Q_0	$\overline{Q}_0$

H = high level, L = low level, X = irrelevant, * = unknown return state

Figure 2: Function Table

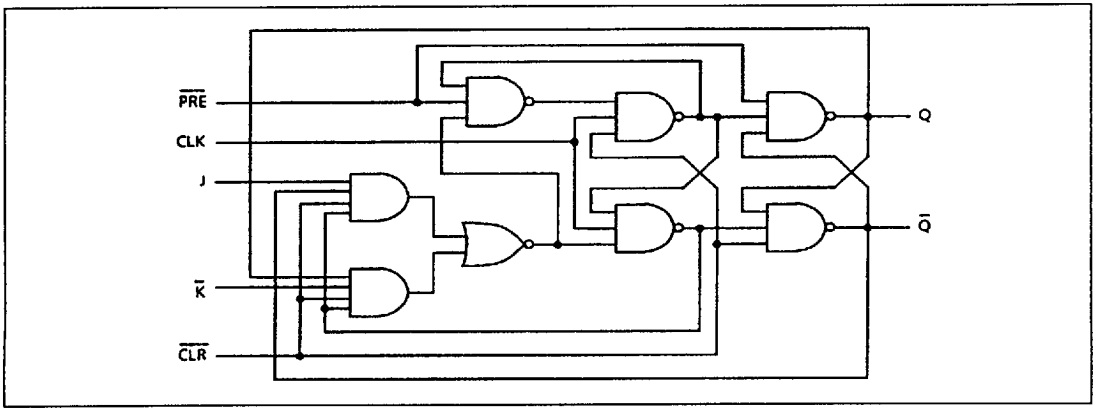


Figure 3: Logic Diagram

Symbol	Parameter	+25°C		-55°C / +125°C		Units
		Typ.	Max.	Typ.	Max.	
t_{PLH}	Propagation delay. Preset to Q or $\overline{Q}$.	15	19	17	19	ns
t_{PHL}	Propagation delay. Preset to Q or $\overline{Q}$.	16	25	19	25	ns
t_{PLH}	Propagation delay. Clear to Q or $\overline{Q}$.	17	25	20	25	ns
t_{PHL}	Propagation delay. Clear to Q or $\overline{Q}$.	15	25	18	25	ns
t_{PLH}	Propagation delay. Clock to Q or $\overline{Q}$.	18	25	21	25	ns
t_{PHL}	Propagation delay. Clock to Q or $\overline{Q}$.	15	25	18	25	ns

Figure 4: Switching Characteristics

54HSC/T109 : Dual J-KB Flip-Flops with Preset and Clear

Symbol	Parameter	Test Conditions	Limits				Units
			+25°C		-55°C / +125°C		
			Min.	Max.	Min.	Max.	
I_{DD}	Quiescent Current	V_{IN} = 0V or V_{DD}	-	20	-	400	µA
V_{OL}	Output Voltage Low Level	I_{OL} = 9mA	-	0.4	-	0.4	V
V_{OH}	Output Voltage High Level	I_{OH} = -11mA	2.5	-	2.5	-	V
V_{IL1}	Voltage Input Low (CMOS)	-	-	1.5	-	1.5	V
V_{IH1}	Voltage Input High (CMOS)	-	3.5	-	3.5	-	V
V_{IL2}	Voltage Input Low (TTL)	-	-	0.8	-	0.8	V
V_{IH2}	Voltage Input High (TTL)	-	2.0	-	2.0	-	V
I_{IN}	Input Leakage Current	V_{IN} = V_{DD} or V_{SS}	-	±0.5	-	±5.0	µA

Figure 5: DC Characteristics

54HSC/T273 : Octal D-Type Flip-Flops

The 54HSC/T273 is an Octal D-Type Flip-Flop with a direct active low clear. The D-Inputs are transferred to the Q-Outputs on the positive going edge of the clock pulse.

Inputs			Outputs
$\overline{CLEAR}$	CLOCK	D	Q
L	X	X	L
H	L-H	H	H
H	L-H	L	L
H	L	X	Q_0

Q_0 = level of Q before inputs were established
H = high level, L = low level, X = irrelevant

Figure 1: Function Table

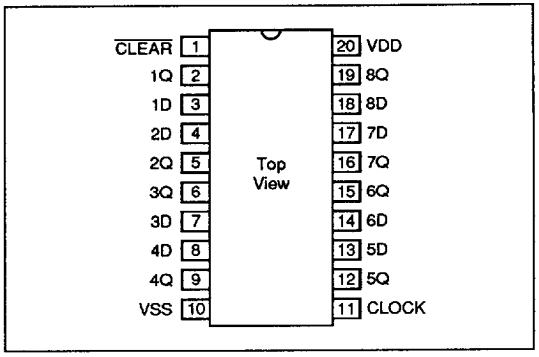


Figure 2: Pin Out

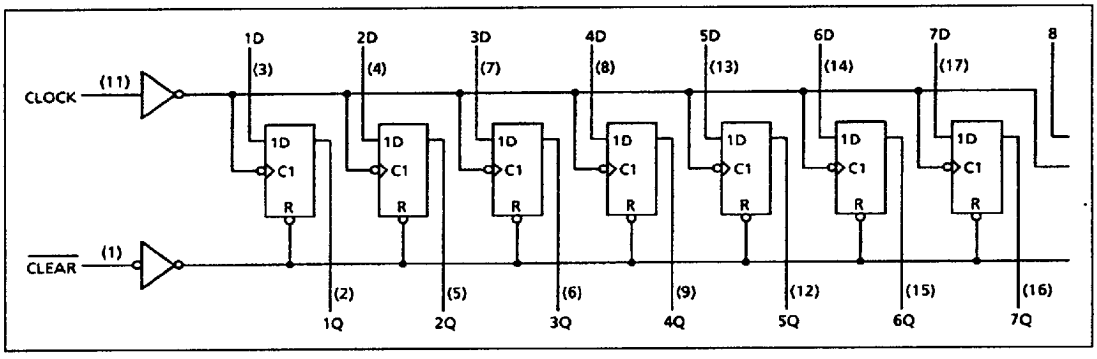


Figure 3: Logic Diagram

Symbol	Parameter	+25°C		-55°C / +125°C		Units
		Typ.	Max.	Typ.	Max.	
t_{PLH}	Propagation delay. Clear to Q or $\overline{Q}$.	14	25	17	28	ns
t_{PHL}	Propagation delay. Clear to Q or $\overline{Q}$.	16	25	19	28	ns
t_{PLH}	Propagation delay. Clock to Q or $\overline{Q}$.	15	25	18	28	ns
t_{PHL}	Propagation delay. Clock to Q or $\overline{Q}$.	17	25	20	28	ns

Figure 4: Switching Characteristics

54HSC/T273 : Octal D-Type Flip-Flops

Symbol	Parameter	Test Conditions	Limits				Units
			+25°C		-55°C / +125°C		
			Min.	Max.	Min.	Max.	
I_{DD}	Quiescent Current	V_{IN} = 0V or V_{DD}	-	20	-	600	µA
V_{OL}	Output Voltage Low Level	I_{OL} = 9mA	-	0.4	-	0.4	V
V_{OH}	Output Voltage High Level	I_{OH} = -11mA	2.5	-	2.5	-	V
V_{IL1}	Voltage Input Low (CMOS)	-	-	1.5	-	1.5	V
V_{IH1}	Voltage Input High (CMOS)	-	3.5	-	3.5	-	V
V_{IL2}	Voltage Input Low (TTL)	-	-	0.8	-	0.8	V
V_{IH2}	Voltage Input High (TTL)	-	2.0	-	2.0	-	V
I_{IN}	Input Leakage Current	V_{IN} = V_{DD} or V_{SS}	-	±0.5	-	±5.0	µA

Figure 5: DC Characteristics

54HSC/T374 : Octal D-Type Edge-Triggered Flip-Flops

The 54HSC/T374 consists of 8 Positive-Edge Triggered D-Type Flip-Flops with tri-state output.

Inputs			Outputs
$\overline{OC}$	CLOCK	D	Q
L	↑	H	H
L	↑	L	L
L	L	X	Q_0
H	X	X	Z

H = high level, L = low level, X = irrelevant, Z = high impedance

Figure 1: Function Table

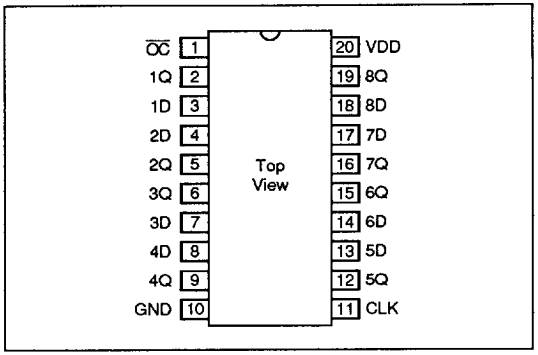


Figure 2: Pin Out

Symbol	Parameter	+25°C			-55°C / +125°C			Units
		Min.	Typ.	Max.	Min.	Typ.	Max.	
t_{PLH}	Propagation delay. Low to high output.	-	14	22	-	17	25	ns
t_{PHL}	Propagation delay. High to low output.	-	15	22	-	16	25	ns
t_{PZL}	Propagation delay. Enable to low.	-	13	20	-	16	25	ns
t_{PZH}	Propagation delay. Enable to high.	-	16	20	-	18	23	ns
t_{PLZ}	Propagation delay. Disable from low.	-	14	20	-	16	22	ns
t_{PHZ}	Propagation delay. Disable from high.	-	13	18	-	15	20	ns

Figure 3: Switching Characteristics

Symbol	Parameter	Test Conditions	Limits				Units
			+25°C		-55°C / +125°C		
			Min.	Max.	Min.	Max.	
I_{DD}	Quiescent Current	V_{IN} = 0V or V_{DD}	-	20	-	600	µA
V_{OL}	Output Voltage Low Level	I_{OL} = 9mA	-	0.4	-	0.4	V
V_{OH}	Output Voltage High Level	I_{OH} = -11mA	2.5	-	2.5	-	V
V_{IL1}	Voltage Input Low (CMOS)	-	-	1.5	-	1.5	V
V_{IH1}	Voltage Input High (CMOS)	-	3.5	-	3.5	-	V
V_{IL2}	Voltage Input Low (TTL)	-	-	0.8	-	0.8	V
V_{IH2}	Voltage Input High (TTL)	-	2.0	-	2.0	-	V
I_{OZ}	Tri-State Leakage	V_O = 0V or V_{DD}	-	±1	-	±50	µA
I_{IN}	Input Leakage Current	V_{IN} = V_{DD} or V_{SS}	-	±0.5	-	±5.0	µA

Figure 4: DC Characteristics

54HSC/T374 : Octal D-Type Edge-Triggered Flip-Flops

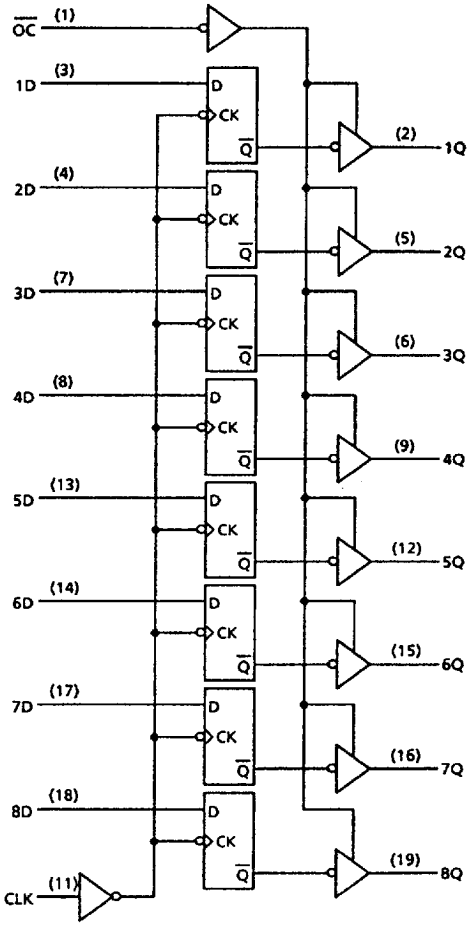


Figure 5: Logic Diagram

54HSC/T574 : Octal D-Type Edge-Triggered Flip-Flops

The 54HSC/T574 consists of 8 Positive-Edge Triggered D-Type Flip-Flops with tri-state output.

Inputs			Outputs
$\overline{OC}$	CLOCK	D	Q
L	↑	H	H
L	↑	L	L
L	L	X	Q_0
H	X	X	Z

H = high level, L = low level, X = irrelevant, Z = high impedance

Figure 1: Function Table

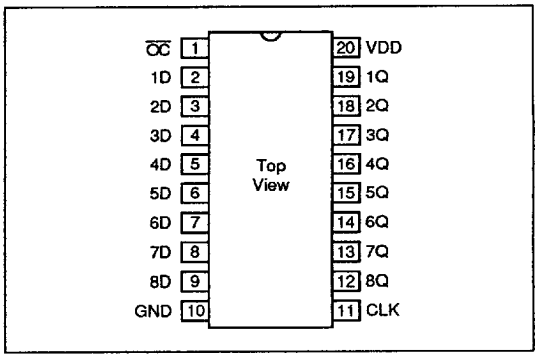


Figure 2: Pin Out

Symbol	Parameter	+25°C			-55°C / +125°C			Units
		Min.	Typ.	Max.	Min.	Typ.	Max.	
t_{PLH}	Propagation delay. Low to high output.	-	16	25	-	19	28	ns
t_{PHL}	Propagation delay. High to low output.	-	19	27	-	22	30	ns
t_{PZL}	Propagation delay. Enable to low.	-	13	21	-	16	24	ns
t_{PZH}	Propagation delay. Enable to high.	-	16	24	-	19	27	ns
t_{PLZ}	Propagation delay. Disable from low.	-	14	22	-	17	25	ns
t_{PHZ}	Propagation delay. Disable from high.	-	13	21	-	16	24	ns

Figure 3: Switching Characteristics

Symbol	Parameter	Test Conditions	Limits				Units
			+25°C		-55°C / +125°C		
			Min.	Max.	Min.	Max.	
I_{DD}	Quiescent Current	V_{IN} = 0V or V_{DD}	-	20	-	600	µA
V_{OL}	Output Voltage Low Level	I_{OL} = 9mA	-	0.4	-	0.4	V
V_{OH}	Output Voltage High Level	I_{OH} = -11mA	2.5	-	2.5	-	V
V_{IL1}	Voltage Input Low (CMOS)	-	-	1.5	-	1.5	V
V_{IH1}	Voltage Input High (CMOS)	-	3.5	-	3.5	-	V
V_{IL2}	Voltage Input Low (TTL)	-	-	0.8	-	0.8	V
V_{IH2}	Voltage Input High (TTL)	-	2.0	-	2.0	-	V
I_{OZ}	Tri-State Leakage	V_O = 0V or V_{DD}	-	±1	-	±50	µA
I_{IN}	Input Leakage Current	V_{IN} = V_{DD} or V_{SS}	-	±0.5	-	±5.0	µA

Figure 4: DC Characteristics

54HSC/T574 : Octal D-Type Edge-Triggered Flip-Flops

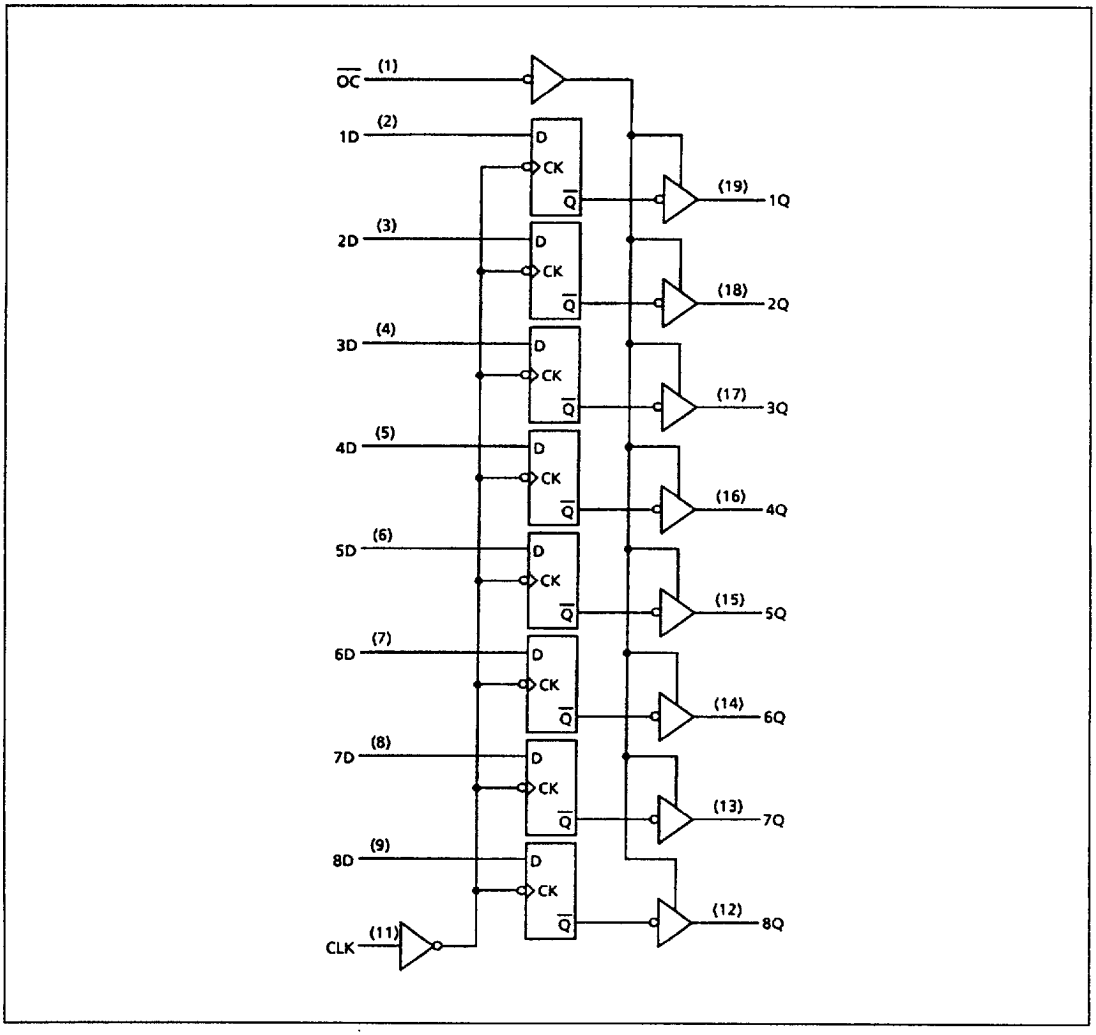


Figure 5: Logic Diagram

54HSC/T283 : 4-Bit Binary Full Adders with Fast Carry

The 54HSC/T283 are 4-Bit Binary Full Adders with fast carry.

Input				Output					
				When CO=L / When C2=L			When CO=H / When C2=H		
A1/A3	B1/B3	A2/A4	B2/B4	Σ1/Σ3	Σ2/Σ4	C2/C4	Σ1/Σ3	Σ2/Σ4	C2/C4
L	L	L	L	L	L	L	H	L	L
H	L	L	L	H	L	L	L	H	L
L	H	L	L	H	L	L	L	H	L
H	H	L	L	L	H	L	H	H	L
L	L	H	L	L	H	L	H	H	L
H	L	H	L	H	H	L	L	L	H
L	H	H	L	H	H	L	L	L	H
H	H	H	L	L	L	H	H	L	H
L	L	L	H	L	H	L	H	H	L
H	L	L	H	H	H	L	L	L	H
L	H	L	H	H	H	L	L	L	H
H	H	L	H	L	L	H	H	L	H
L	L	H	H	L	L	H	H	L	H
H	L	H	H	H	L	H	L	H	H
L	H	H	H	H	L	H	L	H	H
H	H	H	H	L	H	H	H	H	H

H = high level, L = low level

Figure 1: Function Table

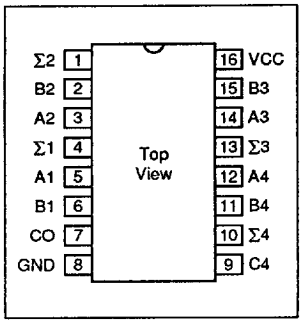


Figure 2: Pin Out

Symbol	Parameter	+25°C		-55°C / +125°C		Units
		Typ.	Max.	Typ.	Max.	
t_{PLH}	Propagation delay. C0 to any Σ.	13	25	16	28	ns
t_{PHL}	Propagation delay. C0 to any Σ.	12	25	15	28	ns
t_{PLH}	Propagation delay. Ai or Bi to Σi.	14	25	17	28	ns
t_{PHL}	Propagation delay. Ai or Bi to Σi.	12	25	15	28	ns
t_{PLH}	Propagation delay. C0 to C4.	11	25	14	28	ns
t_{PHL}	Propagation delay. C0 to C4.	16	25	19	28	ns
t_{PLH}	Propagation delay. Ai or Bi to C4.	15	25	19	28	ns
t_{PHL}	Propagation delay. Ai or Bi to C4.	14	25	17	28	ns

Figure 3: Switching Characteristics

54HSC/T283 : 4-Bit Binary Full Adders with Fast Carry

Symbol	Parameter	Test Conditions	Limits				Units
			+25°C		-55°C / +125°C		
			Min.	Max.	Min.	Max.	
I_{DD}	Quiescent Current	V_{IN} = 0V or V_{DD}	-	20	-	600	µA
V_{OL}	Output Voltage Low Level	I_{OL} = 9mA	-	0.4	-	0.4	V
V_{OH}	Output Voltage High Level	I_{OH} = -11mA	2.5	-	2.5	-	V
V_{IL1}	Voltage Input Low (CMOS)	-	-	1.5	-	1.5	V
V_{IH1}	Voltage Input High (CMOS)	-	3.5	-	3.5	-	V
V_{IL2}	Voltage Input Low (TTL)	-	-	0.8	-	0.8	V
V_{IH2}	Voltage Input High (TTL)	-	2.0	-	2.0	-	V
I_{IN}	Input Leakage Current	V_{IN} = V_{DD} or V_{SS}	-	±0.5	-	±5.0	µA

Figure 4: DC Characteristics

54HSC/T283 : 4-Bit Binary Full Adders with Fast Carry

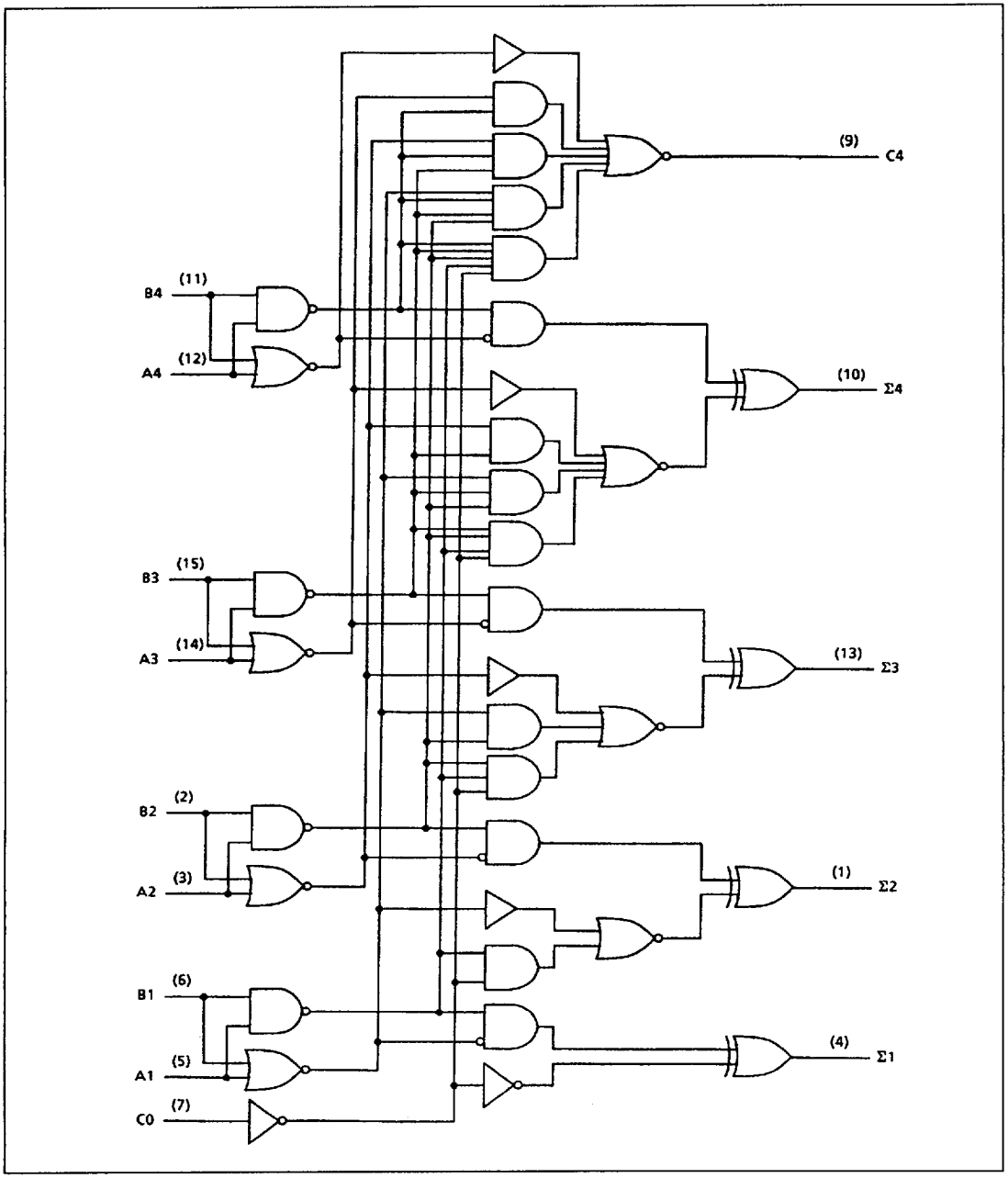


Figure 5: Logic Diagram

54HSC/T161 : 4-Bit Synchronous Binary Counter

The 54HSC/T161 is a Synchronous 4-Bit Binary Counter which features direct clear and an internal carry look-ahead.

Inputs						Output
$\overline{\text{Clear}}$	Enable P	Enable T	A→D	$\overline{\text{Load}}$	Clock	$Q_A \rightarrow Q_D$
L	X	X	X	X	X	0
H	L	X	X	H	X	Inhibit
H	X	L	X	H	X	Inhibit
H	X	X	Q_n	L	↑	Q_n
H	X	X	X	X	L	Q_0
H	X	X	X	X	H	Q_0
H	H	H	X	H	↑	Count

CARRY = H when $Q_A \rightarrow Q_D$ = H, Q_0 = previous level of Q
H = high level, L = low level, X = irrelevant

Figure 1: Function Table

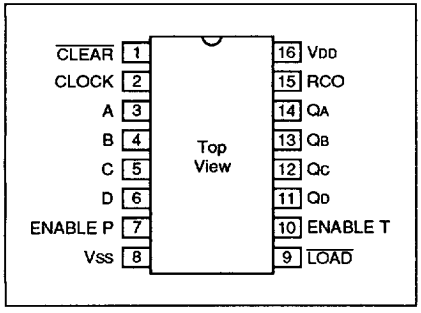


Figure 2: Pin Out

Symbol	From (Input)	To (Output)	+25°C		-55°C / +125°C		Units
			Typ.	Max.	Typ.	Max.	
t_{PLH}	CLOCK	RIPPLE CARRY	20	25	23	28	ns
t_{PHL}	CLOCK	RIPPLE CARRY	19	25	22	28	ns
t_{PLH}	CLOCK (Load Input HIGH)	Any Q Output	16	25	19	28	ns
t_{PHL}	CLOCK (Load Input HIGH)	Any Q Output	15	25	18	28	ns
t_{PLH}	CLOCK (Load Input LOW)	Any Q Output	15	25	18	28	ns
t_{PHL}	CLOCK (Load Input LOW)	Any Q Output	15	25	18	28	ns
t_{PLH}	ENABLE	RIPPLE CARRY	14	25	17	28	ns
t_{PHL}	ENABLE	RIPPLE CARRY	14	25	17	28	ns
t_{PHL}	CLEAR	Any Q Output	18	25	21	28	ns

Figure 3: Switching Characteristics

54HSC/T161 : 4-Bit Synchronous Binary Counter

Symbol	Parameter	Test Conditions	Limits				Units
			+25°C		-55°C / +125°C		
			Min.	Max.	Min.	Max.	
I_{DD}	Quiescent Current	V_{IN} = 0V or V_{DD}	-	20	-	400	µA
V_{OL}	Output Voltage Low Level	I_{OL} = 9mA	-	0.4	-	0.4	V
V_{OH}	Output Voltage High Level	I_{OH} = -11mA	2.5	-	2.5	-	V
V_{IL1}	Voltage Input Low (CMOS)	-	-	1.5	-	1.5	V
V_{IH1}	Voltage Input High (CMOS)	-	3.5	-	3.5	-	V
V_{IL2}	Voltage Input Low (TTL)	-	-	0.8	-	0.8	V
V_{IH2}	Voltage Input High (TTL)	-	2.0	-	2.0	-	V
I_{IN}	Input Leakage Current	V_{IN} = V_{DD} or V_{SS}	-	±0.5	-	±5.0	µA

Figure 4: DC Characteristics

54HSC/T161 : 4-Bit Synchronous Binary Counter

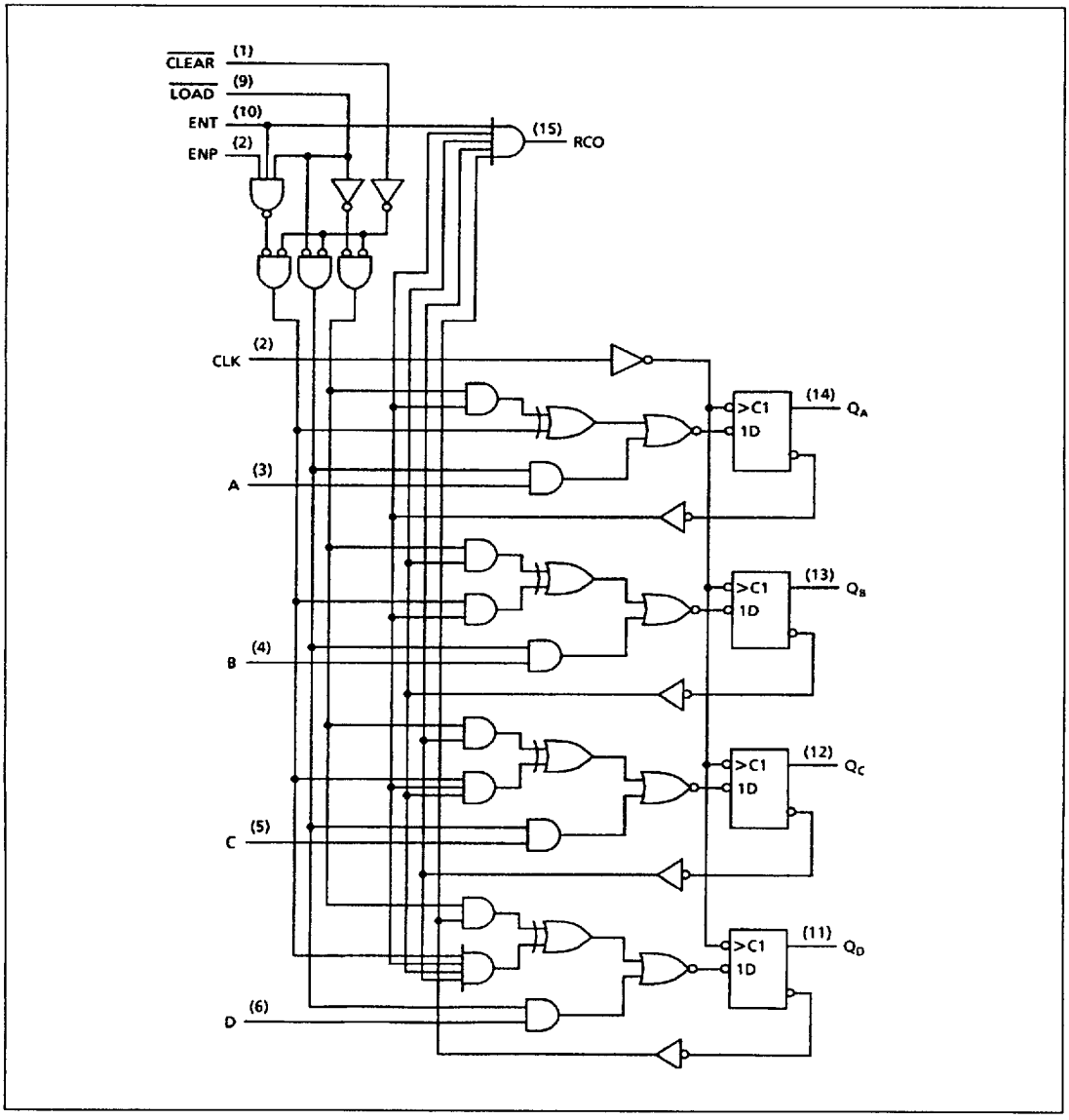


Figure 5: Logic Diagram

54HSC/T163 : Synchronous 4-Bit Counter

The 54HSC/T163 is a 4-Bit Counter with synchronous clear.

Inputs						Output
$\overline{Clear}$	Enable P	Enable T	A→D	$\overline{Load}$	Clock	$Q_A \rightarrow Q_D$
L	X	X	X	X	X	0
H	L	X	X	H	X	Inhibit
H	X	L	X	H	X	Inhibit
H	X	X	Q_n	L	↑	Q_n
H	X	X	X	X	L	Q_0
H	X	X	X	X	H	Q_0
H	H	H	X	H	↑	Count

CARRY = H when $Q_A \rightarrow Q_D$ = H, Q_0 = previous level of Q
H = high level, L = low level, X = irrelevant

Figure 1: Function Table

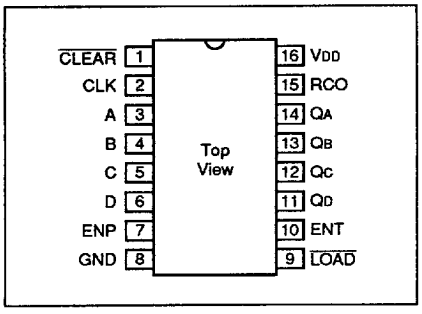


Figure 2: Pin Out

Symbol	Parameter	+25°C		-55°C / +125°C		Units
		Typ.	Max.	Typ.	Max.	
t_{PLH}	Propagation delay Clock to RCO	12	20	15	22	ns
t_{PHL}	Propagation delay Clock to RCO	14	20	17	22	ns
t_{PLH}	Propagation delay Clock to any Q	15	20	18	22	ns
t_{PHL}	Propagation delay Clock to any Q	13	20	16	22	ns
t_{PLH}	Propagation delay ENT to RCO	9	15	12	17	ns
t_{PHL}	Propagation delay ENT to RCO	10	15	13	17	ns

Figure 3: Switching Characteristics

54HSC/T163 : Synchronous 4-Bit Counter

Symbol	Parameter	Test Conditions	Limits				Units
			+25°C		-55°C / +125°C		
			Min.	Max.	Min.	Max.	
I_{DD}	Quiescent Current	V_{IN} = 0V or V_{DD}	-	20	-	400	µA
V_{OL}	Output Voltage Low Level	I_{OL} = 9mA	-	0.4	-	0.4	V
V_{OH}	Output Voltage High Level	I_{OH} = -11mA	2.5	-	2.5	-	V
V_{IL1}	Voltage Input Low (CMOS)	-	-	1.5	-	1.5	V
V_{IH1}	Voltage Input High (CMOS)	-	3.5	-	3.5	-	V
V_{IL2}	Voltage Input Low (TTL)	-	-	0.8	-	0.8	V
V_{IH2}	Voltage Input High (TTL)	-	2.0	-	2.0	-	V
I_{IN}	Input Leakage Current	V_{IN} = V_{DD} or V_{SS}	-	±0.5	-	±5.0	µA

Figure 4: DC Characteristics

54HSC/T163 : Synchronous 4-Bit Counter

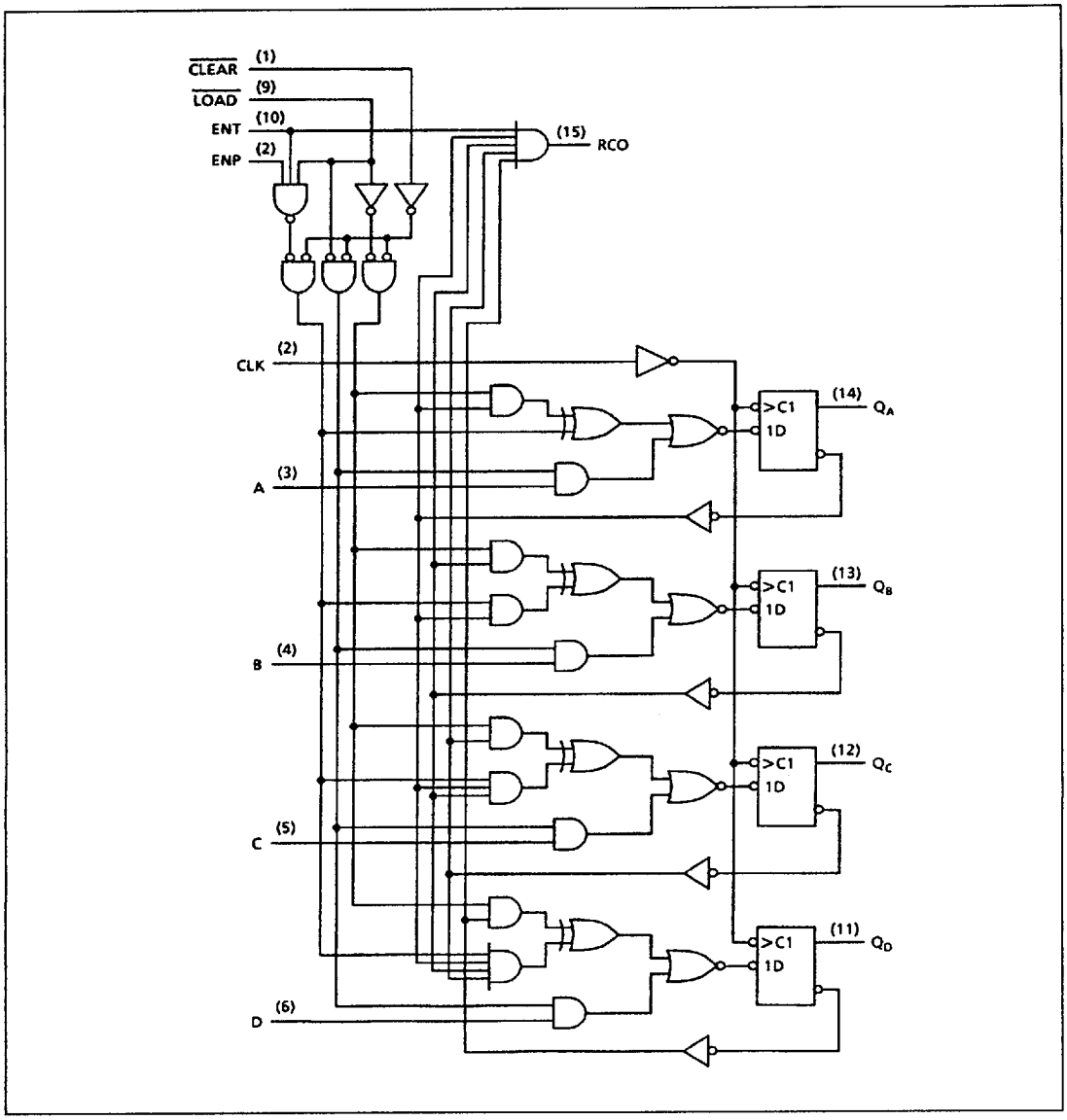


Figure 5: Logic Diagram

54HSC/T191 : Synchronous 4-Bit Counter

The 54HSC/T191 is a 4-Bit Synchronous Counter with presettable up/down and asynchronous reset.

Inputs				Function
$\overline{PL}$	$\overline{CE}$	$\overline{U}$/D	CP	
H	L	L	↑	Count Up
H	L	H	↑	Count Down
L	X	X	X	Asyn. Preset
H	H	X	X	No Change

H = high level, L = low level, X = irrelevant, ↑ = low-to-high clock (CP) transition.
Note: $\overline{U}$/D or $\overline{CE}$ should be changed only when clock (CP) is high.

Figure 1: Function Table

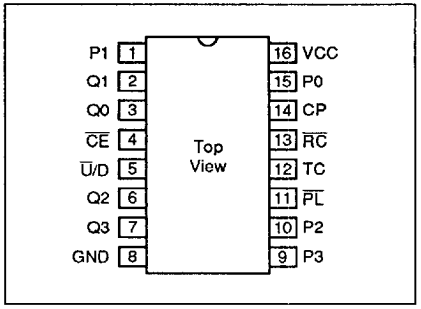


Figure 2: Pin Out

Symbol	Parameter	+25°C		-55°C / +125°C		Units
		Typ.	Max.	Typ.	Max.	
t_{PLH}	Propagation delay $\overline{PL}$ to Qn	-	29	-	33	ns
t_{PHL}	Propagation delay $\overline{PL}$ to Qn	-	32	-	36	ns
t_{PLH}	Propagation delay Pn to Qn	-	27	-	31	ns
t_{PHL}	Propagation delay Pn to Qn	-	30	-	34	ns
t_{PLH}	Propagation delay CP to Qn	-	26	-	30	ns
t_{PHL}	Propagation delay CP to Qn	-	29	-	33	ns
t_{PLH}	Propagation delay CP to $\overline{RC}$	-	20	-	23	ns
t_{PHL}	Propagation delay CP to $\overline{RC}$	-	32	-	34	ns
t_{PLH}	Propagation delay CP to TC	-	29	-	33	ns
t_{PHL}	Propagation delay CP to TC	-	32	-	36	ns
t_{PLH}	Propagation delay $\overline{U}$/D to $\overline{RC}$	-	27	-	31	ns
t_{PHL}	Propagation delay $\overline{U}$/D to $\overline{RC}$	-	30	-	34	ns
t_{PLH}	Propagation delay $\overline{U}$/D to TC	-	26	-	30	ns
t_{PHL}	Propagation delay $\overline{U}$/D to TC	-	29	-	33	ns
t_{PLH}	Propagation delay $\overline{CE}$ to $\overline{RC}$	-	22	-	25	ns
t_{PHL}	Propagation delay $\overline{CE}$ to $\overline{RC}$	-	35	-	38	ns

Figure 3: Switching Characteristics

54HSC/T191 : Synchronous 4-Bit Counter

Symbol	Parameter	Test Conditions	Limits				Units
			+25°C		-55°C / +125°C		
			Min.	Max.	Min.	Max.	
I_{DD}	Quiescent Current	V_{IN} = 0V or V_{DD}	-	20	-	600	µA
V_{OL}	Output Voltage Low Level	I_{OL} = 9mA	-	0.4	-	0.4	V
V_{OH}	Output Voltage High Level	I_{OH} = -11mA	2.5	-	2.5	-	V
V_{IL1}	Voltage Input Low (CMOS)	-	-	1.5	-	1.5	V
V_{IH1}	Voltage Input High (CMOS)	-	3.5	-	3.5	-	V
V_{IL2}	Voltage Input Low (TTL)	-	-	0.8	-	0.8	V
V_{IH2}	Voltage Input High (TTL)	-	2.0	-	2.0	-	V
I_{IN}	Input Leakage Current	V_{IN} = V_{DD} or V_{SS}	-	±0.5	-	±5.0	µA

Figure 4: DC Characteristics

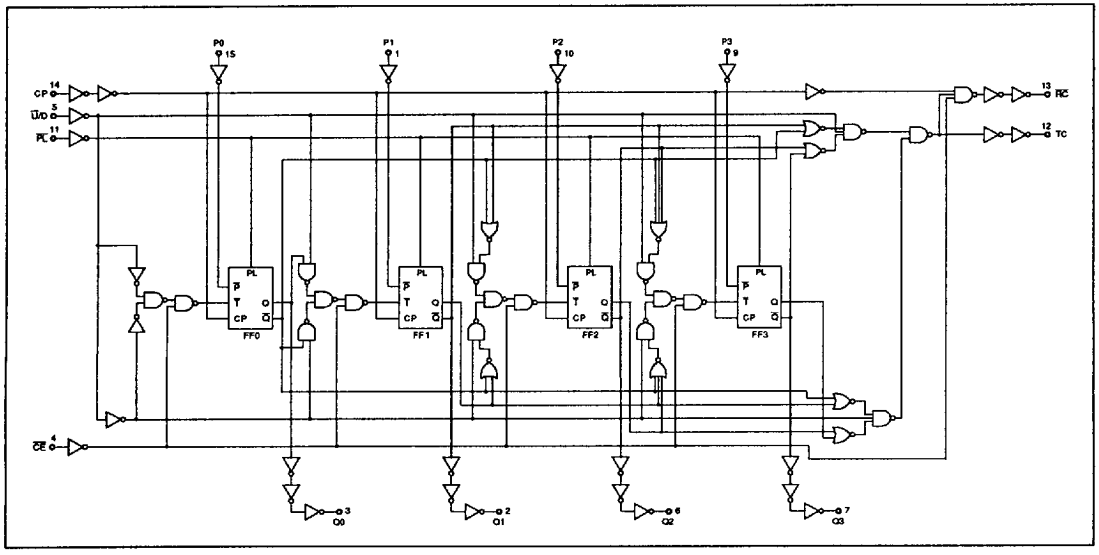


Figure 5: Logic Diagram

54HSC/T138 : 3-Line to 8-Line Decoder/Multiplexer

The 54HSC/T138 is a 3-Line to 8-Line Decoder/Multiplexer, with inverted outputs.

Enable Inputs			Select Inputs			Outputs							
G1	$\overline{G}$2A	$\overline{G}$2B	C	B	A	Y0	Y1	Y2	Y3	Y4	Y5	Y6	Y7
X	H	X	X	X	X	H	H	H	H	H	H	H	H
X	X	H	X	X	X	H	H	H	H	H	H	H	H
L	X	X	X	X	X	H	H	H	H	H	H	H	H
H	L	L	L	L	L	L	H	H	H	H	H	H	H
H	L	L	L	L	H	H	L	H	H	H	H	H	H
H	L	L	L	H	L	H	H	L	H	H	H	H	H
H	L	L	L	H	H	H	H	H	L	H	H	H	H
H	L	L	H	L	L	H	H	H	H	L	H	H	H
H	L	L	H	L	H	H	H	H	H	H	L	H	H
H	L	L	H	H	L	H	H	H	H	H	H	L	H
H	L	L	H	H	H	H	H	H	H	H	H	H	L

H = high level, L = low level, X = irrelevant

Figure 1: Function Table

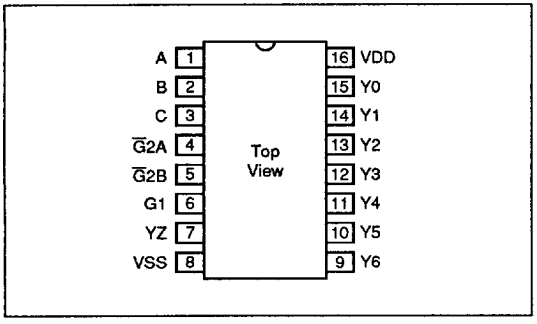


Figure 2: Pin Out

Symbol	Parameter	+25°C		-55°C / +125°C		Units
		Typ.	Max.	Typ.	Max.	
t_{PLH}	Propagation delay. Address to Output.	17	25	20	28	ns
t_{PHL}	Propagation delay. Address to Output.	19	25	22	28	ns
t_{PLH}	Propagation delay. G to Output.	21	25	24	28	ns
t_{PHL}	Propagation delay. G to Output.	21	25	24	28	ns

Figure 3: Switching Characteristics

54HSC/T138 : 3-Line to 8-Line Decoder/Multiplexer

Symbol	Parameter	Test Conditions	Limits				Units
			+25°C		-55°C / +125°C		
			Min.	Max.	Min.	Max.	
I_{DD}	Quiescent Current	V_{IN} = 0V or V_{DD}	-	10	-	400	µA
V_{OL}	Output Voltage Low Level	I_{OL} = 9mA	-	0.4	-	0.4	V
V_{OH}	Output Voltage High Level	I_{OH} = -11mA	2.5	-	2.5	-	V
V_{IL1}	Voltage Input Low (CMOS)	-	-	1.5	-	1.5	V
V_{IH1}	Voltage Input High (CMOS)	-	3.5	-	3.5	-	V
V_{IL2}	Voltage Input Low (TTL)	-	-	0.8	-	0.8	V
V_{IH2}	Voltage Input High (TTL)	-	2.0	-	2.0	-	V
I_{IN}	Input Leakage Current	V_{IN} = V_{DD} or V_{SS}	-	±0.5	-	±5.0	µA

Figure 4: DC Characteristics

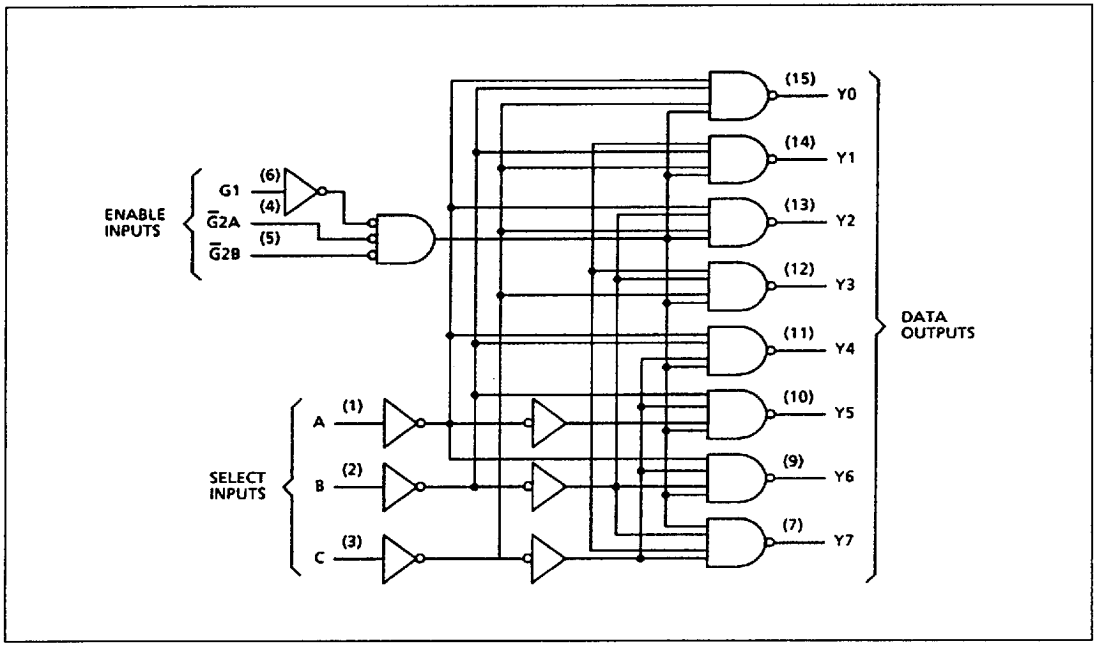


Figure 5: Logic Diagram

54HSC/T139 : Dual 2 to 4 Decoders/Multiplexers

The 54HSC/T139 consists of Two Independent 2 to 4 Line Decoder/Multiplexers.

Inputs			Output			
Enable	Select					
$\overline{G}$	B	A	Y0	Y1	Y2	Y3
H	X	X	H	H	H	H
L	L	L	L	H	H	H
L	L	H	H	L	H	H
L	H	L	H	H	L	H
L	H	H	H	H	H	L

H = high level, L = low level, X = irrelevant

Figure 1: Function Table

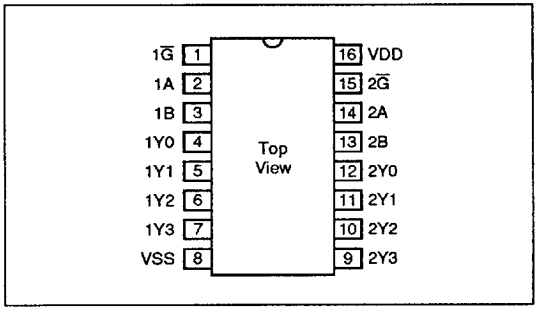


Figure 2: Pin Out

Symbol	Parameter	+25°C		-55°C / +125°C		Units
		Typ.	Max.	Typ.	Max.	
t_{PLH}	Propagation delay. Address to Output.	16	28	22	34	ns
t_{PHL}	Propagation delay. Address to Output.	17	28	20	34	ns
t_{PLH}	Propagation delay. G to Output.	16	22	19	25	ns
t_{PHL}	Propagation delay. G to Output.	17	22	20	25	ns

Figure 3: Switching Characteristics

54HSC/T139 : Dual 2 to 4 Decoders/Multiplexers

Symbol	Parameter	Test Conditions	Limits				Units
			+25°C		-55°C / +125°C		
			Min.	Max.	Min.	Max.	
I_{DD}	Quiescent Current	V_{IN} = 0V or V_{DD}	-	10	-	400	µA
V_{OL}	Output Voltage Low Level	I_{OL} = 9mA	-	0.4	-	0.4	V
V_{OH}	Output Voltage High Level	I_{OH} = -11mA	2.5	-	2.5	-	V
V_{IL1}	Voltage Input Low (CMOS)	-	-	1.5	-	1.5	V
V_{IH1}	Voltage Input High (CMOS)	-	3.5	-	3.5	-	V
V_{IL2}	Voltage Input Low (TTL)	-	-	0.8	-	0.8	V
V_{IH2}	Voltage Input High (TTL)	-	2.0	-	2.0	-	V
I_{IN}	Input Leakage Current	V_{IN} = V_{DD} or V_{SS}	-	±0.5	-	±5.0	µA

Figure 4: DC Characteristics

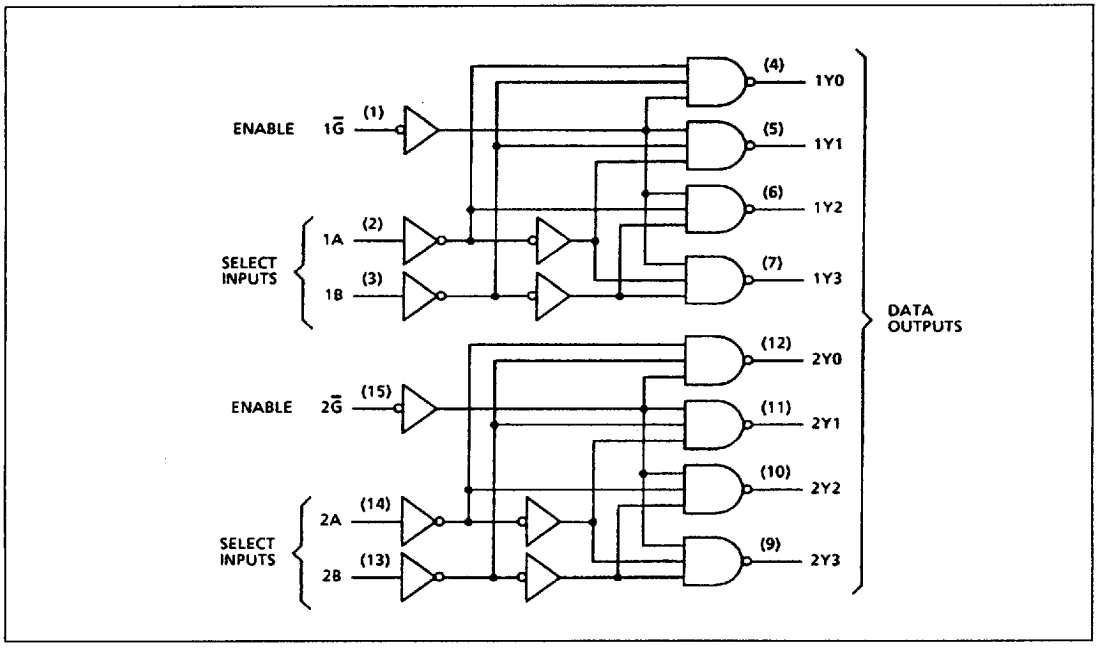


Figure 5: Logic Diagram

54HSC/T148 : 8-Line to 3-Line Octal Priority Encoders

The 54HSC/T148 is an 8 to 3 Line Priority Encoder. Data inputs and outputs are active at the low logic level. Data is accepted on the eight priority inputs (I0-I7). The binary code, corresponding to the highest priority input which is low, is generated on the address outputs (A0-A2) if the enable input is high. The group select (GS) is low when one or more priority inputs and the enable input (EI) are low. The enable output (EO) is low when all priority inputs are high and the enable is low. When the enable input is high all outputs are high.

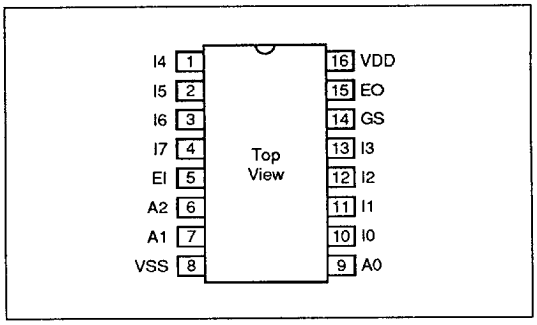


Figure 1: Pin Out

Inputs									Outputs				
EI	I0	I1	I2	I3	I4	I5	I6	I7	A2	A1	A0	GS	EO
H	X	X	X	X	X	X	X	X	H	H	H	H	H
L	H	H	H	H	H	H	H	H	H	H	H	H	L
L	X	X	X	X	X	X	X	L	L	L	L	L	H
L	X	X	X	X	X	X	L	H	L	L	H	L	H
L	X	X	X	X	X	L	H	H	L	H	L	L	H
L	X	X	X	X	L	H	H	H	L	H	H	L	H
L	X	X	X	L	H	H	H	H	H	L	L	L	H
L	X	X	L	H	H	H	H	H	H	L	H	L	H
L	X	L	H	H	H	H	H	H	H	H	L	L	H
L	L	H	H	H	H	H	H	H	H	H	H	L	H

H = high level, L = low level, X = irrelevant

Figure 2: Function Table

Symbol	Parameter	+25°C		-55°C / +125°C		Units
		Typ.	Max.	Typ.	Max.	
t_{PLH}	Propagation delay EI to A	14	22	17	28	ns
t_{PHL}	Propagation delay EI to A	15	22	18	28	ns
t_{PLH}	Propagation delay EI to GS	15	22	18	28	ns
t_{PHL}	Propagation delay EI to GS	15	22	18	28	ns
t_{PLH}	Propagation delay EI to EO	14	22	17	28	ns
t_{PHL}	Propagation delay EI to EO	15	22	18	28	ns
t_{PLH}	Propagation delay I to A	12	22	15	28	ns
t_{PHL}	Propagation delay I to A	14	22	17	28	ns

Figure 3: Switching Characteristics

54HSC/T148 : 8-Line to 3-Line Octal Priority Encoders

Symbol	Parameter	Test Conditions	Limits				Units
			+25°C		-55°C / +125°C		
			Min.	Max.	Min.	Max.	
I_{DD}	Quiescent Current	V_{IN} = 0V or V_{DD}	-	20	-	400	µA
V_{OL}	Output Voltage Low Level	I_{OL} = 9mA	-	0.4	-	0.4	V
V_{OH}	Output Voltage High Level	I_{OH} = -11mA	2.5	-	2.5	-	V
V_{IL1}	Voltage Input Low (CMOS)	-	-	1.5	-	1.5	V
V_{IH1}	Voltage Input High (CMOS)	-	3.5	-	3.5	-	V
V_{IL2}	Voltage Input Low (TTL)	-	-	0.8	-	0.8	V
V_{IH2}	Voltage Input High (TTL)	-	2.0	-	2.0	-	V
I_{IN}	Input Leakage Current	V_{IN} = V_{DD} or V_{SS}	-	±0.5	-	±5.0	µA

Figure 4: DC Characteristics

54HSC/T148 : 8-Line to 3-Line Octal Priority Encoders

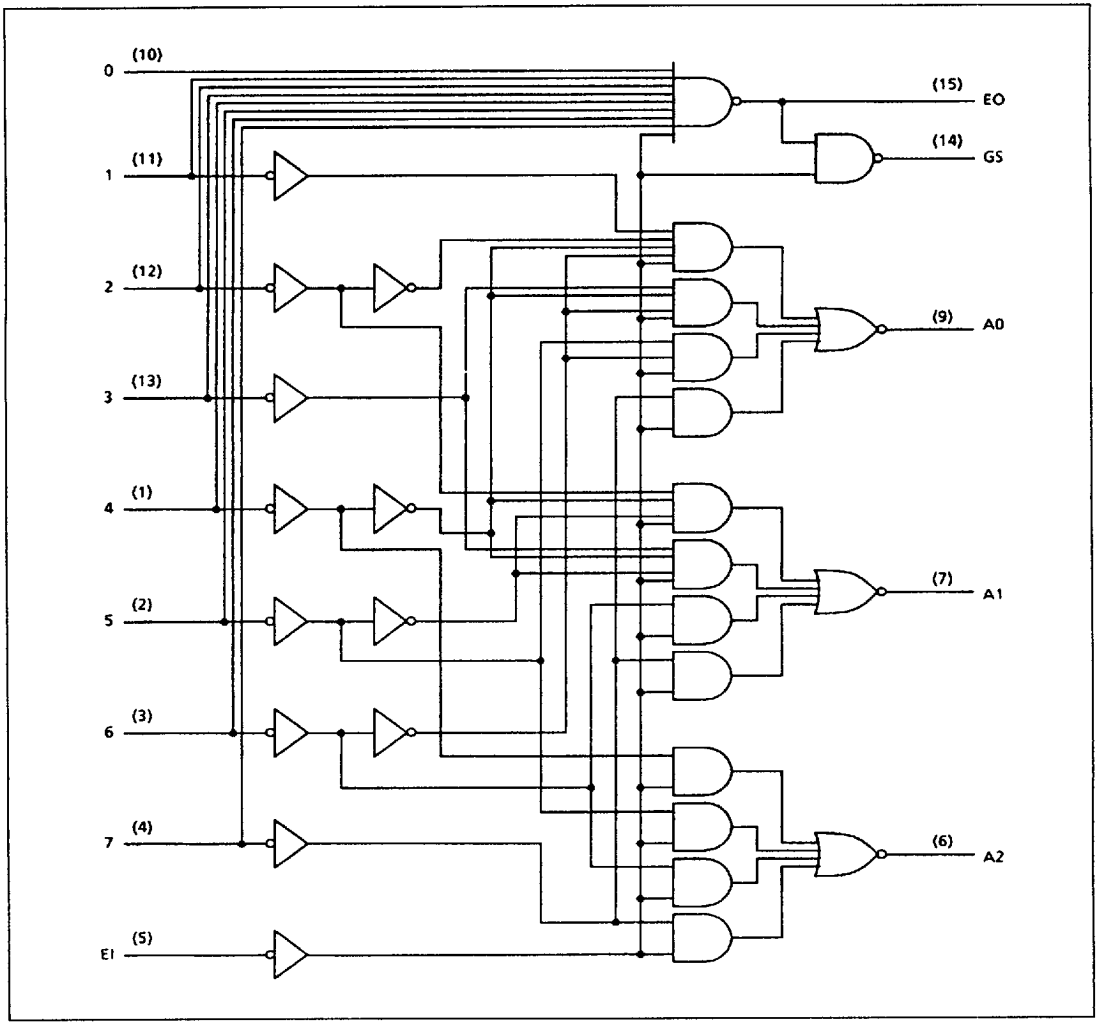


Figure 5: Logic Diagram

54HSC/T151 : 1 of 8 Data Selectors/Multiplexers

The 54HSC/T151 is a 1 of 8 Data Selector. When the strobe input is low the device is enabled. When high this forces the W-output high and the Y-output low.

Inputs				Output	
Select			Strobe		
C	B	A	$\overline{STR}$	Y	W
X	X	X	H	L	H
L	L	L	L	D_0	$\overline{D}_0$
L	L	H	L	D_1	$\overline{D}_1$
L	H	L	L	D_2	$\overline{D}_2$
L	H	H	L	D_3	$\overline{D}_3$
H	L	L	L	D_4	$\overline{D}_4$
H	L	H	L	D_5	$\overline{D}_5$
H	H	L	L	D_6	$\overline{D}_6$
H	H	H	L	D_7	$\overline{D}_7$

H = high level, L = low level, X = irrelevant

Figure 1: Function Table

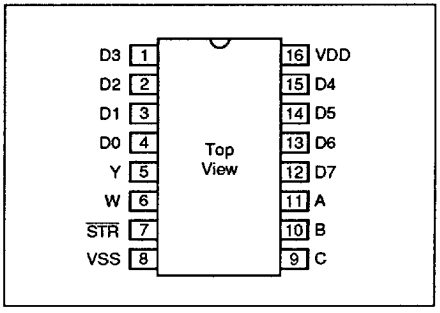


Figure 2: Pin Out

Symbol	Parameter	+25°C		-55°C / +125°C		Units
		Typ.	Max.	Typ.	Max.	
t_{PLH}	Propagation delay A B or C to Y	15	22	18	25	ns
t_{PHL}	Propagation delay A B or C to Y	16	22	19	25	ns
t_{PLH}	Propagation delay A B or C to W	14	22	17	25	ns
t_{PHL}	Propagation delay A B or C to W	15	22	18	25	ns
t_{PLH}	Propagation delay Strobe to Y	14	22	17	25	ns
t_{PHL}	Propagation delay Strobe to Y	16	22	19	25	ns
t_{PLH}	Propagation delay Strobe to W	14	22	17	25	ns
t_{PHL}	Propagation delay Strobe to W	15	22	18	25	ns
t_{PLH}	Propagation delay D_0-D_7 to Y	12	22	15	25	ns
t_{PHL}	Propagation delay D_0-D_7 to Y	14	22	17	25	ns
t_{PLH}	Propagation delay D_0-D_7 to W	12	22	15	25	ns
t_{PHL}	Propagation delay D_0-D_7 to W	14	22	17	25	ns

Figure 3: Switching Characteristics

54HSC/T151 : 1 of 8 Data Selectors/Multiplexers

Symbol	Parameter	Test Conditions	Limits				Units
			+25°C		-55°C / +125°C		
			Min.	Max.	Min.	Max.	
I_{DD}	Quiescent Current	V_{IN} = 0V or V_{DD}	-	20	-	400	µA
V_{OL}	Output Voltage Low Level	I_{OL} = 9mA	-	0.4	-	0.4	V
V_{OH}	Output Voltage High Level	I_{OH} = -11mA	2.5	-	2.5	-	V
V_{IL1}	Voltage Input Low (CMOS)	-	-	1.5	-	1.5	V
V_{IH1}	Voltage Input High (CMOS)	-	3.5	-	3.5	-	V
V_{IL2}	Voltage Input Low (TTL)	-	-	0.8	-	0.8	V
V_{IH2}	Voltage Input High (TTL)	-	2.0	-	2.0	-	V
I_{IN}	Input Leakage Current	V_{IN} = V_{DD} or V_{SS}	-	±0.5	-	±5.0	µA

Figure 4: DC Characteristics

54HSC/T151 : 1 of 8 Data Selectors/Multiplexers

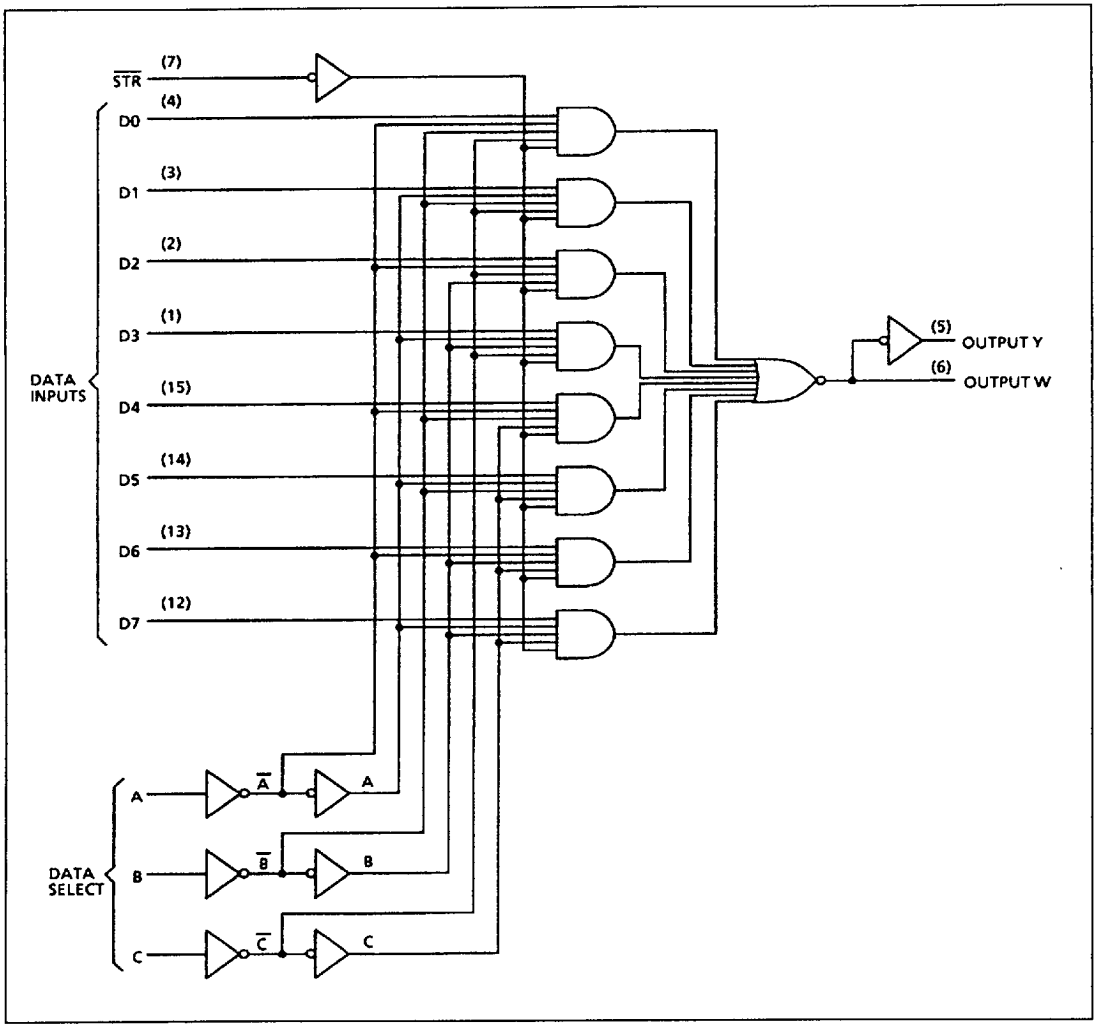


Figure 5: Logic Diagram

54HSC/T154 : 4 to 16 Line Decoders/Demultiplexers

The 54HSC/T154 consists of a 4 to 16 Line Decoder/Demultiplexer.

Inputs						Outputs															
$\overline{G1}$	$\overline{G2}$	D	C	B	A	0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15
L	L	L	L	L	L	L	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H
L	L	L	L	L	H	H	L	H	H	H	H	H	H	H	H	H	H	H	H	H	H
L	L	L	L	H	L	H	H	L	H	H	H	H	H	H	H	H	H	H	H	H	H
L	L	L	L	H	H	H	H	H	L	H	H	H	H	H	H	H	H	H	H	H	H
L	L	L	H	L	L	H	H	H	H	L	H	H	H	H	H	H	H	H	H	H	H
L	L	L	H	L	H	H	H	H	H	H	L	H	H	H	H	H	H	H	H	H	H
L	L	L	H	H	L	H	H	H	H	H	H	L	H	H	H	H	H	H	H	H	H
L	L	L	H	H	H	H	H	H	H	H	H	H	L	H	H	H	H	H	H	H	H
L	L	H	L	L	L	H	H	H	H	H	H	H	H	L	H	H	H	H	H	H	H
L	L	H	L	L	H	H	H	H	H	H	H	H	H	H	L	H	H	H	H	H	H
L	L	H	L	H	L	H	H	H	H	H	H	H	H	H	H	L	H	H	H	H	H
L	L	H	L	H	H	H	H	H	H	H	H	H	H	H	H	H	L	H	H	H	H
L	L	H	H	L	L	H	H	H	H	H	H	H	H	H	H	H	H	L	H	H	H
L	L	H	H	L	H	H	H	H	H	H	H	H	H	H	H	H	H	H	L	H	H
L	L	H	H	H	L	H	H	H	H	H	H	H	H	H	H	H	H	H	H	L	H
L	L	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	L
L	H	X	X	X	X	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H
H	L	X	X	X	X	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H
H	H	X	X	X	X	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H

H = high level, L = low level, X = irrelevant

Figure 1: Function Table

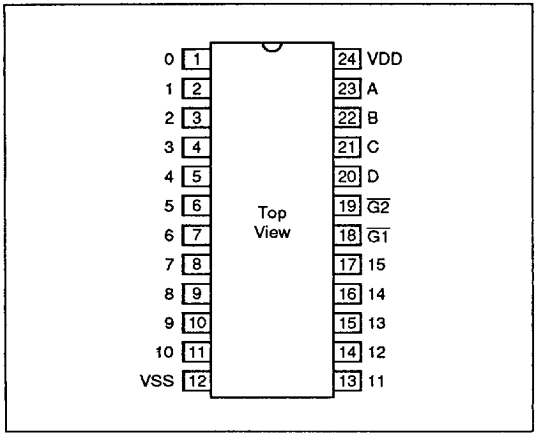


Figure 2: Pin Out

54HSC/T154 : 4 to 16 Line Decoders/Demultiplexers

Sym	Parameter	+25°C		-55°C / +125°C		Units
		Typ.	Max.	Typ.	Max.	
t_{PLH}	Propagation delay low to high level output for change in A B C or D input	18	30	21	33	ns
t_{PHL}	Propagation delay high to low level output for change in A B C or D input	21	30	24	33	ns
t_{PLH}	Propagation delay low to high level output for change in $\overline{G1}$ or $\overline{G2}$	21	30	24	33	ns
t_{PHL}	Propagation delay high to low level output for change in $\overline{G1}$ or $\overline{G2}$	18	30	21	33	ns

Figure 3: Switching Characteristics

Symbol	Parameter	Test Conditions	Limits				Units
			+25°C		-55°C / +125°C		
			Min.	Max.	Min.	Max.	
I_{DD}	Quiescent Current	V_{IN} = 0V or V_{DD}	-	100	-	600	µA
V_{OL}	Output Voltage Low Level	I_{OL} = 9mA	-	0.4	-	0.4	V
V_{OH}	Output Voltage High Level	I_{OH} = -11mA	2.5	-	2.5	-	V
V_{IL1}	Voltage Input Low (CMOS)	-	-	1.5	-	1.5	V
V_{IH1}	Voltage Input High (CMOS)	-	3.5	-	3.5	-	V
V_{IL2}	Voltage Input Low (TTL)	-	-	0.8	-	0.8	V
V_{IH2}	Voltage Input High (TTL)	-	2.0	-	2.0	-	V
I_{IN}	Input Leakage Current	V_{IN} = V_{DD} or V_{SS}	-	±0.5	-	±5.0	µA

Figure 4: DC Characteristics

54HSC/T154 : 4 to 16 Line Decoders/Demultiplexers

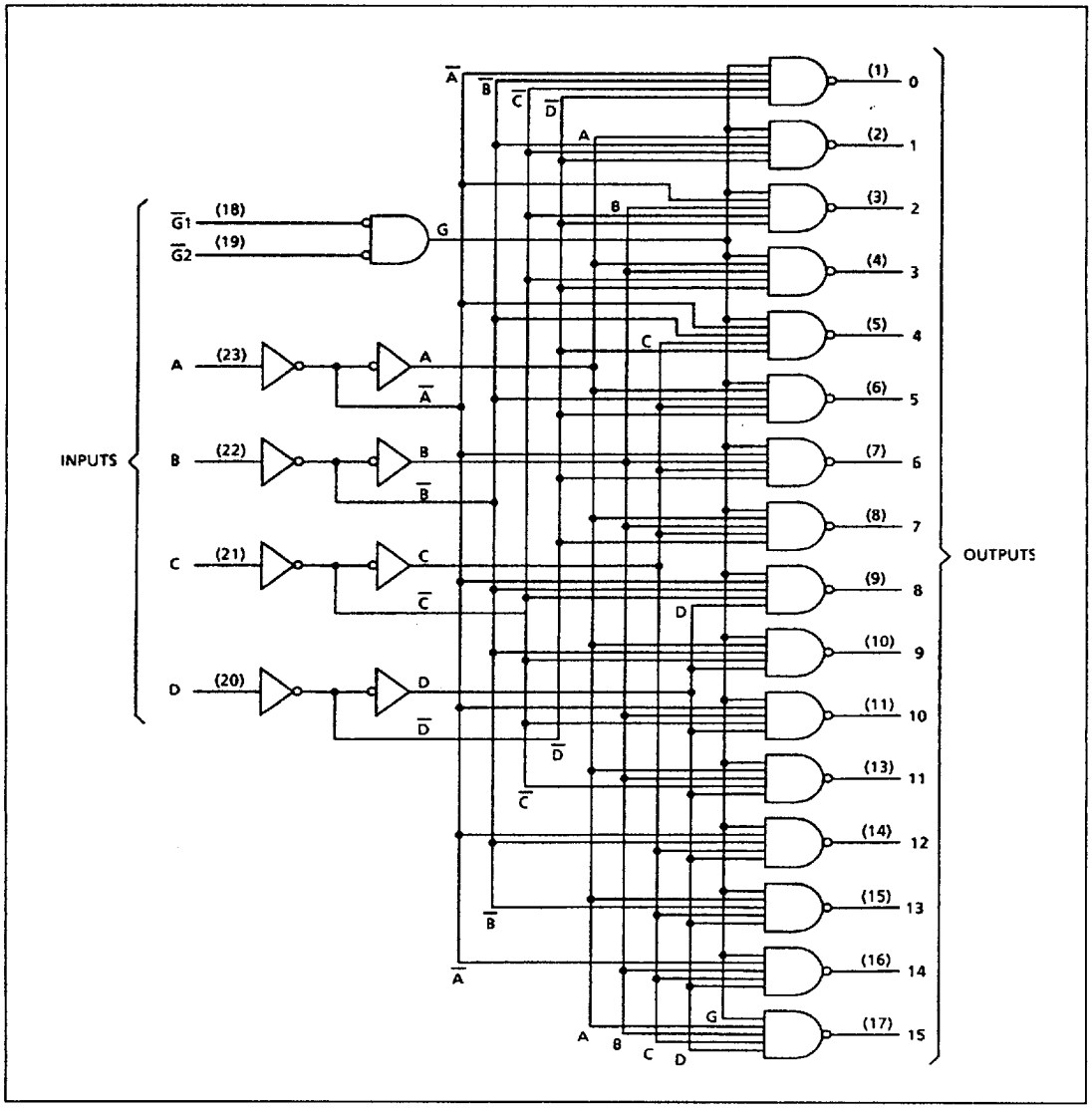


Figure 5: Logic Diagram

54HSC/T157 : Quad 2-Line to 1-Line Data Selectors/Multiplexers

The 54HSC/T157 is a Quadruple 2-Line to 1-Line Data Selector with non-inverted output. The strobe must be low to enable the device. When select is low, A is selected. When select is high, B is selected.

Inputs				Outputs
$\overline{STR}$	Select	A	B	Y
H	X	X	X	L
L	L	L	X	L
L	L	H	X	H
L	H	X	L	L
L	H	X	H	H

H = high level, L = low level, X = irrelevant

Figure 1: Function Table

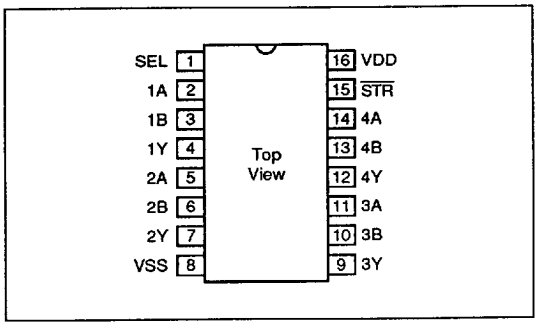


Figure 2: Pin Out

Symbol	Parameter	+25°C Typ.	+25°C Max.	-55°C / +125°C Typ.	-55°C / +125°C Max.	Units
t_{PLH}	Propagation delay A or B to Y	14	25	17	25	ns
t_{PHL}	Propagation delay A or B to Y	15	20	18	22	ns
t_{PZH}	Propagation delay Strobe to Y	14	22	17	24	ns
t_{PZL}	Propagation delay Strobe to Y	15	22	18	24	ns
t_{PHZ}	Propagation delay Select to Y	14	25	17	25	ns
t_{PLZ}	Propagation delay Select to Y	15	25	18	25	ns

Figure 3: Switching Characteristics

Symbol	Parameter	Test Conditions	Limits +25°C Min.	Limits +25°C Max.	Limits -55°C / +125°C Min.	Limits -55°C / +125°C Max.	Units
I_{DD}	Quiescent Current	V_{IN} = 0V or V_{DD}	-	20	-	600	µA
V_{OL}	Output Voltage Low Level	I_{OL} = 9mA	-	0.4	-	0.4	V
V_{OH}	Output Voltage High Level	I_{OH} = -11mA	2.5	-	2.5	-	V
V_{IL1}	Voltage Input Low (CMOS)	-	-	1.5	-	1.5	V
V_{IH1}	Voltage Input High (CMOS)	-	3.5	-	3.5	-	V
V_{IL2}	Voltage Input Low (TTL)	-	-	0.8	-	0.8	V
V_{IH2}	Voltage Input High (TTL)	-	2.0	-	2.0	-	V
I_{IN}	Input Leakage Current	V_{IN} = V_{DD} or V_{SS}	-	±0.5	-	±5.0	µA

Figure 4: DC Characteristics

54HSC/T157 : Quad 2-Line to 1-Line Data Selectors/Multiplexers

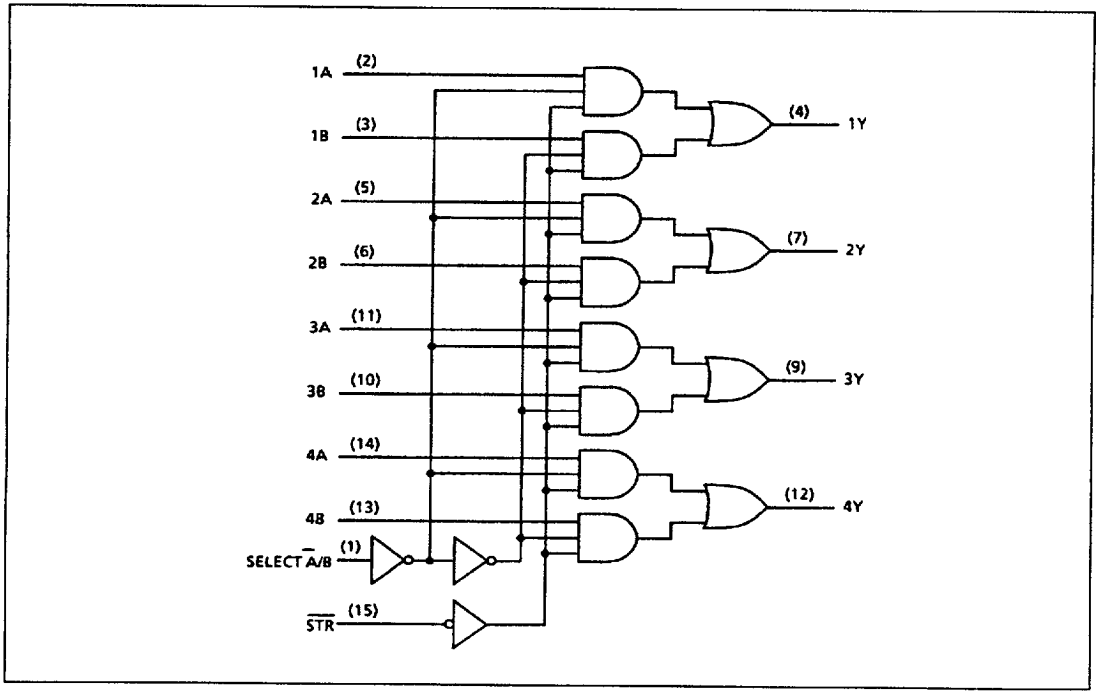


Figure 5: Logic Diagram

54HSC/T238 : 3-Line to 8-Line Decoder/Demultiplexer

The 54HSC/T238 is a 3-Line to 8-Line Decoder/Demultiplexer, with unlatched inputs and non-inverted outputs.

Enable Inputs		Select Inputs			Outputs							
E_3	$\overline{E}_2/\overline{E}_1$	A_2	A_1	A_0	O_0	O_1	O_2	O_3	O_4	O_5	O_6	O_7
X	H	X	X	X	L	L	L	L	L	L	L	L
L	X	X	X	X	L	L	L	L	L	L	L	L
H	L	L	L	L	H	L	L	L	L	L	L	L
H	L	L	L	H	L	H	L	L	L	L	L	L
H	L	L	H	L	L	L	H	L	L	L	L	L
H	L	L	H	H	L	L	L	H	L	L	L	L
H	L	H	L	L	L	L	L	L	H	L	L	L
H	L	H	L	H	L	L	L	L	L	H	L	L
H	L	H	H	L	L	L	L	L	L	L	H	L
H	L	H	H	H	L	L	L	L	L	L	L	H

H = high level, L = low level, X = irrelevant

Figure 1: Function Table

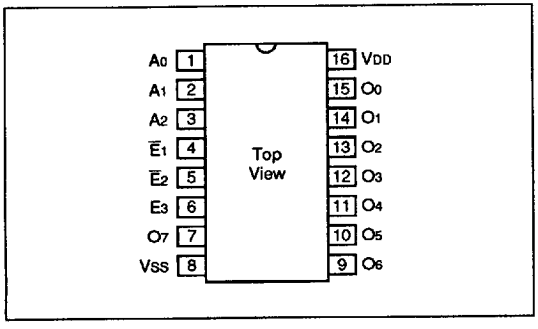


Figure 2: Pin Out

Symbol	Parameter	+25°C		-55°C / +125°C		Units
		Typ.	Max.	Typ.	Max.	
t_{PLH}	Propagation delay, address to output, low to high level output	16	24	19	27	ns
t_{PHL}	Propagation delay, address to output, high to low level output	17	25	20	28	ns
t_{PLH}	Propagation delay, enable to output, low to high level output	19	27	22	30	ns
t_{PHL}	Propagation delay, enable to output, high to low level output	19	27	22	30	ns

Figure 3: Switching Characteristics

54HSC/T238 : 3-Line to 8-Line Decoder/Demultiplexer

Symbol	Parameter	Test Conditions	Limits				Units
			+25°C		-55°C / +125°C		
			Min.	Max.	Min.	Max.	
I_{DD}	Quiescent Current	V_{IN} = 0V or V_{DD}	-	20	-	600	µA
V_{OL}	Output Voltage Low Level	I_{OL} = 9mA	-	0.4	-	0.4	V
V_{OH}	Output Voltage High Level	I_{OH} = -11mA	2.5	-	2.5	-	V
V_{IL1}	Voltage Input Low (CMOS)	-	-	1.5	-	1.5	V
V_{IH1}	Voltage Input High (CMOS)	-	3.5	-	3.5	-	V
V_{IL2}	Voltage Input Low (TTL)	-	-	0.8	-	0.8	V
V_{IH2}	Voltage Input High (TTL)	-	2.0	-	2.0	-	V
I_{IN}	Input Leakage Current	V_{IN} = V_{DD} or V_{SS}	-	±0.5	-	±5.0	µA

Figure 4: DC Characteristics

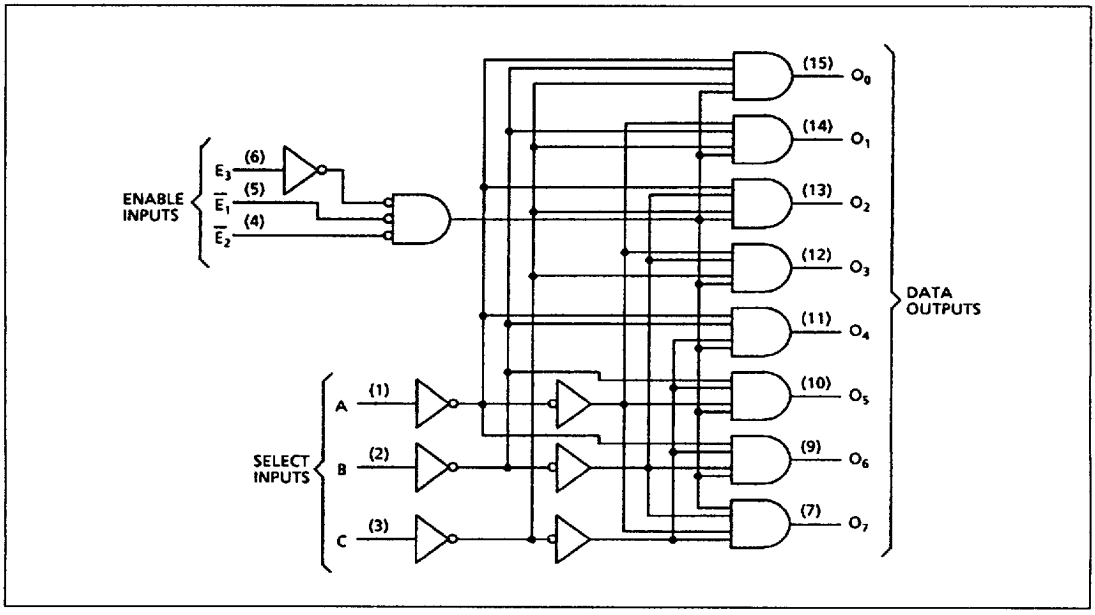


Figure 5: Logic Diagram

54HSC/T253 : Dual 4 to 1 Data Selectors/Multiplexers

The 54HSC/T253 is a Dual 4-Line to 1-Line Data Selector/Multiplexer with tri-state outputs.

Select Inputs		Data Inputs				Output Control	Output
B	A	C0	C1	C2	C3	$\overline{G}$	Y
X	X	X	X	X	X	H	Z
L	L	L	X	X	X	L	L
L	L	H	X	X	X	L	H
L	H	X	L	X	X	L	L
L	H	X	H	X	X	L	H
H	L	X	X	L	X	L	L
H	L	X	X	H	X	L	H
H	H	X	X	X	L	L	L
H	H	X	X	X	H	L	H

H = high level, L = low level, X = irrelevant, Z = high impedance

Figure 1: Function Table

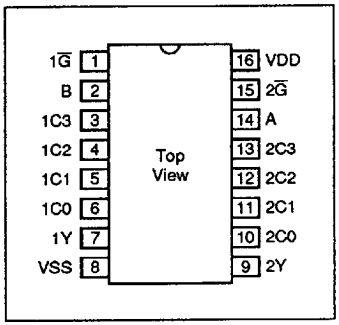


Figure 2: Pin Out

Symbol	Parameter	+25°C		-55°C / +125°C		Units
		Typ.	Max.	Typ.	Max.	
t_{PLH}	Propagation delay Data to Output	14	25	17	25	ns
t_{PHL}	Propagation delay Data to Output	15	25	18	25	ns
t_{PLH}	Propagation delay Select to Output	14	25	17	25	ns
t_{PHL}	Propagation delay Select to Output	15	25	18	25	ns
t_{PZL}	Propagation delay Tri-state to Output Low	12	25	15	25	ns
t_{PZH}	Propagation delay Tri-state to Output High	13	25	16	25	ns
t_{PLZ}	Propagation delay Low to Tri-state	12	25	15	25	ns
t_{PHZ}	Propagation delay High to Tri-state	13	25	16	25	ns

Figure 3: Switching Characteristics

54HSC/T253 : Dual 4 to 1 Data Selectors/Multiplexers

Symbol	Parameter	Test Conditions	Limits				Units
			+25°C		-55°C / +125°C		
			Min.	Max.	Min.	Max.	
I_{DD}	Quiescent Current	V_{IN} = 0V or V_{DD}	-	20	-	600	µA
V_{OL}	Output Voltage Low Level	I_{OL} = 9mA	-	0.4	-	0.4	V
V_{OH}	Output Voltage High Level	I_{OH} = -11mA	2.5	-	2.5	-	V
V_{IL1}	Voltage Input Low (CMOS)	-	-	1.5	-	1.5	V
V_{IH1}	Voltage Input High (CMOS)	-	3.5	-	3.5	-	V
V_{IL2}	Voltage Input Low (TTL)	-	-	0.8	-	0.8	V
V_{IH2}	Voltage Input High (TTL)	-	2.0	-	2.0	-	V
I_{OZ}	Tri-State Leakage	V_O = 0V or V_{DD}	-	±1	-	±50	µA
I_{IN}	Input Leakage Current	V_{IN} = V_{DD} or V_{SS}	-	±0.5	-	±5.0	µA

Figure 4: DC Characteristics

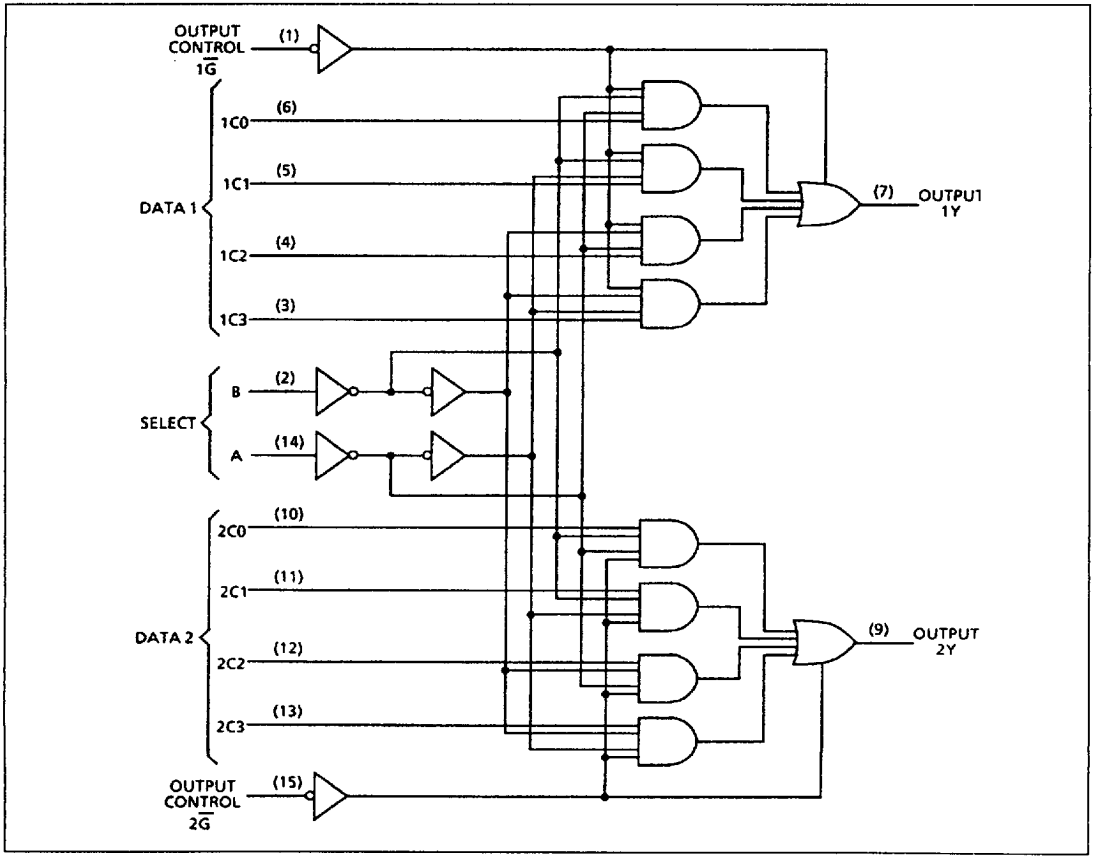


Figure 5: Logic Diagram

54HSC/T164 : 8-Bit Parallel Output Serial Shift Register

The 54HSC/T164 is an 8-Bit Parallel Output Serial Shift Register with asynchronous clear.

Inputs				Outputs		
$\overline{CLEAR}$	CLOCK	A	B	Q_A	Q_B	Q_H
L	X	X	X	L	L	L
H	L	X	X	Q_{AO}	Q_{BO}	Q_{HO}
H	↑	H	H	H	Q_{AN}	Q_{GN}
H	↑	L	X	L	Q_{AN}	Q_{GN}
H	↑	X	L	L	Q_{AN}	Q_{GN}

H = high level, L = low level, X = irrelevant, ↑ = transition from low to high level. Q_{AO}, Q_{BO}, Q_{HO} = the level of Q_A, Q_B or Q_H, respectively, before the indicated steady-state input conditions were set up. Q_{AN}, Q_{BN}, Q_{HN} = the level of Q_A or Q_G before the latest ↑ transition of the clock. Indicates a one bit shift.

Figure 1: Function Table

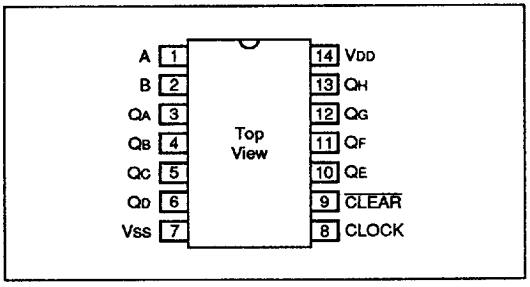


Figure 2: Pin Out

Symbol	Parameter	+25°C Typ.	+25°C Max.	-55°C / +125°C Typ.	-55°C / +125°C Max.	Units
t_{PLH}	Propagation delay. Q output from clock input, low to high level output.	15	25	18	28	ns
t_{PHL}	Propagation delay. Q output from clock input, high to low level output.	15	25	18	28	ns
t_{PHL}	Propagation delay. Q output from clear input, high to low level output.	15	25	18	28	ns

Figure 3: Switching Characteristics

Symbol	Parameter	Test Conditions	Limits +25°C Min.	Limits +25°C Max.	Limits -55°C / +125°C Min.	Limits -55°C / +125°C Max.	Units
I_{DD}	Quiescent Current	V_{IN} = 0V or V_{DD}	-	20	-	400	µA
V_{OL}	Output Voltage Low Level	I_{OL} = 9mA	-	0.4	-	0.4	V
V_{OH}	Output Voltage High Level	I_{OH} = -11mA	2.5	-	2.5	-	V
V_{IL1}	Voltage Input Low (CMOS)	-	-	1.5	-	1.5	V
V_{IH1}	Voltage Input High (CMOS)	-	3.5	-	3.5	-	V
V_{IL2}	Voltage Input Low (TTL)	-	-	0.8	-	0.8	V
V_{IH2}	Voltage Input High (TTL)	-	2.0	-	2.0	-	V
I_{IN}	Input Leakage Current	V_{IN} = V_{DD} or V_{SS}	-	±0.5	-	±5.0	µA

Figure 4: DC Characteristics

54HSC/T164 : 8-Bit Parallel Output Serial Shift Register

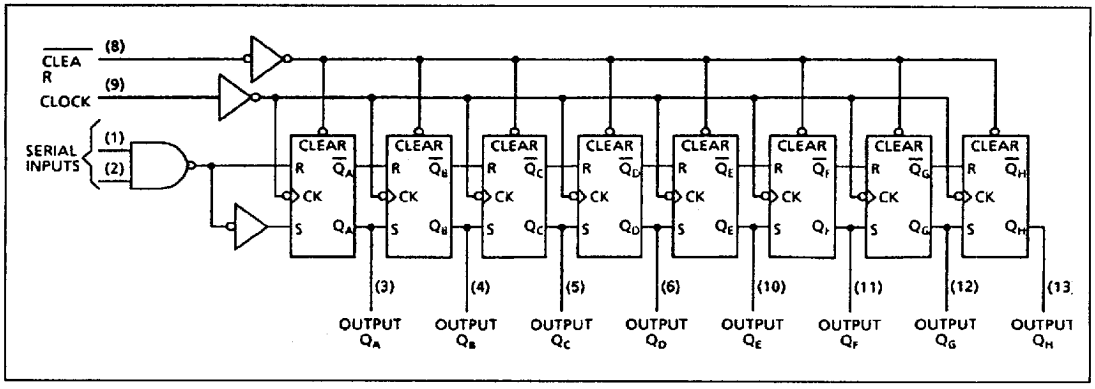


Figure 5: Logic Diagram

54HSC/T165 : Parallel Load 8-Bit Shift Register

The 54HSC/T165 is an 8-Bit Serial Shift Register that shifts the data in the direction of Q_A to Q_H when clocked.

Inputs					Internal Outputs		Output
Shift/$\overline{\text{Load}}$	Clock Inhibit	Clock	Serial	Parallel A...H	Q_A	Q_B	Q_H
L	X	X	X	a...h	a	b	h
H	L	L	X	X	Q_{AO}	Q_{BO}	Q_{HO}
H	L	↑	H	X	H	Q_{AN}	Q_{GN}
H	L	↑	L	X	L	Q_{AN}	Q_{GN}
H	H	X	X	X	Q_{AO}	Q_{BO}	Q_{HO}

H = high level, L = low level, X = irrelevant, ↑ = transition from low to high, a...h = the level of steady state inputs at inputs A through H. Q_O = level of Q before the indicated steady state input conditions were set up. Q_N = level of Q before the most recent active transition indicated by ↑.

Figure 1: Function Table

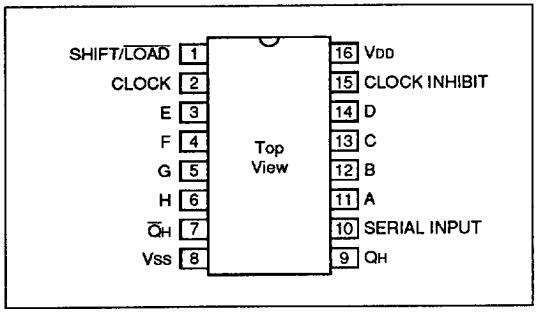


Figure 2: Pin Out

Symbol	Parameter	+25°C		-55°C / +125°C		Units
		Typ.	Max.	Typ.	Max.	
t_{PLH}	Propagation delay. Load to Any Output.	18	25	21	28	ns
t_{PHL}	Propagation delay. Load to Any Output.	16	25	19	28	ns
t_{PLH}	Propagation delay. Clock to Any Output.	18	25	21	28	ns
t_{PHL}	Propagation delay. Clock to Any Output.	18	25	21	28	ns
t_{PLH}	Propagation delay. H to Q_H.	18	25	21	28	ns
t_{PHL}	Propagation delay. H to Q_H.	18	25	21	28	ns
t_{PLH}	Propagation delay. H to QB_H.	18	25	21	28	ns
t_{PHL}	Propagation delay. H to QB_H.	18	25	21	28	ns

Figure 3: Switching Characteristics

54HSC/T165 : Parallel Load 8-Bit Shift Register

Symbol	Parameter	Test Conditions	Limits				Units
			+25°C		-55°C / +125°C		
			Min.	Max.	Min.	Max.	
I_{DD}	Quiescent Current	V_{IN} = 0V or V_{DD}	-	20	-	400	µA
V_{OL}	Output Voltage Low Level	I_{OL} = 9mA	-	0.4	-	0.4	V
V_{OH}	Output Voltage High Level	I_{OH} = -11mA	2.5	-	2.5	-	V
V_{IL1}	Voltage Input Low (CMOS)	-	-	1.5	-	1.5	V
V_{IH1}	Voltage Input High (CMOS)	-	3.5	-	3.5	-	V
V_{IL2}	Voltage Input Low (TTL)	-	-	0.8	-	0.8	V
V_{IH2}	Voltage Input High (TTL)	-	2.0	-	2.0	-	V
I_{IN}	Input Leakage Current	V_{IN} = V_{DD} or V_{SS}	-	±0.5	-	±5.0	µA

Figure 4: DC Characteristics

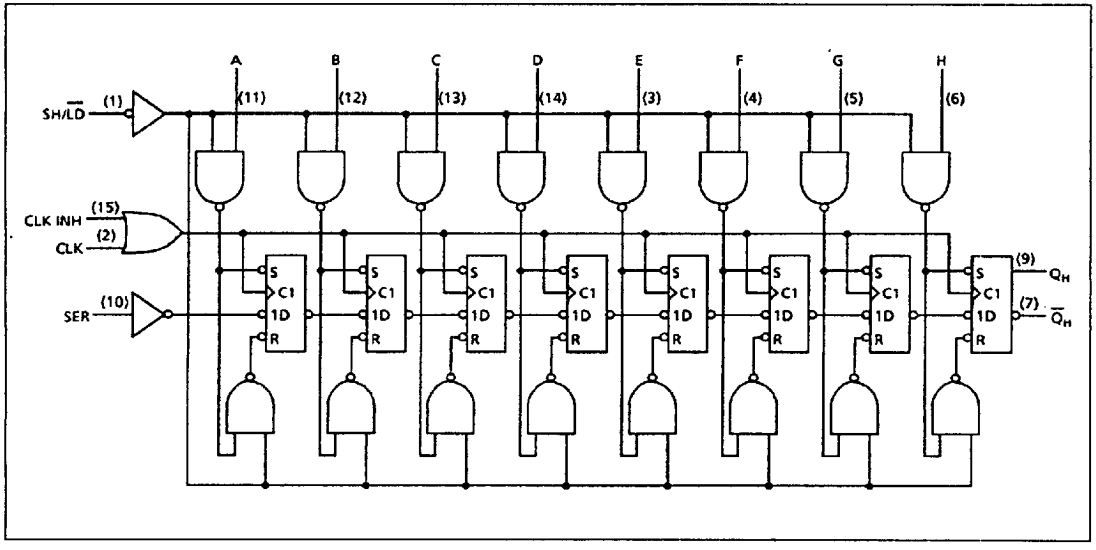


Figure 5: Logic Diagram

54HSC/T166 : 8-Bit Shift Register

The 54HSC/T166 is an 8-Bit parallel in or serial in, serial out Shift Register with a gated clock input and an overriding clear input.

Inputs						Internal Outputs		Output
$\overline{\text{Clear}}$	Shift/ $\overline{\text{Load}}$	Clock Inhibit	Clock	Serial	Parallel A...H	Q_A	Q_B	Q_H
L	X	X	X	X	X	L	L	L
H	X	L	L	X	X	Q_{AO}	Q_{BO}	Q_{HO}
H	L	L	↑	X	a...h	a	b	h
H	H	L	↑	H	X	H	Q_{AN}	Q_{GN}
H	H	L	↑	L	X	L	Q_{AN}	Q_{GN}
H	X	H	↑	X	X	Q_{AO}	Q_{BO}	Q_{HO}

H = high level, L = low level, X = irrelevant, ↑ = transition from low to high, a...h = the level of steady state inputs at inputs A through H. Q_O = level of Q before the indicated steady state input conditions were set up. Q_N = level of Q before the most recent active transition indicated by ↑.

Figure 1: Function Table

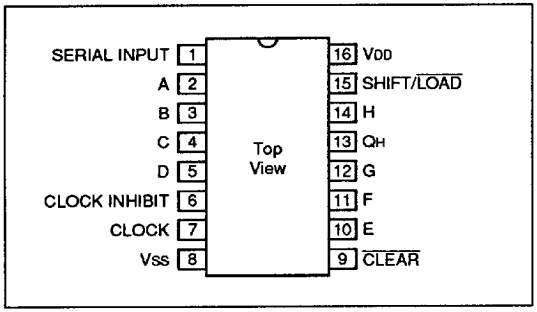


Figure 2: Pin Out

Symbol	Parameter	+25°C		-55°C / +125°C		Units
		Typ.	Max.	Typ.	Max.	
t_{PHL}	Propagation delay. Clear to Q_H.	15	25	18	28	ns
t_{PHL}	Propagation delay. Clock to Q_H.	15	25	18	28	ns
t_{PLH}	Propagation delay. Clock to Q_H.	15	25	18	28	ns

Figure 3: Switching Characteristics

54HSC/T166 : 8-Bit Shift Register

Symbol	Parameter	Test Conditions	Limits				Units
			+25°C		-55°C / +125°C		
			Min.	Max.	Min.	Max.	
I_{DD}	Quiescent Current	V_{IN} = 0V or V_{DD}	-	20	-	400	µA
V_{OL}	Output Voltage Low Level	I_{OL} = 9mA	-	0.4	-	0.4	V
V_{OH}	Output Voltage High Level	I_{OH} = -11mA	2.5	-	2.5	-	V
V_{IL1}	Voltage Input Low (CMOS)	-	-	1.5	-	1.5	V
V_{IH1}	Voltage Input High (CMOS)	-	3.5	-	3.5	-	V
V_{IL2}	Voltage Input Low (TTL)	-	-	0.8	-	0.8	V
V_{IH2}	Voltage Input High (TTL)	-	2.0	-	2.0	-	V
I_{IN}	Input Leakage Current	V_{IN} = V_{DD} or V_{SS}	-	±0.5	-	±5.0	µA

Figure 4: DC Characteristics

54HSC/T166 : 8-Bit Shift Register

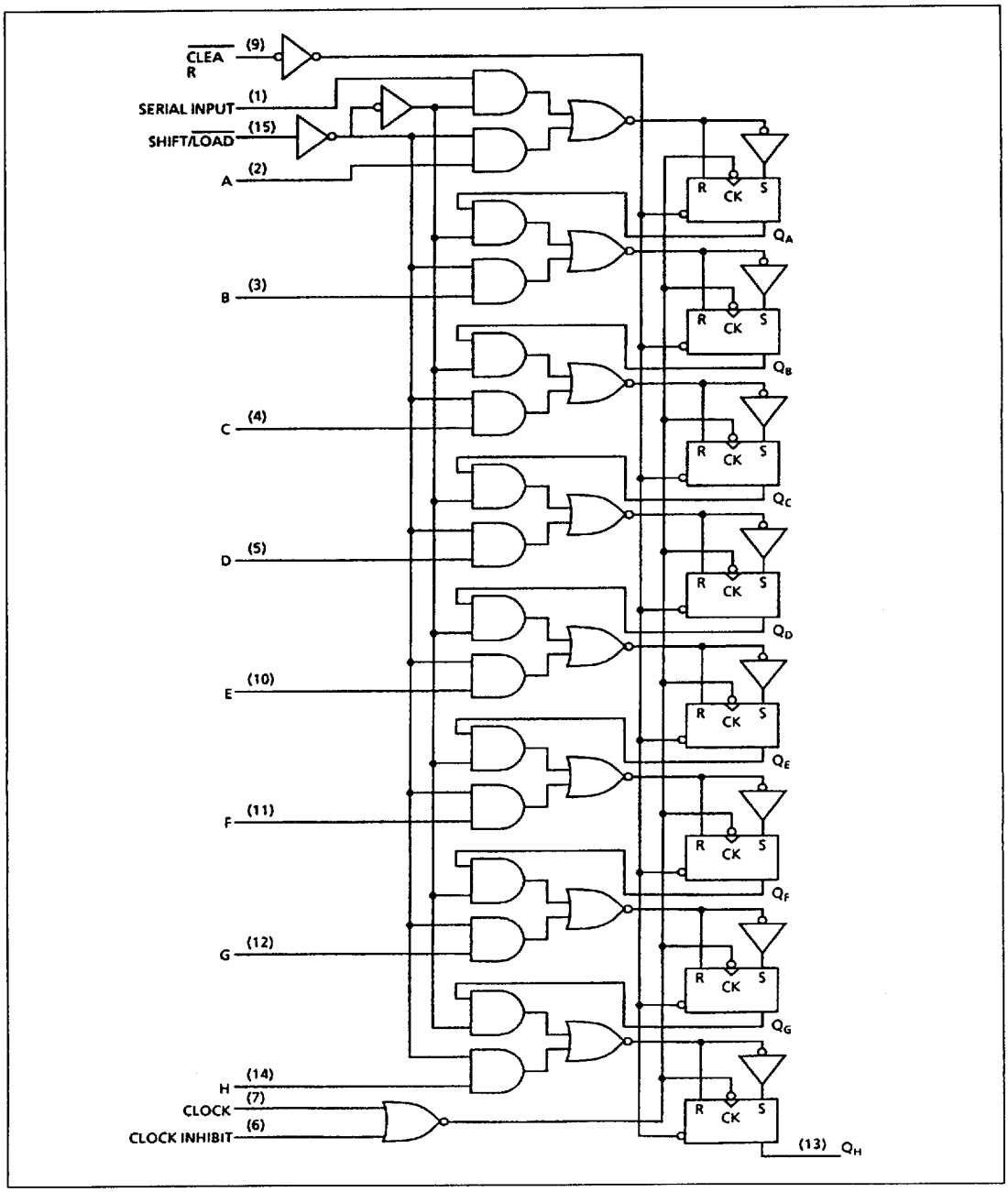


Figure 5: Logic Diagram

54HSC/T521 : 8-Bit Magnitude Comparator

The 54HSC/T521 is an 8-Bit Magnitude Comparator.

Inputs		Outputs
Data P,Q	Enable $\overline{G}$	$\overline{P = Q}$
P = Q	L	L
P > Q	L	H
P < Q	L	H
X	H	H

H = high level, L = low level, X = irrelevant

Figure 1: Function Table

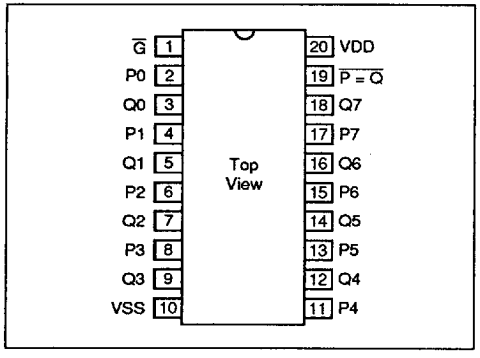


Figure 2: Pin Out

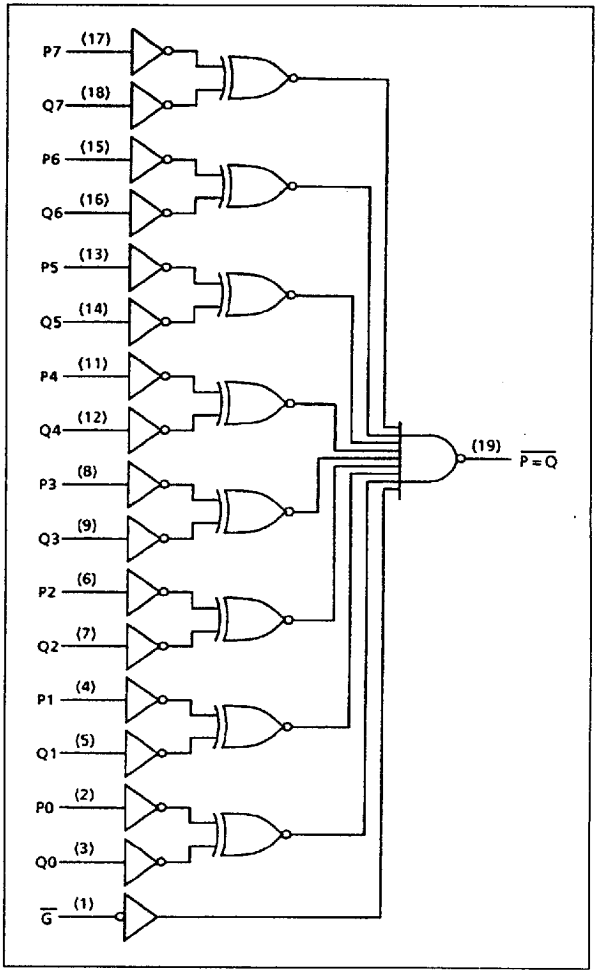


Figure 3: Logic Diagram

Symbol	Parameter	+25°C		-55°C / +125°C		Units
		Typ.	Max.	Typ.	Max.	
t_{PLH}	Propagation delay. P or Q to PN = QN.	15	25	18	28	ns
t_{PHL}	Propagation delay. P or Q to PN = QN.	16	25	19	28	ns
t_{PLH}	Propagation delay. GN to PN = QN.	14	25	17	28	ns
t_{PHL}	Propagation delay. GN to PN = QN.	15	25	18	28	ns

Figure 4: Switching Characteristics

54HSC/T521 : 8-Bit Magnitude Comparator

Symbol	Parameter	Test Conditions	Limits				Units
			+25°C		-55°C / +125°C		
			Min.	Max.	Min.	Max.	
I_{DD}	Quiescent Current	V_{IN} = 0V or V_{DD}	-	20	-	600	µA
V_{OL}	Output Voltage Low Level	I_{OL} = 9mA	-	0.4	-	0.4	V
V_{OH}	Output Voltage High Level	I_{OH} = -11mA	2.5	-	2.5	-	V
V_{IL1}	Voltage Input Low (CMOS)	-	-	1.5	-	1.5	V
V_{IH1}	Voltage Input High (CMOS)	-	3.5	-	3.5	-	V
V_{IL2}	Voltage Input Low (TTL)	-	-	0.8	-	0.8	V
V_{IH2}	Voltage Input High (TTL)	-	2.0	-	2.0	-	V
I_{IN}	Input Leakage Current	V_{IN} = V_{DD} or V_{SS}	-	±0.5	-	±5.0	µA

Figure 5: DC Characteristics

54HSC/T240 : Octal 3-State Driver, Inverting

The 54HSC/T240 is an Octal 3-State Driver, inverting.

Inputs		Outputs
$\overline{E}$	I_{0-3}	$\overline{O}_{0-3}$
L	L	H
L	H	L
H	X	Z

H = high level
L = low level
X = irrelevant
Z = high impedance

Figure 1: Function Table

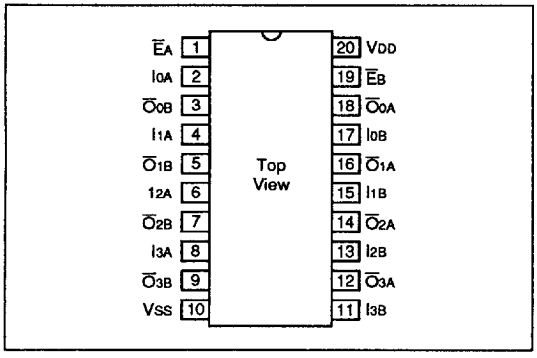


Figure 2: Pin Out

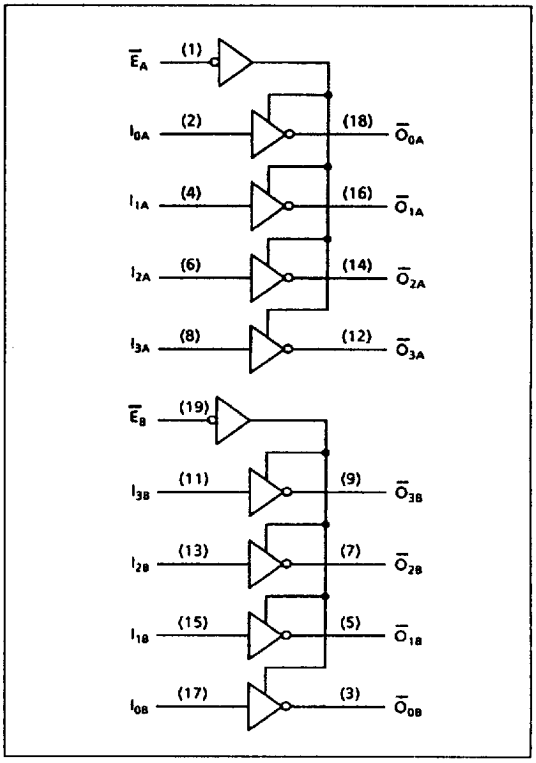


Figure 3: Logic Diagram

Symbol	Parameter	+25°C		-55°C / +125°C		Units
		Typ.	Max.	Typ.	Max.	
t_{PLH}	Propagation delay, low to high level output.	12	20	15	23	ns
t_{PHL}	Propagation delay, high to low level output.	14	22	17	25	ns
t_{PZL}	Propagation delay, enable to low level.	19	27	21	30	ns
t_{PZH}	Propagation delay, enable to high level.	14	22	17	25	ns
t_{PLZ}	Propagation delay, disable from low.	22	30	25	33	ns
t_{PHZ}	Propagation delay, disable from high.	21	30	24	33	ns

Figure 4: Switching Characteristics

54HSC/T240 : Octal 3-State Driver, Inverting

Symbol	Parameter	Test Conditions	Limits				Units
			+25°C		-55°C / +125°C		
			Min.	Max.	Min.	Max.	
I_{DD}	Quiescent Current	V_{IN} = 0V or V_{DD}	-	20	-	600	µA
V_{OL}	Output Voltage Low Level	I_{OL} = 9mA	-	0.4	-	0.4	V
V_{OH}	Output Voltage High Level	I_{OH} = -11mA	2.5	-	2.5	-	V
V_{IL1}	Voltage Input Low (CMOS)	-	-	1.5	-	1.5	V
V_{IH1}	Voltage Input High (CMOS)	-	3.5	-	3.5	-	V
V_{IL2}	Voltage Input Low (TTL)	-	-	0.8	-	0.8	V
V_{IH2}	Voltage Input High (TTL)	-	2.0	-	2.0	-	V
I_{OZ}	Tri-State Leakage	V_O = 0V or V_{DD}	-	±1	-	±50	µA
I_{IN}	Input Leakage Current	V_{IN} = V_{DD} or V_{SS}	-	±0.5	-	±5.0	µA

Figure 5: DC Characteristics

54HSC/T241 : Octal 3-State Driver, Complementary Enable

The 54HSC/T241 is an Octal 3-State Driver, complementary enable.

Inputs			Outputs
$\overline{E}_A$	E_B	I_{0-3}	O_{0-3}
L	H	L	H
L	H	H	L
H	L	X	Z

H = high level
L = low level
X = irrelevant
Z = high impedance

Figure 1: Function Table

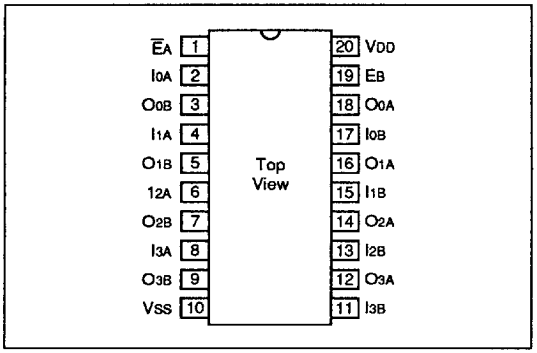


Figure 2: Pin Out

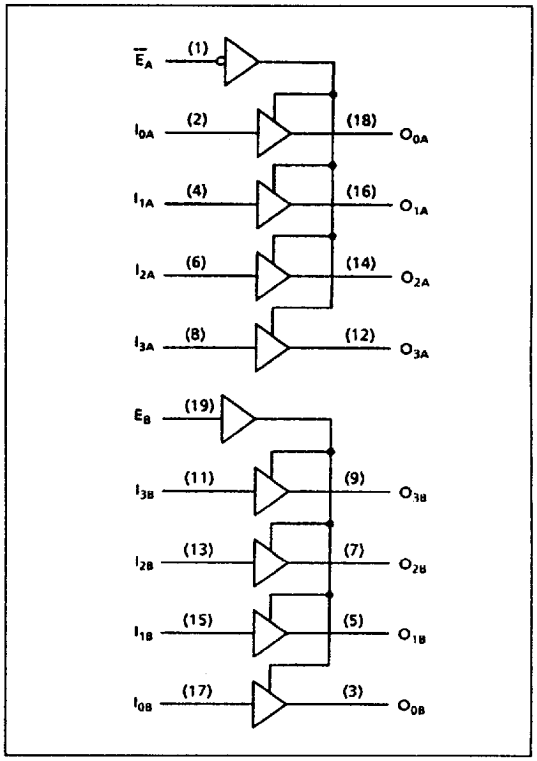


Figure 3: Logic Diagram

Symbol	Parameter	+25°C		-55°C / +125°C		Units
		Typ.	Max.	Typ.	Max.	
t_{PLH}	Propagation delay, low to high level output.	11	19	14	22	ns
t_{PHL}	Propagation delay, high to low level output.	13	21	16	24	ns
t_{PZL}	Propagation delay, enable to low level.	19	27	21	30	ns
t_{PZH}	Propagation delay, enable to high level.	19	27	21	30	ns
t_{PLZ}	Propagation delay, low to disable.	22	30	25	33	ns
t_{PHZ}	Propagation delay, high to disable.	21	30	24	33	ns

Figure 4: Switching Characteristics

54HSC/T241 : Octal 3-State Driver, Complementary Enable

Symbol	Parameter	Test Conditions	Limits				Units
			+25°C		-55°C / +125°C		
			Min.	Max.	Min.	Max.	
I_{DD}	Quiescent Current	V_{IN} = 0V or V_{DD}	-	20	-	600	µA
V_{OL}	Output Voltage Low Level	I_{OL} = 9mA	-	0.4	-	0.4	V
V_{OH}	Output Voltage High Level	I_{OH} = -11mA	2.5	-	2.5	-	V
V_{IL1}	Voltage Input Low (CMOS)	-	-	1.5	-	1.5	V
V_{IH1}	Voltage Input High (CMOS)	-	3.5	-	3.5	-	V
V_{IL2}	Voltage Input Low (TTL)	-	-	0.8	-	0.8	V
V_{IH2}	Voltage Input High (TTL)	-	2.0	-	2.0	-	V
I_{IN}	Input Leakage Current	V_{IN} = V_{DD} or V_{SS}	-	±0.5	-	±5.0	µA

Figure 5: DC Characteristics

54HSC/T244 : Octal 3-State Driver

The 54HSC/T244 is an Octal 3-State Driver.

Inputs		Outputs
$\overline{E}$	I_{0-3}	O_{0-3}
L	L	H
L	H	L
H	X	Z

H = high level
L = low level
X = irrelevant
Z = high impedance

Figure 1: Function Table

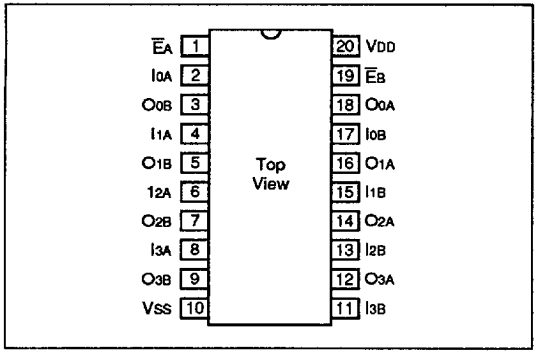


Figure 2: Pin Out

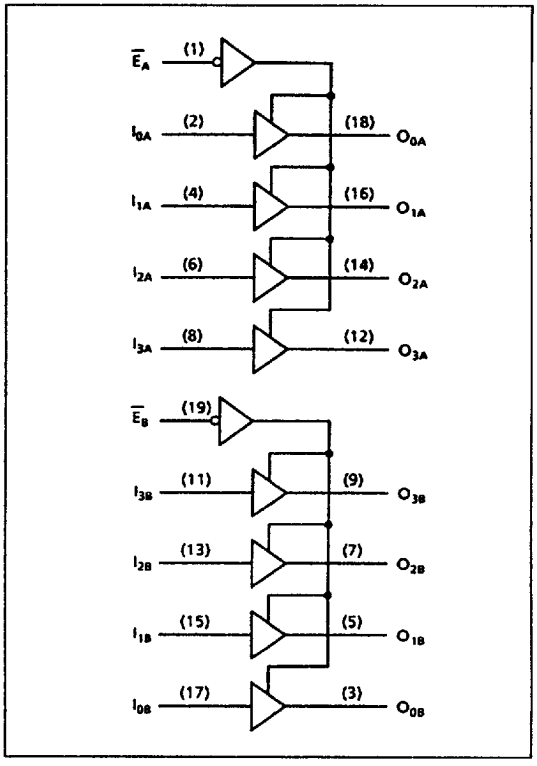


Figure 3: Logic Diagram

Symbol	Parameter	+25°C		-55°C / +125°C		Units
		Typ.	Max.	Typ.	Max.	
t_{PLH}	Propagation delay, low to high level output.	11	21	14	21	ns
t_{PHL}	Propagation delay, high to low level output.	13	21	16	21	ns
t_{PZL}	Propagation delay, enable to low level.	19	25	21	25	ns
t_{PZH}	Propagation delay, enable to high level.	15	20	21	24	ns
t_{PLZ}	Propagation delay, low to disable.	19	25	22	25	ns
t_{PHZ}	Propagation delay, high to disable.	18	25	21	25	ns

Figure 4: Switching Characteristics

54HSC/T244 : Octal 3-State Driver

Symbol	Parameter	Test Conditions	Limits				Units
			+25°C		-55°C / +125°C		
			Min.	Max.	Min.	Max.	
I_{DD}	Quiescent Current	V_{IN} = 0V or V_{DD}	-	20	-	600	µA
V_{OL}	Output Voltage Low Level	I_{OL} = 9mA	-	0.4	-	0.4	V
V_{OH}	Output Voltage High Level	I_{OH} = -11mA	2.5	-	2.5	-	V
V_{IL1}	Voltage Input Low (CMOS)	-	-	1.5	-	1.5	V
V_{IH1}	Voltage Input High (CMOS)	-	3.5	-	3.5	-	V
V_{IL2}	Voltage Input Low (TTL)	-	-	0.8	-	0.8	V
V_{IH2}	Voltage Input High (TTL)	-	2.0	-	2.0	-	V
I_{OZ}	Tri-State Leakage	V_O = 0V or V_{DD}	-	±1	-	±50	µA
I_{IN}	Input Leakage Current	V_{IN} = V_{DD} or V_{SS}	-	±0.5	-	±5.0	µA

Figure 5: DC Characteristics

54HSC/T540 : Octal 3-State Driver/Buffer Inverting

The 54HSC/T540 is an Octal 3-State Driver/Buffer Inverting.

Inputs			Outputs
$\overline{E}_A$	$\overline{E}_B$	I_{0-7}	$\overline{O}_{0-7}$
L	L	L	H
L	L	H	L
H	X	X	Z
X	H	X	Z

H = high level
L = low level
X = irrelevant
Z = high impedance

Figure 1: Function Table

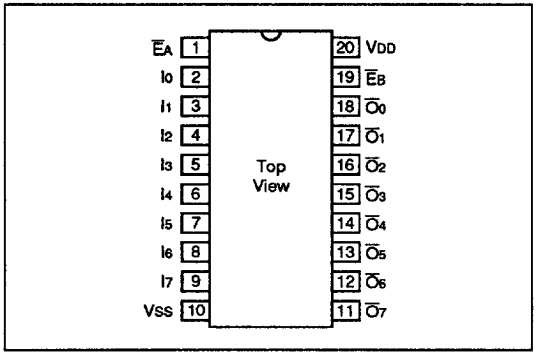


Figure 2: Pin Out

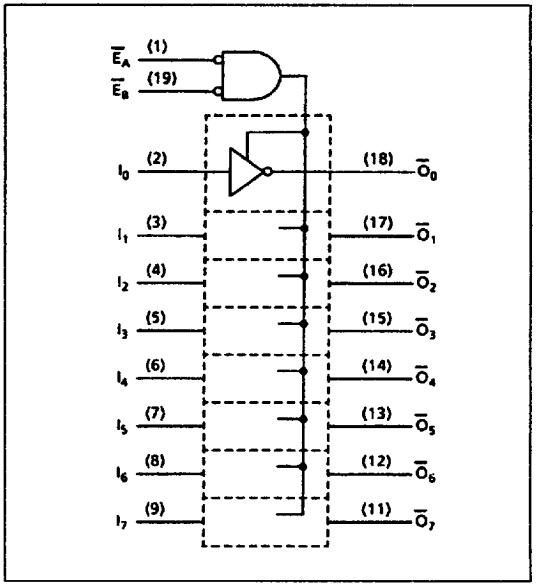


Figure 3: Logic Diagram

Symbol	Parameter	+25°C		-55°C / +125°C		Units
		Typ.	Max.	Typ.	Max.	
t_{PLH}	Propagation delay, low to high level output.	13	21	16	24	ns
t_{PHL}	Propagation delay, high to low level output.	13	21	16	24	ns
t_{PZL}	Propagation delay, enable to low level.	21	29	24	32	ns
t_{PZH}	Propagation delay, enable to high level.	16	24	19	27	ns
t_{PLZ}	Propagation delay, low to disable.	24	32	27	35	ns
t_{PHZ}	Propagation delay, high to disable.	23	31	26	34	ns

Figure 4: Switching Characteristics

54HSC/T540 : Octal 3-State Driver/Buffer Inverting

Symbol	Parameter	Test Conditions	Limits				Units
			+25°C		-55°C / +125°C		
			Min.	Max.	Min.	Max.	
I_{DD}	Quiescent Current	V_{IN} = 0V or V_{DD}	-	20	-	600	µA
V_{OL}	Output Voltage Low Level	I_{OL} = 9mA	-	0.4	-	0.4	V
V_{OH}	Output Voltage High Level	I_{OH} = -11mA	2.5	-	2.5	-	V
V_{IL1}	Voltage Input Low (CMOS)	-	-	1.5	-	1.5	V
V_{IH1}	Voltage Input High (CMOS)	-	3.5	-	3.5	-	V
V_{IL2}	Voltage Input Low (TTL)	-	-	0.8	-	0.8	V
V_{IH2}	Voltage Input High (TTL)	-	2.0	-	2.0	-	V
I_{OZ}	Tri-State Leakage	V_O = 0V or V_{DD}	-	±1	-	±50	µA
I_{IN}	Input Leakage Current	V_{IN} = V_{DD} or V_{SS}	-	±0.5	-	±5.0	µA

Figure 5: DC Characteristics

54HSC/T541 : Octal 3-State Driver/Buffer

The 54HSC/T541 is an Octal 3-State Driver/Buffer.

Inputs			Outputs
$\overline{E}_A$	$\overline{E}_B$	I_{0-7}	O_{0-7}
L	L	L	L
L	L	H	H
H	X	X	Z
X	H	X	Z

H = high level
L = low level
X = irrelevant
Z = high impedance

Figure 1: Function Table

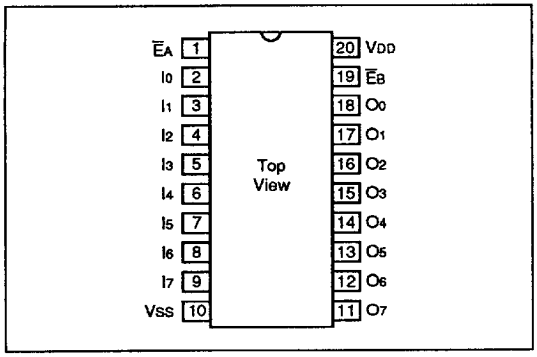


Figure 2: Pin Out

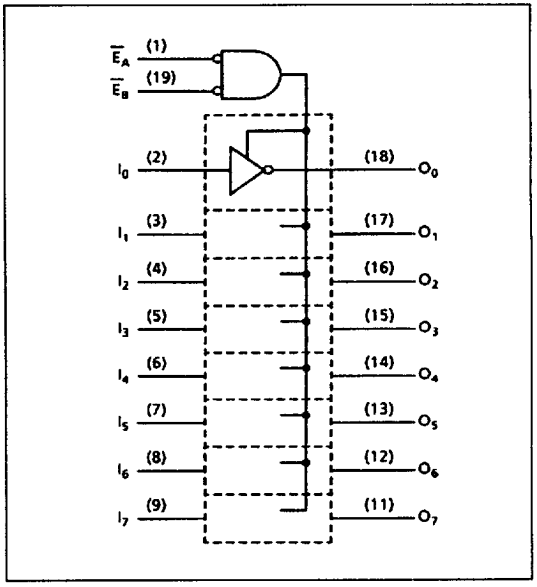


Figure 3: Logic Diagram

Symbol	Parameter	+25°C		-55°C / +125°C		Units
		Typ.	Max.	Typ.	Max.	
t_{PLH}	Propagation delay, low to high level output.	11	19	14	22	ns
t_{PHL}	Propagation delay, high to low level output.	13	21	16	22	ns
t_{PZL}	Propagation delay, enable to low level.	17	21	20	35	ns
t_{PZH}	Propagation delay, enable to high level.	16	24	19	30	ns
t_{PLZ}	Propagation delay, low to disable.	24	21	27	25	ns
t_{PHZ}	Propagation delay, high to disable.	23	21	26	25	ns

Figure 4: Switching Characteristics

54HSC/T541 : Octal 3-State Driver/Buffer

Symbol	Parameter	Test Conditions	Limits				Units
			+25°C		-55°C / +125°C		
			Min.	Max.	Min.	Max.	
I_{DD}	Quiescent Current	V_{IN} = 0V or V_{DD}	-	20	-	600	µA
V_{OL}	Output Voltage Low Level	I_{OL} = 9mA	-	0.4	-	0.4	V
V_{OH}	Output Voltage High Level	I_{OH} = -11mA	2.5	-	2.5	-	V
V_{IL1}	Voltage Input Low (CMOS)	-	-	1.5	-	1.5	V
V_{IH1}	Voltage Input High (CMOS)	-	3.5	-	3.5	-	V
V_{IL2}	Voltage Input Low (TTL)	-	-	0.8	-	0.8	V
V_{IH2}	Voltage Input High (TTL)	-	2.0	-	2.0	-	V
I_{OZ}	Tri-State Leakage	V_O = 0V or V_{DD}	-	±1	-	±50	µA
I_{IN}	Input Leakage Current	V_{IN} = V_{DD} or V_{SS}	-	±0.5	-	±5.0	µA

Figure 5: DC Characteristics

54HSC/T245 : Octal Bus Transceiver

The 54HSC/T245 is an Octal Bus Transceiver.

Inputs		Outputs
$\overline{E}$	DIR	
L	L	B data to Bus A
L	H	A data to Bus B
H	X	Isolation

H = high level, L = low level, X = irrelevant

Figure 1: Function Table

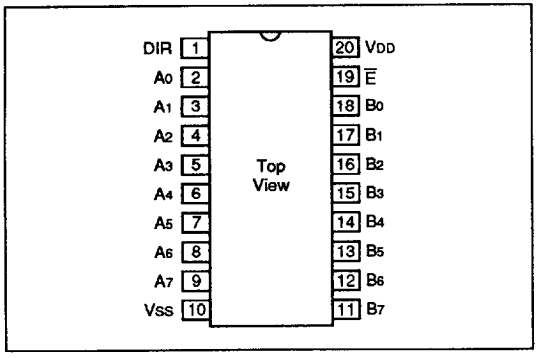


Figure 2: Pin Out

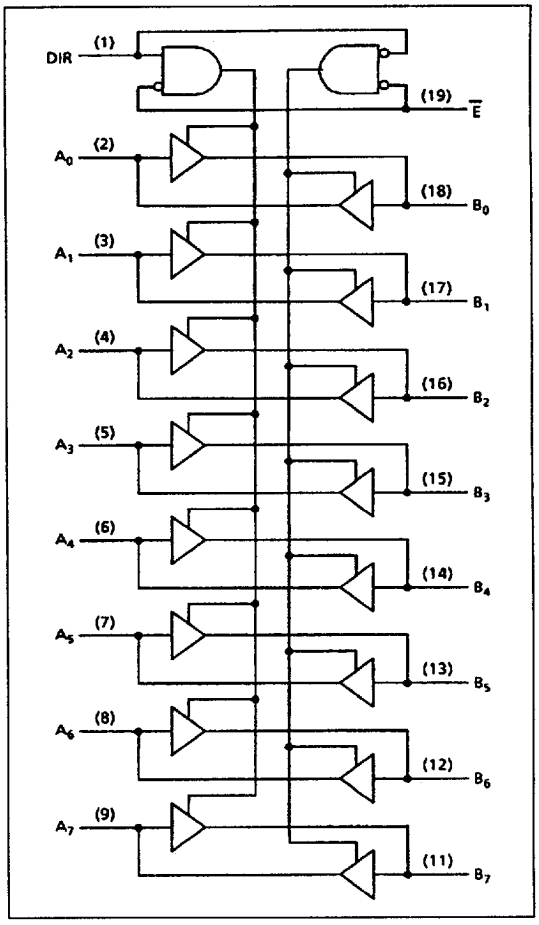


Figure 3: Logic Diagram

Symbol	Parameter	+25°C		-55°C / +125°C		Units
		Typ.	Max.	Typ.	Max.	
t_{PLH}	Propagation delay, low to high level output.	10	19	13	23	ns
t_{PHL}	Propagation delay, high to low level output.	11	19	14	23	ns
t_{PZL}	Propagation delay, enable to low level.	21	26	24	30	ns
t_{PZH}	Propagation delay, enable to high level.	16	25	19	28	ns
t_{PLZ}	Propagation delay, low to disable.	24	28	27	33	ns
t_{PHZ}	Propagation delay, high to disable.	24	28	27	33	ns

Figure 4: Switching Characteristics

54HSC/T245 : Octal Bus Transceiver

Symbol	Parameter	Test Conditions	Limits				Units
			+25°C		-55°C / +125°C		
			Min.	Max.	Min.	Max.	
I_{DD}	Quiescent Current	V_{IN} = 0V or V_{DD}	-	20	-	600	µA
V_{OL}	Output Voltage Low Level	I_{OL} = 9mA	-	0.4	-	0.4	V
V_{OH}	Output Voltage High Level	I_{OH} = -11mA	2.5	-	2.5	-	V
V_{IL1}	Voltage Input Low (CMOS)	-	-	1.5	-	1.5	V
V_{IH1}	Voltage Input High (CMOS)	-	3.5	-	3.5	-	V
V_{IL2}	Voltage Input Low (TTL)	-	-	0.8	-	0.8	V
V_{IH2}	Voltage Input High (TTL)	-	2.0	-	2.0	-	V
I_{OZ}	Tri-State Leakage	V_O = 0V or V_{DD}	-	±1	-	±50	µA
I_{IN}	Input Leakage Current	V_{IN} = V_{DD} or V_{SS}	-	±0.5	-	±5.0	µA

Figure 5: DC Characteristics

54HSC/T373 : Octal Transparent Latch, 3-State Outputs

The 54HSC/T373 is an Octal Transparent Latch with 3-State Outputs.

Inputs			Outputs
$\overline{OC}$	C	D	Q
L	H	H	H
L	H	L	L
L	L	X	Q_0
H	X	X	Z

H = high level
L = low level
X = irrelevant
Z = high impedance

Figure 1: Function Table

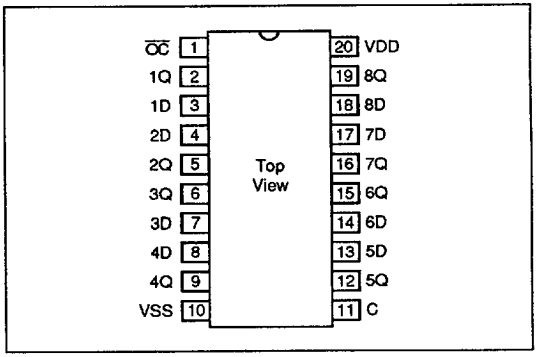


Figure 2: Pin Out

Symbol	Parameter	+25°C			-55°C / +125°C			Units
		Min.	Typ.	Max.	Min.	Typ.	Max.	
t_{PLH}	Propagation delay. Low to high output.	-	15	20	-	20	24	ns
t_{PHL}	Propagation delay. High to low output.	-	14	20	-	21	24	ns
t_{PZL}	Propagation delay. Enable to low.	-	13	25	-	14	25	ns
t_{PZH}	Propagation delay. Enable to high.	-	16	20	-	18	24	ns
t_{PLZ}	Propagation delay. Low to disable.	-	14	25	-	18	25	ns
t_{PHZ}	Propagation delay. High to disable.	-	13	25	-	19	25	ns

Figure 3: Switching Characteristics

Symbol	Parameter	Test Conditions	Limits				Units
			+25°C		-55°C / +125°C		
			Min.	Max.	Min.	Max.	
I_{DD}	Quiescent Current	V_{IN} = 0V or V_{DD}	-	20	-	600	µA
V_{OL}	Output Voltage Low Level	I_{OL} = 9mA	-	0.4	-	0.4	V
V_{OH}	Output Voltage High Level	I_{OH} = -11mA	2.5	-	2.5	-	V
V_{IL1}	Voltage Input Low (CMOS)	-	-	1.5	-	1.5	V
V_{IH1}	Voltage Input High (CMOS)	-	3.5	-	3.5	-	V
V_{IL2}	Voltage Input Low (TTL)	-	-	0.8	-	0.8	V
V_{IH2}	Voltage Input High (TTL)	-	2.0	-	2.0	-	V
I_{OZ}	Tri-State Leakage	V_O = 0V or V_{DD}	-	±1	-	±50	µA
I_{IN}	Input Leakage Current	V_{IN} = V_{DD} or V_{SS}	-	±0.5	-	±5.0	µA

Figure 4: DC Characteristics

54HSC/T373 : Octal Transparent Latch, 3-State Outputs

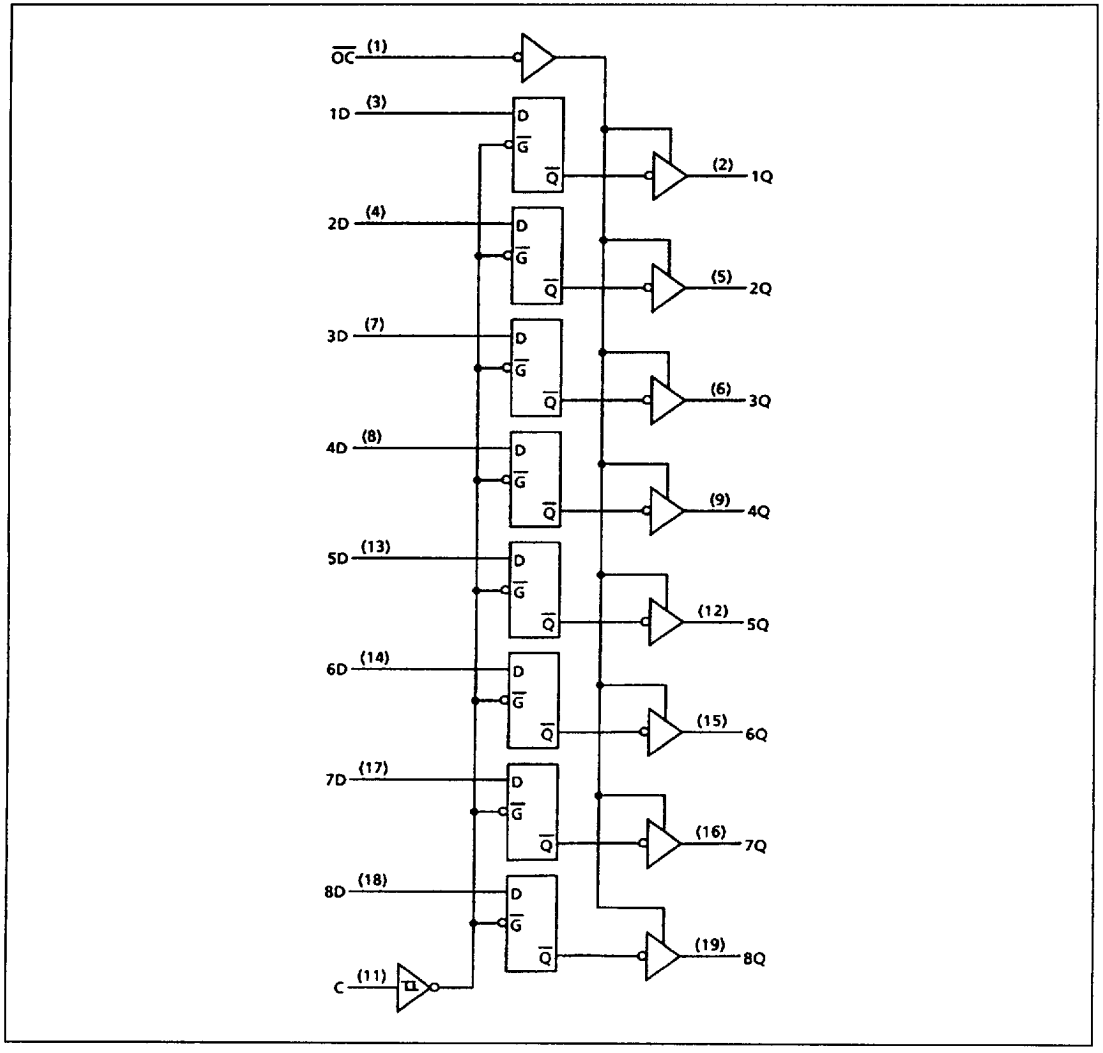


Figure 5: Logic Diagram

54HSC/T573 : Octal Transparent Latch, 3-State Outputs

The 54HSC/T573 is an Octal Transparent Latch with 3-State Outputs.

Inputs			Outputs
$\overline{OC}$	C	D	Q
L	H	H	H
L	H	L	L
L	L	X	Q_0
H	X	X	Z

H = high level
L = low level
X = irrelevant
Z = high impedance

Figure 1: Function Table

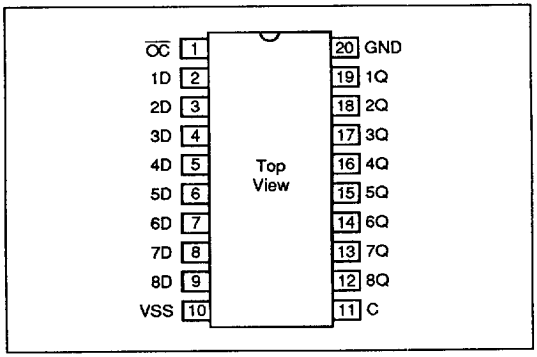


Figure 2: Pin Out

Symbol	Parameter	+25°C			-55°C / +125°C			Units
		Min.	Typ.	Max.	Min.	Typ.	Max.	
t_{PLH}	Propagation delay. Low to high output.	-	19	24	-	22	29	ns
t_{PHL}	Propagation delay. High to low output.	-	19	24	-	22	29	ns
t_{PZL}	Propagation delay. Enable to low.	-	13	21	-	16	24	ns
t_{PZH}	Propagation delay. Enable to high.	-	16	24	-	19	27	ns
t_{PLZ}	Propagation delay. Low to disable.	-	14	22	-	17	25	ns
t_{PHZ}	Propagation delay. High to disable.	-	13	21	-	16	24	ns

Figure 3: Switching Characteristics

Symbol	Parameter	Test Conditions	Limits				Units
			+25°C		-55°C / +125°C		
			Min.	Max.	Min.	Max.	
I_{DD}	Quiescent Current	V_{IN} = 0V or V_{DD}	-	20	-	600	µA
V_{OL}	Output Voltage Low Level	I_{OL} = 9mA	-	0.4	-	0.4	V
V_{OH}	Output Voltage High Level	I_{OH} = -11mA	2.5	-	2.5	-	V
V_{IL1}	Voltage Input Low (CMOS)	-	-	1.5	-	1.5	V
V_{IH1}	Voltage Input High (CMOS)	-	3.5	-	3.5	-	V
V_{IL2}	Voltage Input Low (TTL)	-	-	0.8	-	0.8	V
V_{IH2}	Voltage Input High (TTL)	-	2.0	-	2.0	-	V
I_{OZ}	Tri-State Leakage	V_O = 0V or V_{DD}	-	±1	-	±50	µA
I_{IN}	Input Leakage Current	V_{IN} = V_{DD} or V_{SS}	-	±0.5	-	±5.0	µA

Figure 4: DC Characteristics

54HSC/T573 : Octal Transparent Latch, 3-State Outputs

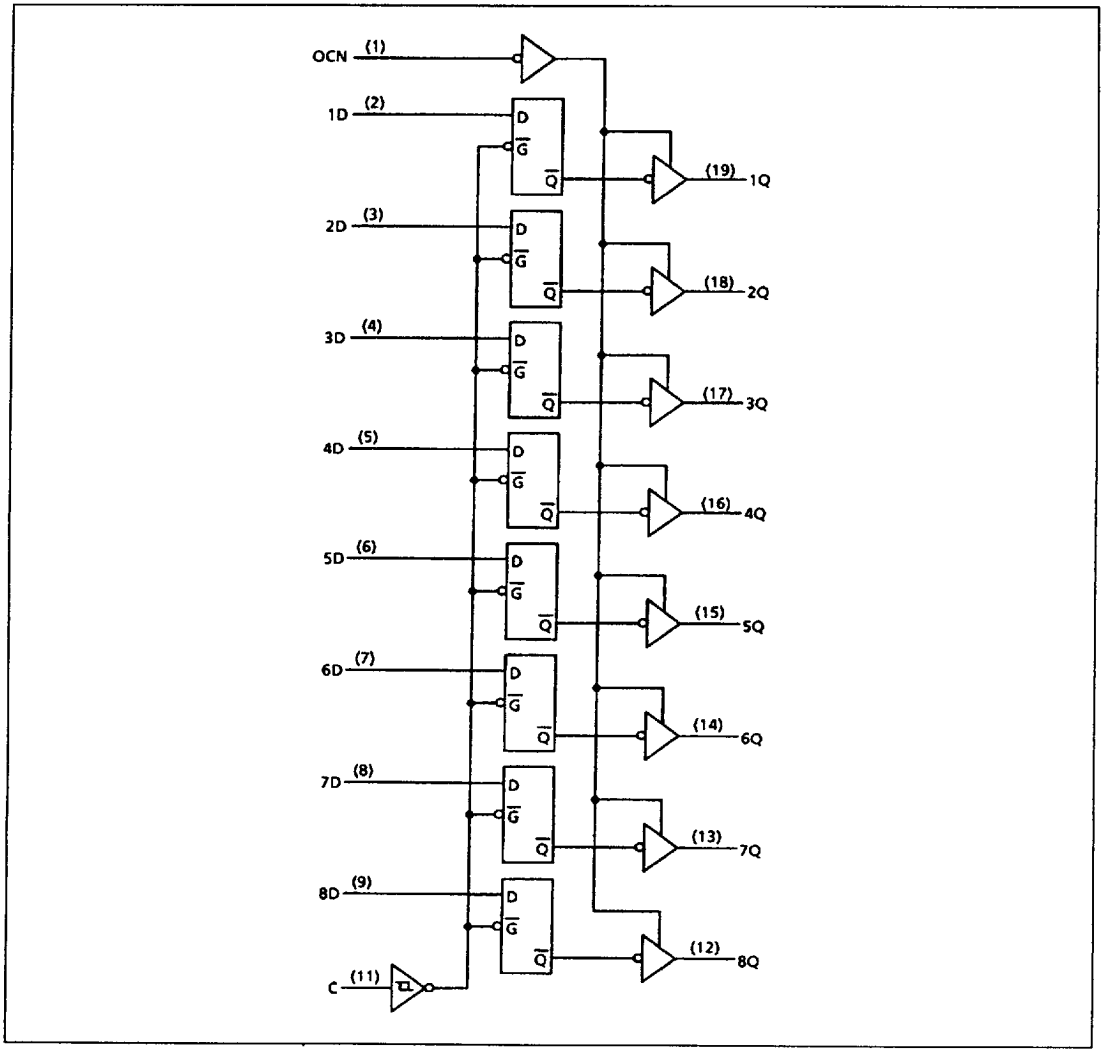


Figure 5: Logic Diagram

54HSC/T670 : 4 x 4 Register Files with Tri-State Outputs

The 54HSC/T670 is a register storing 4 words of 4 bits each. Separate on-chip decoding is provided for addressing the four word locations to either write or retrieve data. This allows simultaneous writing into one location and reading from another location.

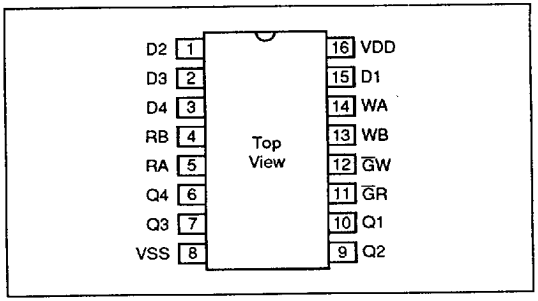


Figure 1: Pin Out

Write Inputs			Word			
WB	WA	$\overline{GW}$	1	2	3	4
L	L	L	Q = D	Q0	Q0	Q0
L	H	L	Q0	Q = D	Q0	Q0
H	L	L	Q0	Q0	Q = D	Q0
H	H	L	Q0	Q0	Q0	Q = D
X	X	H	Q0	Q0	Q0	Q0

Q0 = level of Q before inputs were established
H = high level, L = low level, X = irrelevant

Figure 2: Write Function Table

Read Inputs			Outputs			
WB	WA	$\overline{GW}$	1	2	3	4
L	L	L	W1D1	W1D2	W1D3	W1D4
L	H	L	W2D1	W2D2	W2D3	W2D4
H	L	L	W3D1	W3D2	W3D3	W3D4
H	H	L	W4D1	W4D2	W4D3	W4D4
X	X	H	Z	Z	Z	Z

H = high level, L = low level, X = irrelevant, Z = high impedance

Figure 3: Read Function Table

Symbol	Parameter	+25°C		-55°C / +125°C		Units
		Typ.	Max.	Typ.	Max.	
t_{PLH}	Propagation delay. Read select to Q.	25	30	28	33	ns
t_{PHL}	Propagation delay. Read select to Q.	18	25	21	28	ns
t_{PLH}	Propagation delay. Write enable to Q.	18	25	21	28	ns
t_{PHL}	Propagation delay. Write enable to Q.	18	25	21	28	ns
t_{PLH}	Propagation delay. Data to Q.	27	35	30	38	ns
t_{PHL}	Propagation delay. Data to Q.	23	25	26	28	ns
t_{PZH}	Propagation delay. Read Enable to Q.	18	25	21	28	ns
t_{PZL}	Propagation delay. Read Enable to Q.	18	25	21	28	ns
t_{PHZ}	Propagation delay. Read Enable to Q.	18	25	21	28	ns
t_{PLZ}	Propagation delay. Read Enable to Q.	18	25	21	28	ns

V_{CC} = 5V, T_{MAX} = +125°C, C_L = 50pF

Figure 4: Switching Characteristics

54HSC/T670 : 4 x 4 Register Files with Tri-State Outputs

Symbol	Parameter	Test Conditions	Limits				Units
			+25°C		-55°C / +125°C		
			Min.	Max.	Min.	Max.	
I_{DD}	Quiescent Current	V_{IN} = 0V or V_{DD}	-	20	-	600	µA
V_{OL}	Output Voltage Low Level	I_{OL} = 9mA	-	0.4	-	0.4	V
V_{OH}	Output Voltage High Level	I_{OH} = -11mA	2.5	-	2.5	-	V
V_{IL1}	Voltage Input Low (CMOS)	-	-	1.5	-	1.5	V
V_{IH1}	Voltage Input High (CMOS)	-	3.5	-	3.5	-	V
V_{IL2}	Voltage Input Low (TTL)	-	-	0.8	-	0.8	V
V_{IH2}	Voltage Input High (TTL)	-	2.0	-	2.0	-	V
I_{OZ}	Tri-State Leakage	V_O = 0V or V_{DD}	-	±1	-	±50	µA
I_{IN}	Input Leakage Current	V_{IN} = V_{DD} or V_{SS}	-	±0.5	-	±5.0	µA

Figure 5: DC Characteristics

54HSC/T670 : 4 x 4 Register Files with Tri-State Outputs

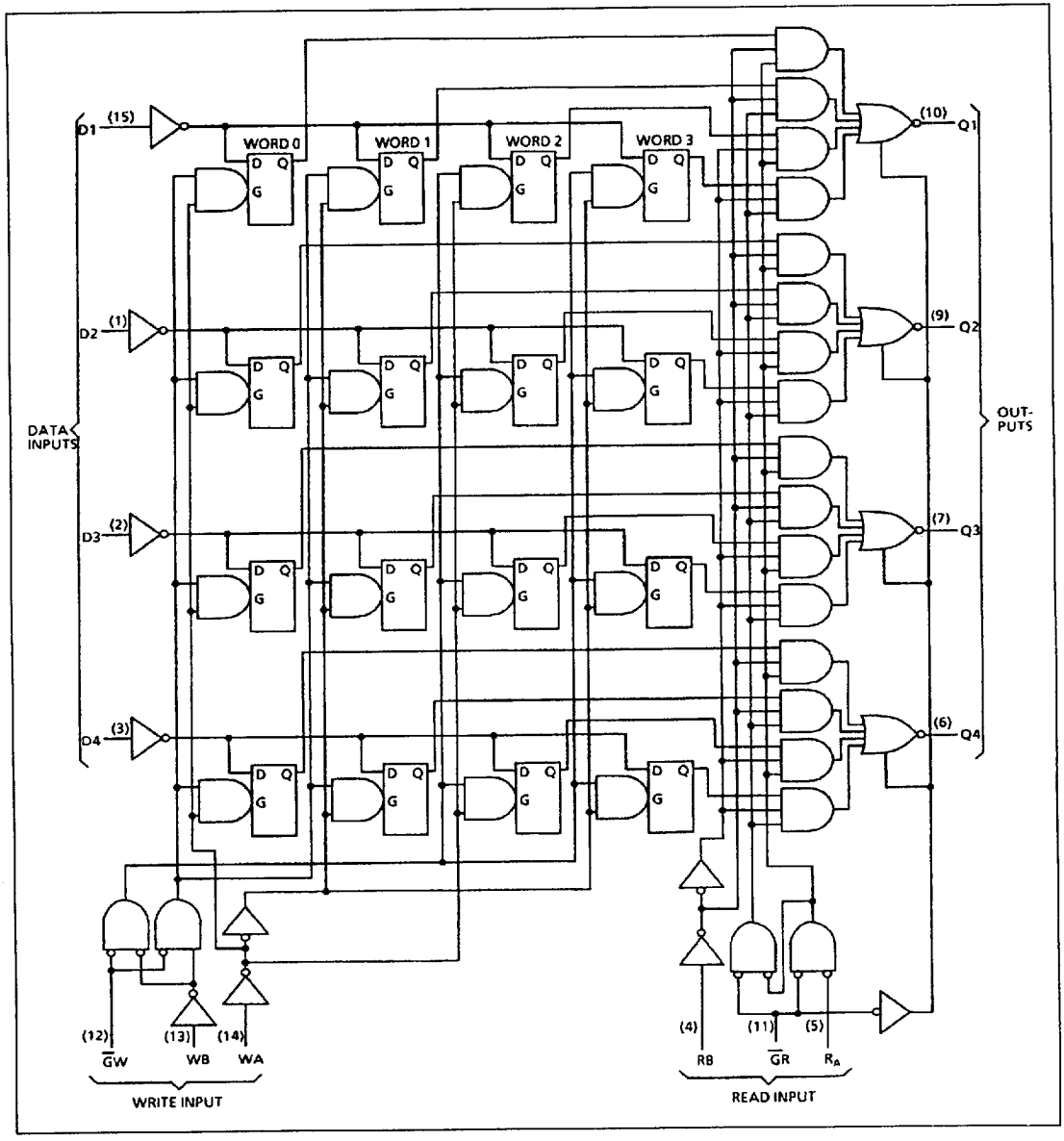


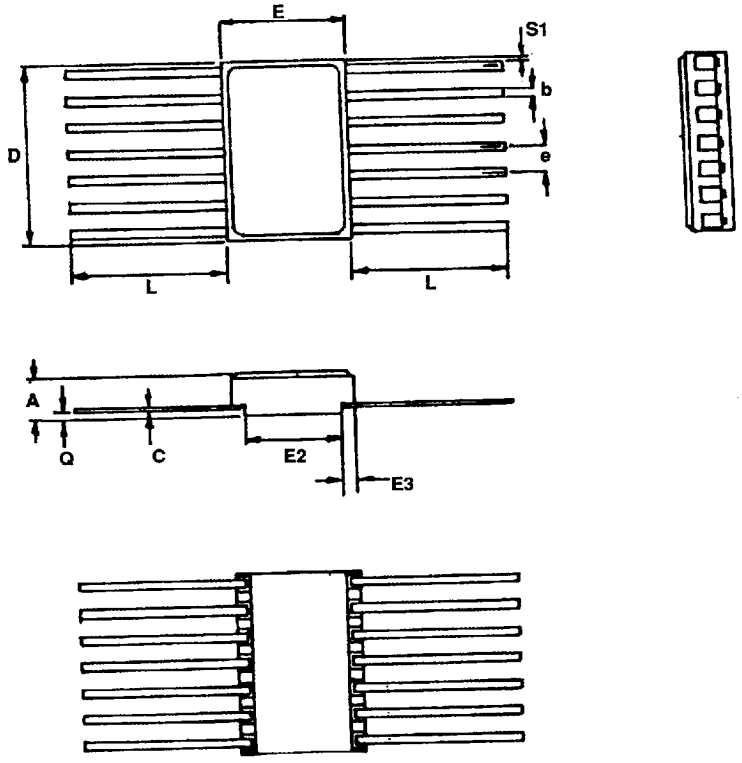
Figure 6: Logic Diagram

CHARACTERISATION DATA

Device base listing as below:

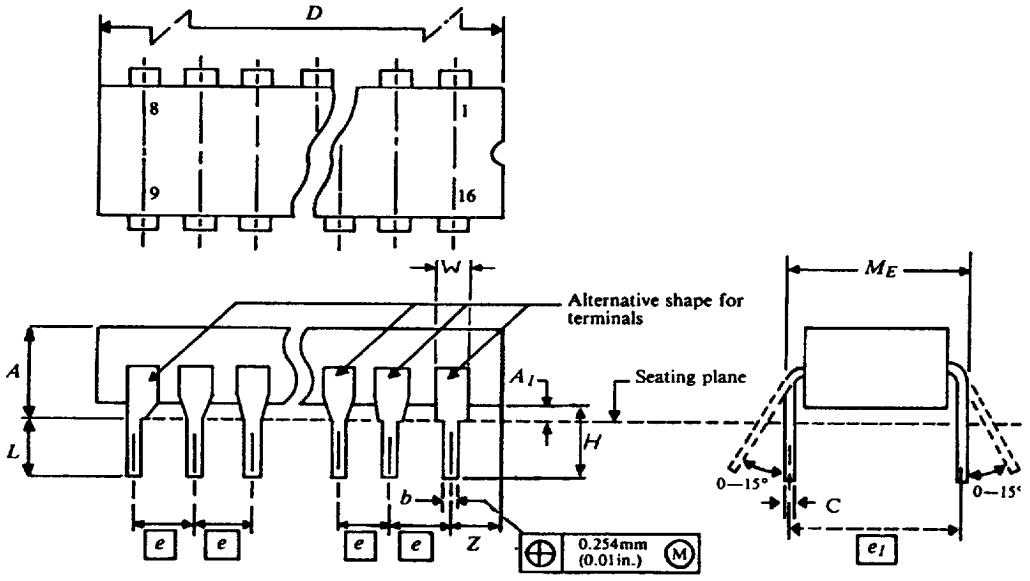
MA9003 Base	Pin Count	MA9007 Base	Pin Count	BMS011 Base	Pin Count
00	14	154	24	138	16
02	14	161	16	139	16
03	14	163	16	238	16
04	14	165	16	240	20
08	14	166	16	241	20
10	14	191	16	244	20
14	14	273	20	245	20
21	14	283	16	373	20
27	14	670	16	374	20
32	14			521	20
74	14			540	20
86	14			541	20
109	16			573	20
125	14			574	20
126	14				
148	16				
151	16				
157	16				
164	14				
253	16				

LI/AS/4/IN/02001 - 14 LEAD BOTTOMBRAZE FLATPACK (MIL-38510H)



	INCHES		
REF	MAX	NOM	MIN
A	0.105		
b	0.019		0.015
c	0.006		0.004
D	0.347		0.333
E	0.260		0.250
E2		0.175	
e		0.050	
L	0.305		0.270
Q			0.026
S1			0.005

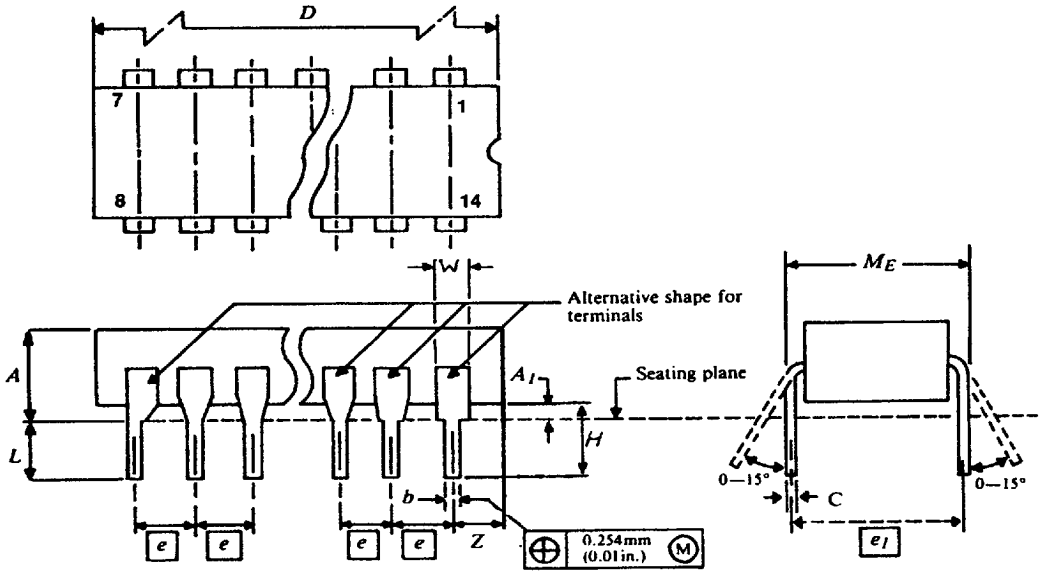
FINISHED PRODUCT OUTLINE



DIMENSION A INCLUDES ANY LID

Ref.	Millimetres			Inches		
	Min.	Nom.	Max.	Min.	Nom.	Max.
A			5.60			0.220
A_1	0.38		1.53	0.015		0.060
b	0.35		0.59	0.014		0.023
c	0.20		0.36	0.008		0.014
D			20.58			0.810
e		2.54TP			0.100TP	
e_1		7.62TP			0.300TP	
H	4.45		5.38	0.175		0.212
M_E			8.30			0.326
Z			1.27			0.050
W			1.53			0.060

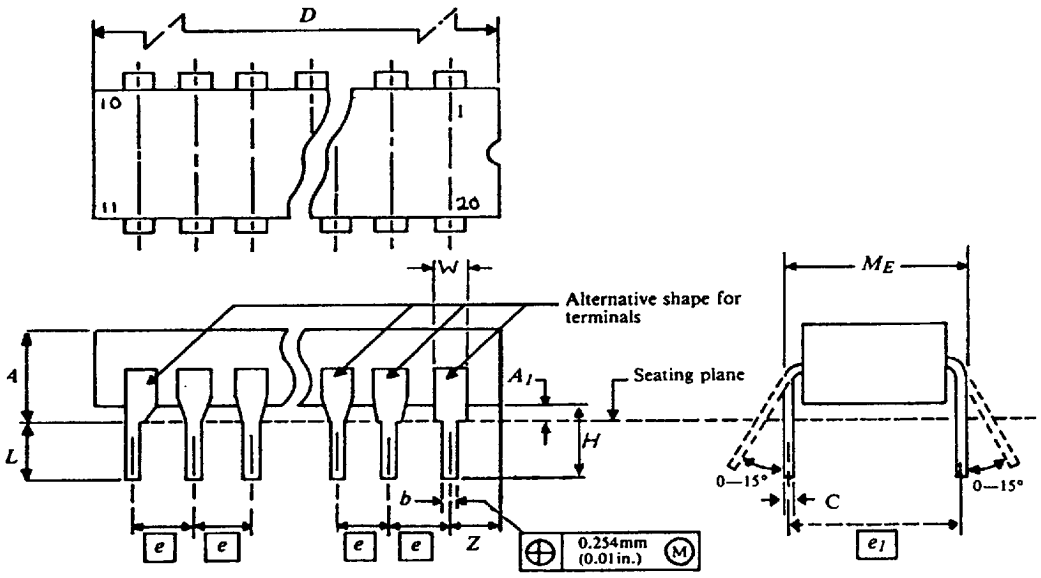
FINISHED PRODUCT OUTLINE



DIMENSION A INCLUDES ANY LID

Ref.	Millimetres			Inches		
	Min.	Nom.	Max.	Min.	Nom.	Max.
A			5.60			0.220
A_1	0.38		1.53	0.015		0.060
b	0.35		0.59	0.014		0.023
c	0.20		0.36	0.008		0.014
D			18.04			0.710
e		2.54TP			0.100TP	
e_1		7.26TP			0.300TP	
H	4.45		5.38	0.175		0.212
M_E			8.30			0.326
Z			1.27			0.050
W			1.53			0.060

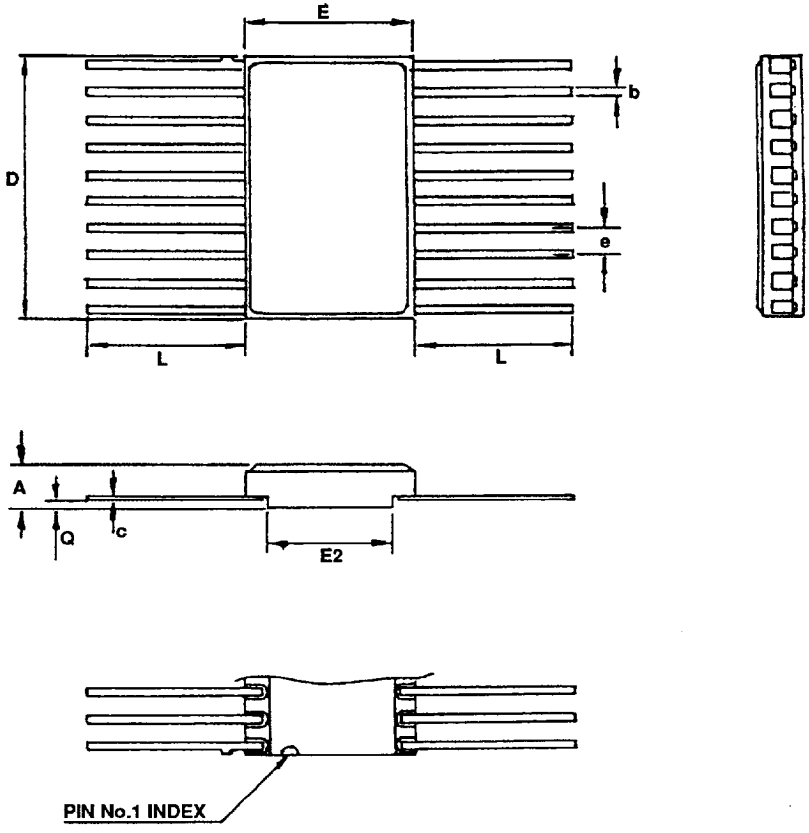
FINISHED PRODUCT OUTLINE



DIMENSION A INCLUDES ANY LID

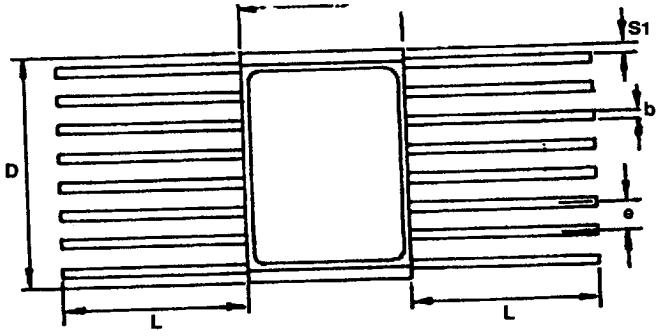
Ref.	Millimetres			Inches		
	Min.	Nom.	Max.	Min.	Nom.	Max.
A			5.60			0.220
A1	0.38		1.53	0.015		0.060
b	0.35		0.59	0.014		0.023
c	0.20		0.36	0.008		0.014
D			25.65			1.010
e		2.54TP			0.100TP	
e1		7.62TP			0.300TP	
H	4.71		5.38	0.185		0.212
ME			8.30			0.326
Z			1.27			0.050
W			1.53			0.060

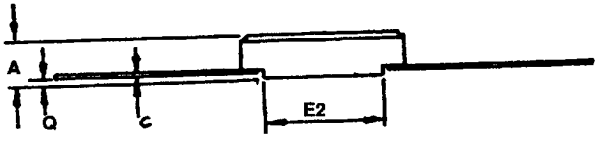
XG 527 - 20 LEAD BOTTOMBRAZE FLATPACK (MIL-STD-38510H)

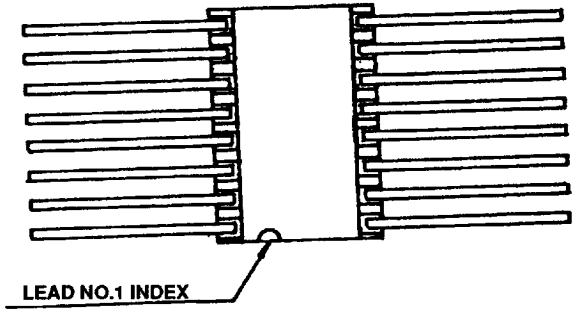


REF.	INCHES		
	MAX	NOM	MIN
A	0.106		-
b	0.019		0.015
c	0.007		0.003
D	0.490		0.470
E	0.303		0.287
E2	0.221		0.209
e	-	0.050	-
L	0.305		0.250
Q	-	-	0.026

16 LEAD BOTTOMBRAZE FLATPACK (MIL-M-38510H)



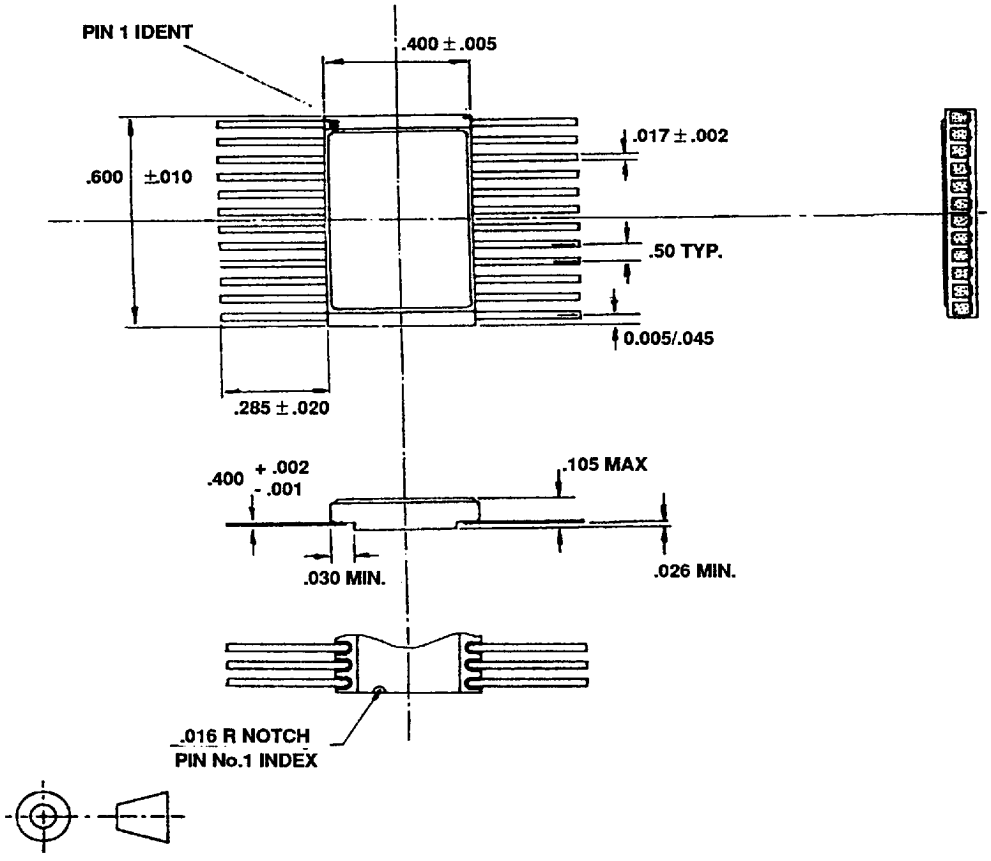




REF	INCHES		
	MAX	NOM	MIN
A	0.103		
b	0.019		0.015
c	0.006		0.004
D	0.408		0.392
E	0.276		0.264
E2	0.196		0.184
e		0.050	
L	0.305		0.250
Q			0.026
S1			0.005

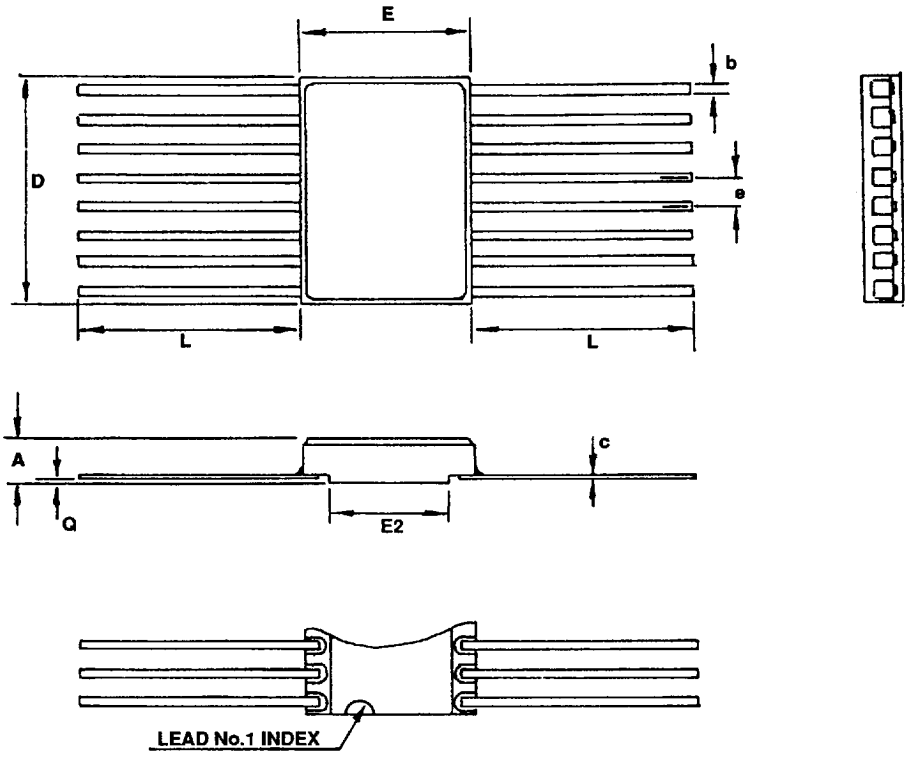
FINISHED PRODUCT OUTLINE FOR 24 LEAD CERAMIC FLATPACK (MIL-M-38510)

GPS STOCK NO - S318380

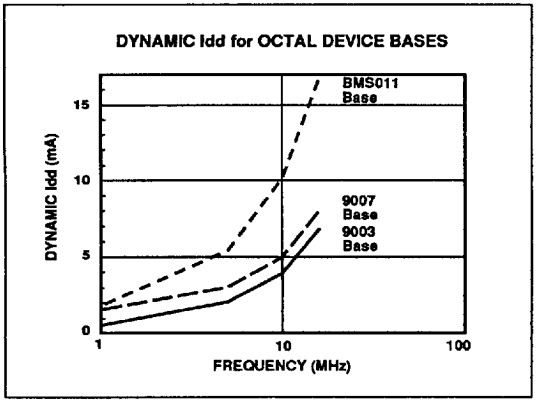


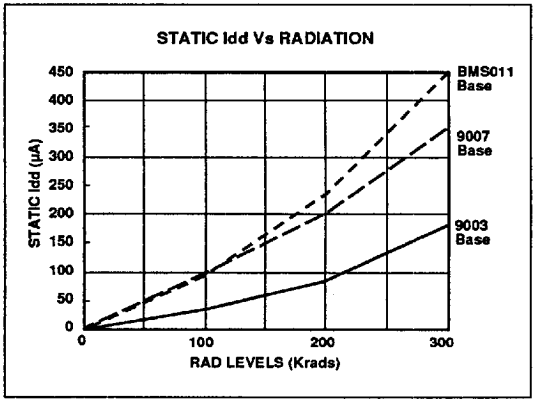
FINISHED PRODUCT OUTLINE FOR A 16 LEAD FLATPACK

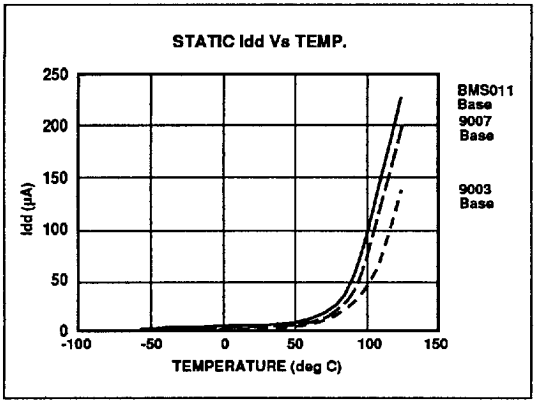
(MIL-M-38510H)

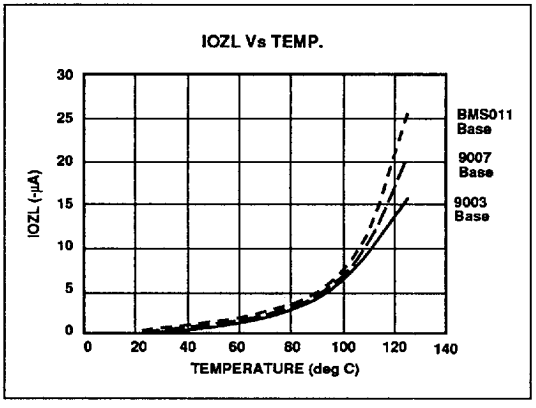


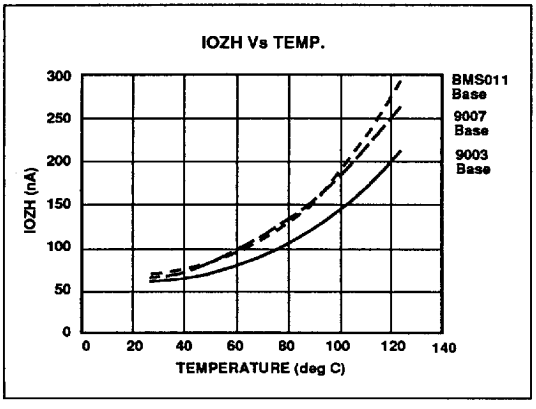
REFERENCE	INCHES		
	MAXIMUM	NOMINAL	MINIMUM
A	0.101		
b	0.019		0.015
c	0.007		0.004
D	0.418		0.402
E	0.275		0.265
E2	0.196		0.184
e		0.050	
L	0.305		0.250
Q	0.045		0.026

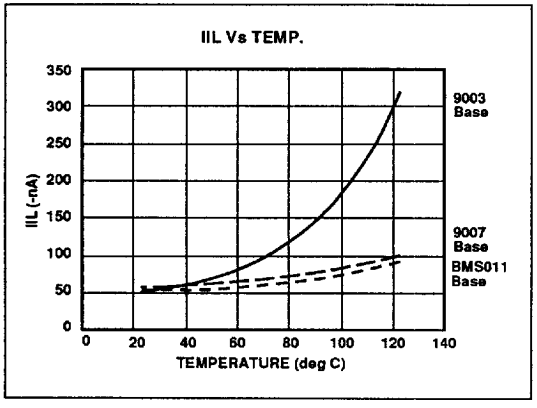


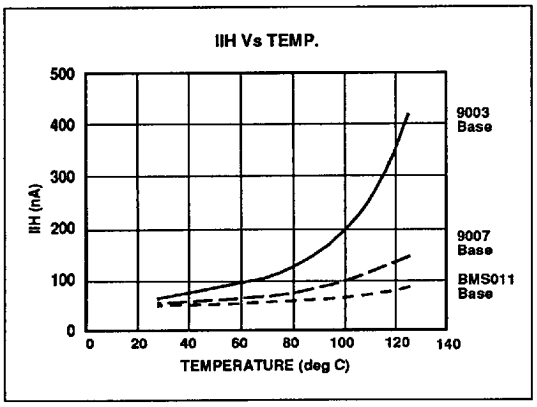


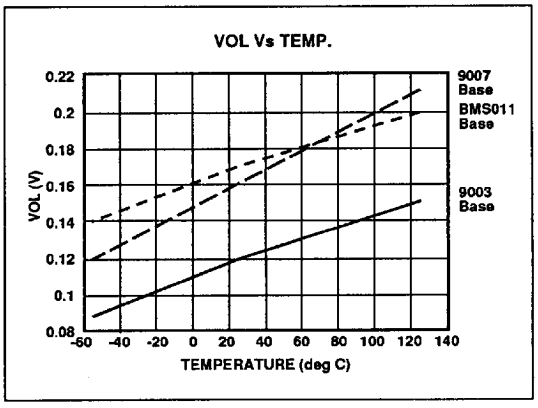


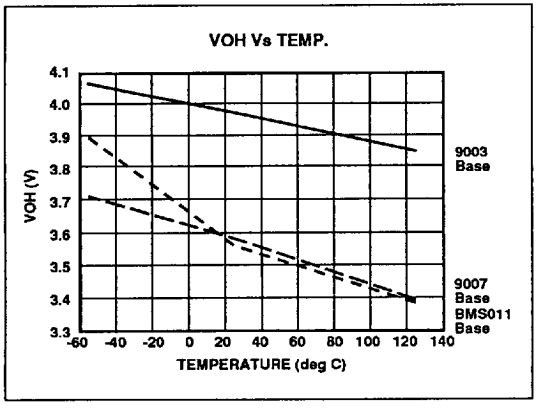


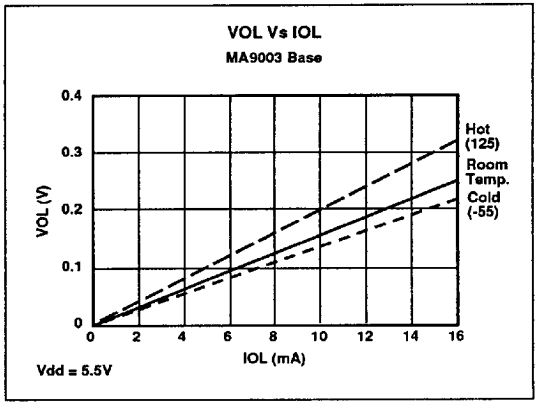


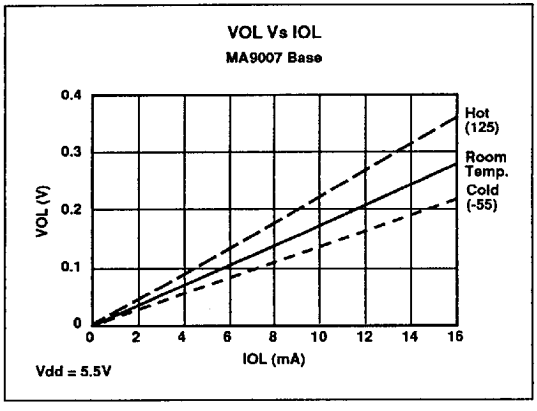


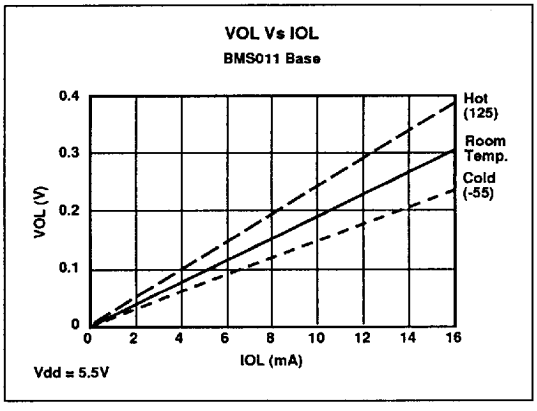


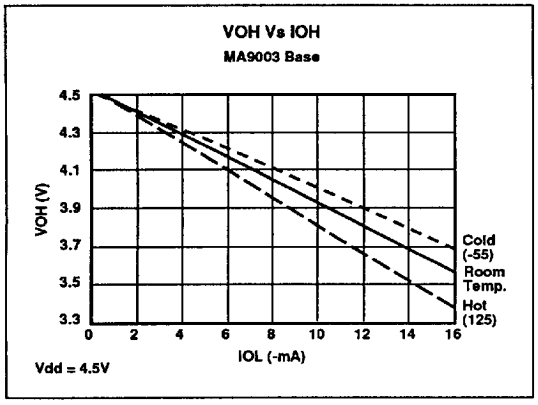


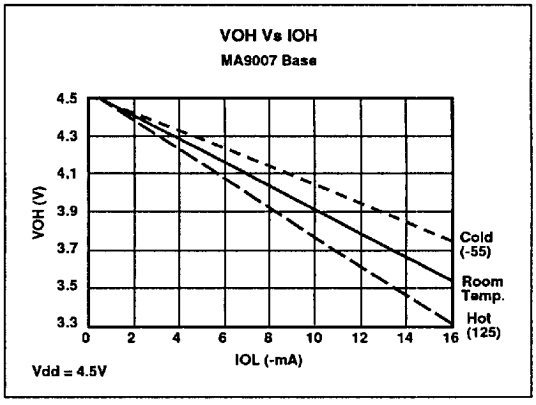


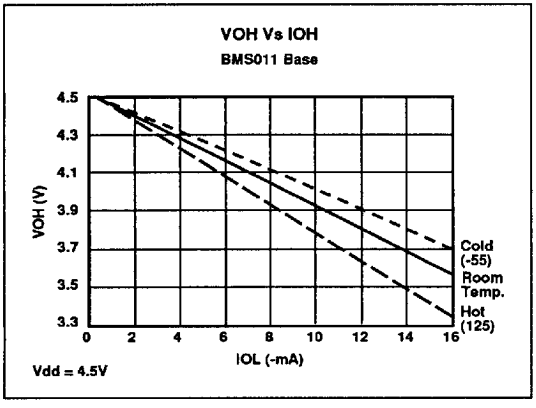


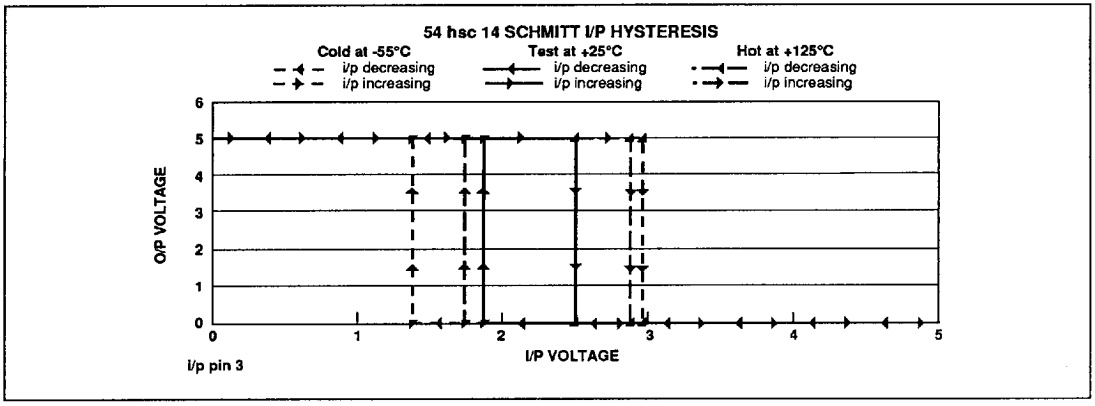


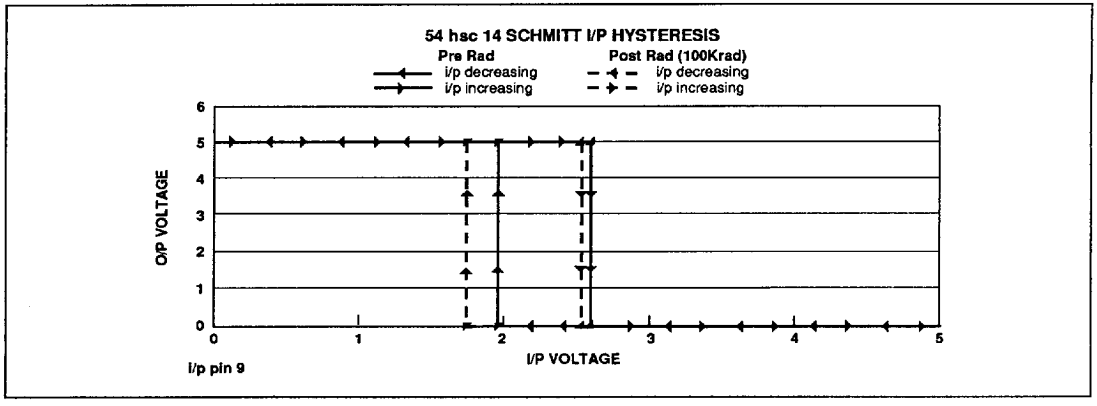












TIMING DIAGRAMS

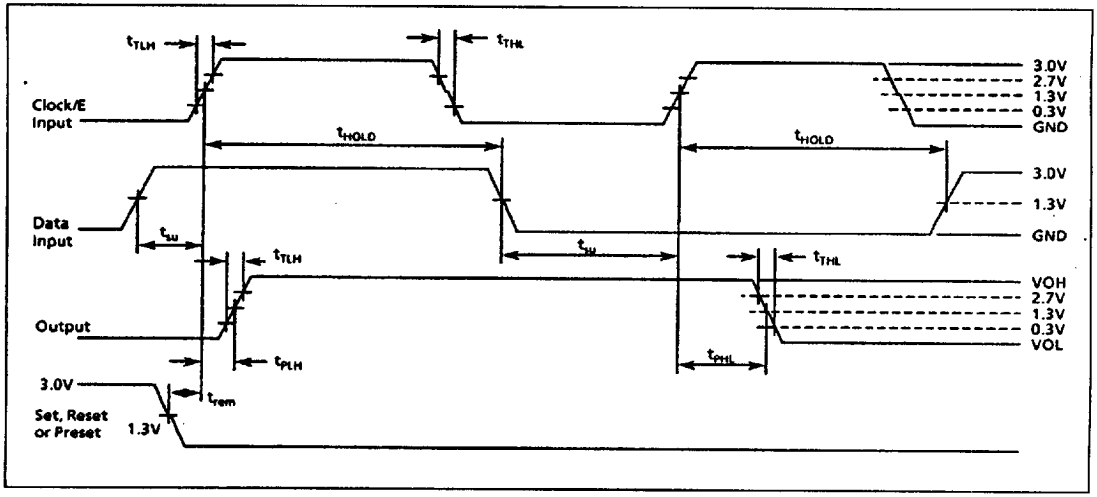


Figure 3: Set-Up Times, Hold Times, Removal Time and Propagation Delay Times

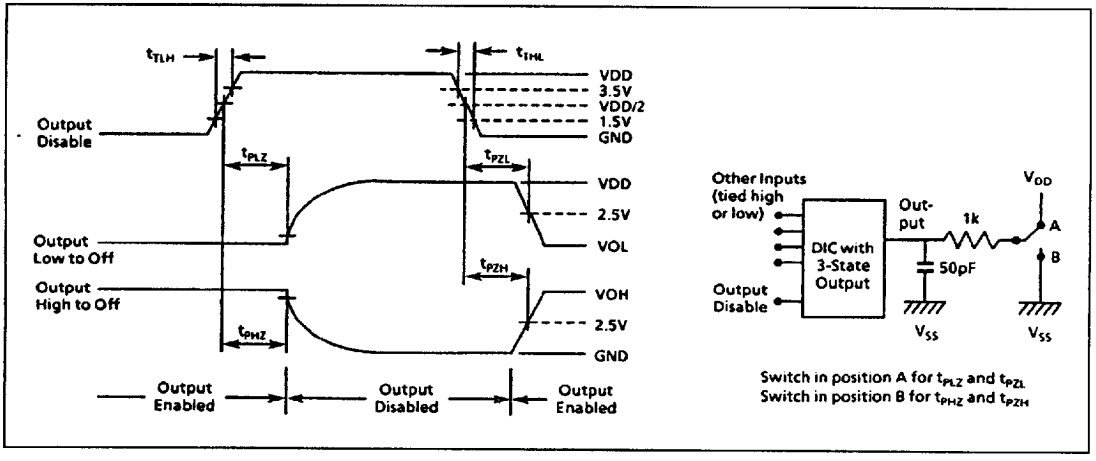


Figure 4: Three-State Propagation Delay Wave Shapes and Test Circuit

RADIATION TOLERANCE

Total Dose Radiation Testing

For product procured to guaranteed total dose radiation levels, each wafer lot will be approved when all sample devices from each lot pass the total dose radiation test.

The sample devices will be subjected to the total dose radiation level (Cobalt-60 Source), defined by the ordering code, and must continue to meet the electrical parameters specified in the data sheet. Electrical tests, pre and post irradiation, will be read and recorded.

GEC Plessey Semiconductors can provide radiation testing compliant with MIL-STD-883 test method 1019, Ionizing Radiation (Total Dose).

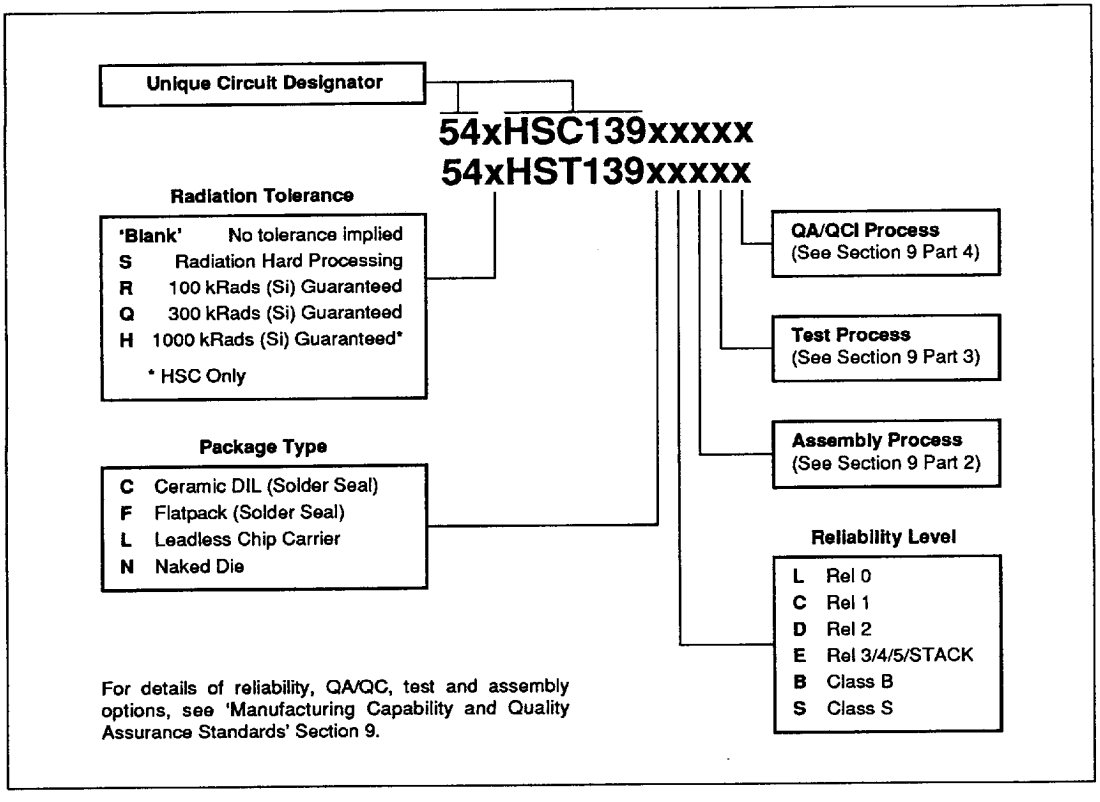
Total Dose (Function to specification)*	$3x10^5$ Rad(Si)
Transient Upset (Stored data loss)	$1x10^{11}$ Rad(Si)/sec
Transient Upset (Survivability)	$>1x10^{12}$ Rad(Si)/sec
Neutron Hardness (Function to specification)	$>1x10^{15}$ n/cm^2
Single Event Upset**	$<1x10^{-10}$ Errors/bit day
Latch Up	Not possible

* Other total dose radiation levels available on request

** Worst case galactic cosmic ray upset - interplanetary/high altitude orbit

Figure 5: Radiation Hardness Parameters

ORDERING INFORMATION



For details of reliability, QA/QC, test and assembly options, see 'Manufacturing Capability and Quality Assurance Standards' Section 9.