

54174, 54LS174, 54S174 Flip-Flops

Hex D Flip-Flops

Product Specification

Military Logic Products

FEATURES

- Six edge-triggered D-type flip-flops
- Three speed-power ranges available
- Buffered common clock
- Buffered, asynchronous Master Reset

DESCRIPTION

The 54174, 54LS174 and 54S174 have six edge-triggered D-type flip-flops with individual D inputs and Q outputs. The common buffered Clock (CP) and Master Reset (MR) inputs load and reset (clear) all flip-flops simultaneously.

The register is fully edge triggered. The state of each D input, one setup time before the Low-to-High clock transition, is transferred to the corresponding flip-flop's Q output.

All outputs will be forced Low independently of Clock or Data inputs by a Low voltage level on the MR input. The device is useful for applications where the true output only is required and the Clock and Master Reset are common to all storage elements.

ORDERING INFORMATION

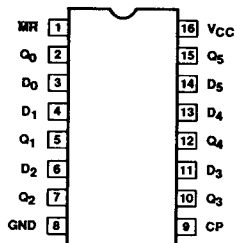
DESCRIPTION	ORDER CODE
16-Pin Ceramic DIP	54LS174/BEA, 54S174/BEA, 54174/BEA
16-Pin Ceramic FlatPack	54LS174/BFA, 54S174/BFA, 54174/BFA
16-Pin Ceramic LLCC	54LS174/B2A, 54S174/B2A

INPUT AND OUTPUT LOADING AND FAN-OUT TABLE

PINS	DESCRIPTION	54	54S	54LS
All	Inputs	1UL	1SUL	1LSUL
Q ₀ - Q ₅	Outputs	10UL	10SUL	10LSUL

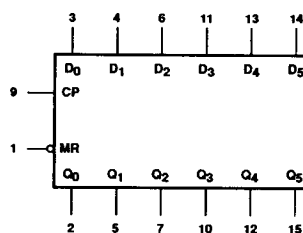
NOTE: Where a 54 Unit Load (UL) is understood to be 40 μ A I_{IH} and -1.6mA I_{IL} , a 54S Unit Load (SUL) is 50 μ A I_{IH} and -2.0mA I_{IL} , and 54LS Unit Load (LSUL) is 20 μ A I_{IH} and -0.4mA I_{IL} .

PIN CONFIGURATION



For LLCC Pin Assignments see JEDEC Standard No. 2

LOGIC SYMBOL



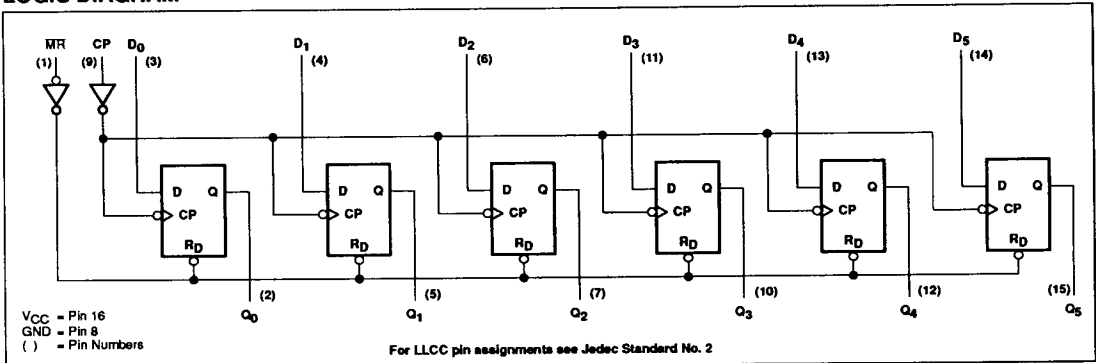
VCC = Pin 16
GND = Pin 8

For LLCC Pin Assignments see JEDEC Standard No. 2

Flip-Flops

54174, 54LS174, 54S174

LOGIC DIAGRAM



FUNCTION TABLE

OPERATING MODE	INPUTS			OUTPUTS
	MR	CP	D _n	Q _n
Reset (clear)	L	X	X	L
Load "1"	H	↑	h	H
Load "0"	H	↑	l	L

H = High voltage level steady state
h = High voltage level one setup time prior to the Low-to-High clock transition
L = Low voltage level steady state
l = Low voltage level one setup time prior to the Low-to-High clock transition
X = Don't care
↑ = Low-to-High clock transition

ABSOLUTE MAXIMUM RATINGS (Over operating free-air temperature range unless otherwise noted.)

SYMBOL	PARAMETER	54	54LS	54S	UNIT
V _{CC}	Supply voltage	7.0	7.0	7.0	V
V _I	Input voltage range	-0.5 to +5.5	-0.5 to +7.0	-0.5 to +7.0	V
I _I	Input current range	-30 to +5	-30 to +1	-30 to +5	mA
V _O	Voltage applied to output in High output state range	-0.5 to +V _{CC}	-0.5 to +V _{CC}	-0.5 to +V _{CC}	V
T _{STG}	Storage temperature range	-65 to +150			°C

RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	54			54LS			54S			UNIT
		Min	Nom	Max	Min	Nom	Max	Min	Nom	Max	
V _{CC}	Supply voltage	4.5	5.0	5.5	4.5	5.0	5.5	4.5	5.0	5.5	V
V _{IH}	High-level input voltage	2.0			2.0			2.0			V
V _{IL}	Low-level input voltage			+0.8			+0.7			+0.8	V
I _{IK}	Input clamp current			-12			-18			-18	mA
I _{OH}	High-level output current			-800			-400			-1000	μA
I _{OL}	Low-level output current			16			4			20	mA
T _A	Operating free-air temperature range	-55		+125	-55		+125	-55		+125	°C

Flip-Flops

54174, 54LS174, 54S174

DC ELECTRICAL CHARACTERISTICS (Over recommended operating free-air temperature range unless otherwise noted.)

SYMBOL	PARAMETER	TEST CONDITIONS ¹	54174			54LS174			54S174			UNIT
			Min	Typ ²	Max	Min	Typ ²	Max	Min	Typ ²	Max	
V _{OH}	High-level output voltage	V _{CC} = Min, V _{IH} = Min, V _{IL} = Max, I _{OH} = Max	2.4	3.4		2.5	3.4		2.5	3.4		V
V _{OL}	Low-level output voltage	V _{CC} = Min, I _{OL} = Max V _{IH} = Min, V _{IL} = Max		0.2	0.4		0.25	0.4			0.5	V
V _{IK}	Input clamp voltage	V _{CC} = Min, I _I = I _{IK}			-1.5			-1.5			-1.2	V
I _{IH2}	Input current at maximum input voltage	V _{CC} = Max V _I = 5.5V			1.0						1.0	mA
		V _I = 7.0V						0.1				mA
I _{IH1}	High-level input current	V _{CC} = Max V _I = 2.4V			40							μA
		V _I = 2.7V						20			50	μA
I _{IL}	Low-level input current	V _{CC} = Max V _I = 0.4V			-1.6			-0.4				mA
		V _I = 0.5V									-2.0	mA
I _{OS}	Short-circuit output current ³	V _{CC} = Max	-20		-57	-20		-100	-40		-110	mA
I _{CC}	Supply current ⁴ (total)	V _{CC} = Max		45	65		16	26		90	144	mA

AC ELECTRICAL CHARACTERISTICS T_A = 25°C, V_{CC} = 5.0V

SYMBOL	PARAMETER	TEST CONDITIONS	54 ⁵		54LS ⁵		54S		UNIT
			C _L = 15pF		C _L = 15pF		C _L = 15pF		
			Min	Max	Min	Max	Min	Max	
f _{MAX}	Maximum clock frequency	Waveform 1	25		30		75		MHz
t _{PLH}	Propagation delay	Waveform 1		30		30		13	ns
t _{PHL}	Clock to output			35		30		17	ns
t _{PHL}	Propagation <u>MR</u> delay to output	Waveform 3		35		35		22	ns

AC SETUP REQUIREMENTS T_A = 25°C, V_{CC} = 5.0V

SYMBOL	PARAMETER	TEST CONDITIONS	54		54LS		54S		UNIT
			Min	Max	Min	Max	Min	Max	
t _{w(L)}	Clock pulse width (Low)	Waveform 1	20		20		7.0		ns
t _w	Master Reset pulse width	Waveform 3	20		20		10		ns
t _s	Setup time, data to CP	Waveform 2	20		20		5.0		ns
t _h	Hold time, data to CP	Waveform 2	5		5		3.0		ns
t _{rec}	Recovery time, MR to CP	Waveform 3	25		25		5.0		ns

AC ELECTRICAL CHARACTERISTICS T_A = 25°C, V_{CC} = 5.0V

SYMBOL	PARAMETER	TEST CONDITIONS	54		54LS		54S ⁵		UNIT
			C _L = 50pF		C _L = 50pF		C _L = 50pF		
			Min	Max	Min	Max	Min	Max	
f _{MAX}	Maximum clock frequency	Waveform 1	25		30		75		MHz
t _{PLH}	Propagation delay	Waveform 1		34		35		14.0	ns
t _{PHL}	Clock to output			39		35		19.0	ns
t _{PHL}	Propagation MR delay to output	Waveform 3		39		40		24.0	ns

Flip-Flops

54174, 54LS174, 54S174

AC ELECTRICAL CHARACTERISTICS $T_A = -55^\circ\text{C}$ and $+125^\circ\text{C}$, $V_{CC} = 5.0\text{V}^5$

SYMBOL	PARAMETER	TEST CONDITIONS	54		54LS		54S		UNIT
			$C_L = 50\text{pF}$		$C_L = 50\text{pF}$		$C_L = 50\text{pF}$		
			Min	Max	Min	Max	Min	Max	
f_{MAX}	Maximum clock frequency	Waveform 1	25		30		55		MHz
t_{PLH}	Propagation delay	Waveform 1		44		46		17	ns
t_{PHL}	Clock to output			51		46		23	ns
t_{PHL}	Propagation MR delay to output	Waveform 3		51		52		29	ns

AC SETUP REQUIREMENTS $T_A = -55^\circ\text{C}$ and $+125^\circ\text{C}$, $V_{CC} = 5.0\text{V}^5$

SYMBOL	PARAMETER	TEST CONDITIONS	54		54LS		54S		UNIT
			Min	Max	Min	Max	Min	Max	
$t_w(L)$	Clock pulse width (Low)	Waveform 1	20		30		10		ns
t_w	Master Reset pulse width	Waveform 3	30		35		10		ns
t_s	Setup time, data to CP	Waveform 2	25		20		7		ns
t_h	Hold time, data to CP	Waveform 2	5		5		5		ns
t_{rec}	Recovery time, MR to CP	Waveform 3	30		25		7		ns

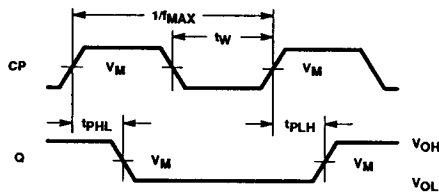
NOTES:

1. For conditions shown as Min or Max, use the appropriate value specified under recommended operating conditions for the applicable type and function table operating mode.
2. All typical values are at $V_{CC} = 5\text{V}$, $T_A = 25^\circ\text{C}$.
3. Not more than one output should be shorted at a time and duration of the short circuit should not exceed one second.
4. I_{CC} is measured after a momentary ground, then $\geq 4.0\text{V}$ is applied to Clock, with $\geq 4.0\text{V}$ applied to all Data and MR inputs and all outputs open.
5. These parameters are guaranteed, but not tested.

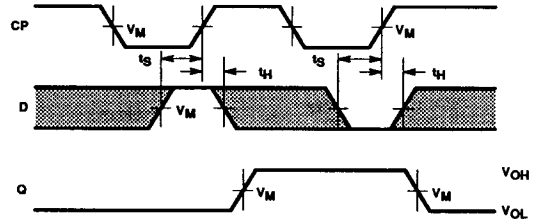
Flip-Flops

54174, 54LS174, 54S174

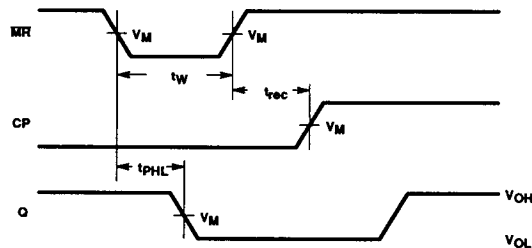
AC WAVEFORMS



Waveform 1. Clock to Output Delays and Clock Pulse Width



Waveform 2. Data Setup and Hold Times



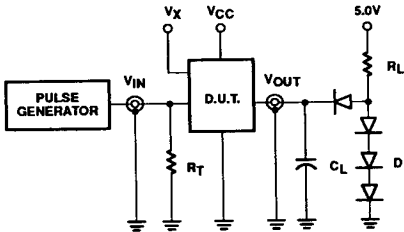
Waveform 3. Master Reset to Output Delay, Master Reset Pulse Width, and Master Reset Recovery Time

NOTE: For all waveforms $V_M = 1.5V$ for 54 and 54S; $V_M = 1.3V$ for 54LS
The shaded areas indicate when the input is permitted to change for predictable output performance.

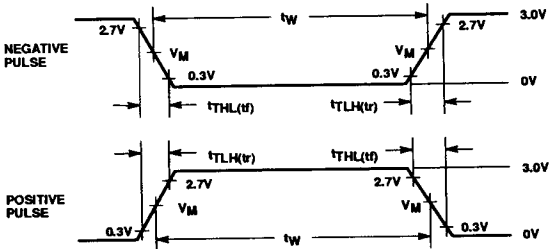
Flip-Flops

54174, 54LS174, 54S174

TEST CIRCUIT AND WAVEFORM



Test Circuit for 54 Totem-Pole Outputs



Input Pulse Definition

FAMILY	INPUT PULSE CHARACTERISTICS					
	RL	VM	Rep. Rate	Tw	TLH	TTHL
54LSXXX	2.0kΩ	1.3V	1MHz	500ns	≤15ns	≤6ns
54XXX	400Ω	1.5V	1MHz	500ns	≤7ns	≤7ns
54SXXX	280Ω	1.5V	1MHz	500ns	≤2.5ns	≤2.5ns

DEFINITIONS:

- CL = Load capacitance includes jig and probe capacitance; see AC Characteristics for value.
RT = Termination resistance should be equal to ZOUT of Pulse Generators.
D = Diodes are 1N916, 1N3064, or equivalent.
VX = Unlocked pins must be held at ≤0.8V, ≥2.7V or open per Function Table.