**NE/SE5539** 

## **DESCRIPTION**

The NE/SE5539 is a very wide bandwidth, high slew rate, monolithic operational amplifier for use in video amplifiers, RF amplifiers, and extremely high slew rate amplifiers.

Emitter-follower inputs provide a true differential input impedance device. Proper external compensation will allow design operation over a wide range of closed-loop gains, both inverting and non-inverting, to meet specific design requirements.

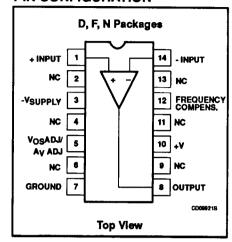
## **FEATURES**

- Bandwidth
  - Unity gain 350MHz
  - Full power 48MHz
- GBW 1.2GHz at 17dB
- Slew rate: 600/Vµs
- A<sub>VOL</sub>: 52dB typical
- Low noise 4nV√Hz typical
- MIL-STD processing available

### **APPLICATIONS**

- High speed datacom
- Video monitors & TV
- Satellite communications
- Image processing
- RF instrumentation & oscillators
- Magnetic storage
- Military communications

### **PIN CONFIGURATION**



# **ORDERING INFORMATION**

DESCRIPTION	TEMPERATURE RANGE	ORDER CODE	DWG#
14-Pin Plastic DIP	0 to +70°C	NE5539N	0405
14-Pin Plastic SO	0 to +70°C	NE5539D	0175
14-Pin Cerdip	0 to +70°C	NE5539F	0581
14-Pin Cerdip	-55 to +125°C	SE5539F	0581

## **ABSOLUTE MAXIMUM RATINGS<sup>1</sup>**

SYMBOL	PARAMETER	RATING	UNITS
Vcc	Supply voltage	±12	V
P <sub>DMAX</sub>	Maximum power dissipation,  T <sub>A</sub> = 25°C (still-air) <sup>2</sup> F package  N package  D package	1.17 1.45 0.99	W W W
TA	Operating temperature range NE SE	0 to 70 -55 to +125	တို
T <sub>STG</sub>	Storage temperature range	-65 to +150	°C
Tj	Max junction temperature	150	~℃
T <sub>SOLD</sub>	Lead soldering temperature (10sec max)	+300	°C

#### NOTES:

- Differential input voltage should not exceed 0.25V to prevent excesive input bias current and common-mode voltage 2.5V. These voltage limits may be exceeded if current is limited to less than 10mA.
- 2. Derate above 25°C, at the following rates:

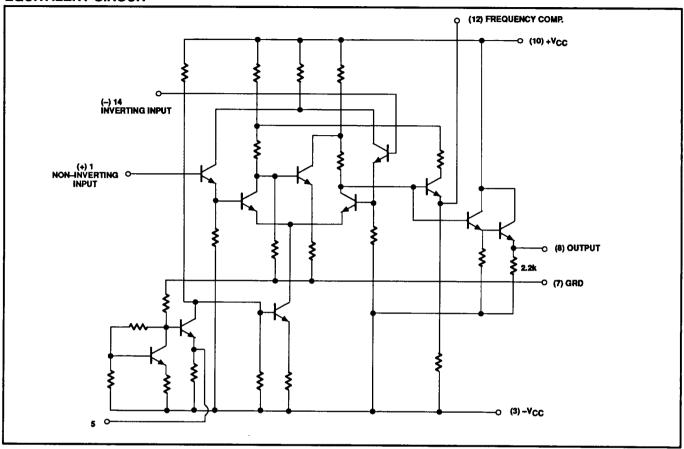
F package at 9.3mW/°C

N package at 11.6mW/°C

D package at 7.9mW/°C

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# **EQUIVALENT CIRCUIT**



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## DC ELECTRICAL CHARACTERISTICS

 $V_{CC} = \pm 8V$ ,  $T_A = 25$ °C; unless otherwise specified.

					SE5539			NE5539		
SYMBOL	PARAMETER	TEST CONDITIO	NS	MIN	ТҮР	MAX	MIN TYP MAX		MAX	UNITS
V <sub>OUT</sub>	Output voltage swing	$R_L = 150\Omega$ to GND and 470 $\Omega$ to -V <sub>CC</sub>	+Swing -Swing				+2.3 -1.7	+2.7 -2.2		٧
V <sub>out</sub>	Output voltage swing	$R_L = 25\Omega$ to GND Over temp	+Swing -Swing	+2.3 -1.5	+3.0 -2.1			<u> </u>	•	V
		$R_L = 25\Omega$ to GND $T_A = 25^{\circ}C$	+Swing -Swing	+2.5 -2.0	+3.1 -2.7					V
I <sub>CC+</sub>	Positive supply current	V <sub>O</sub> = 0, R <sub>1</sub> = ∞, Ove	r temp		14	18		2.8	3.5	mA
		$V_0 = 0, R_1 = \infty, T_A = \infty$	= 25°C		14	17		14	18	mA
I <sub>CC</sub> -	Negative supply current	V <sub>O</sub> = 0, R <sub>1</sub> = ∞, Ove	r temp		11	15		2.8	3.5	mA
		V <sub>O</sub> = 0, R <sub>1</sub> = ∞, T <sub>A</sub> :	= 25°C		11	14		11	15	mÁ
PSRR	Power supply rejection ratio	$\Delta V_{CC} = \pm 1 V$ , Over	temp		300	1000				μ٧/٧
		$\Delta V_{CC} = \pm 1 V$ , $T_A =$	25°C					200	1000	μ٧/٧
A <sub>VOL</sub>	Large signal voltage gain	$V_0 = +2.3V, -1.7V, R_L = GND, 470\Omega$ to -\	= 150Ω to / <sub>CC</sub>				47	52	57	dB
Avol	Large signal voltage gain	V <sub>O</sub> = +2.3V, -1.7V	Over temp							dB
		$R_L = 2\Omega$ to GND	T <sub>A</sub> = 25°C				47	52	57	1
A <sub>VOL</sub>	Large signal voltage gain	V <sub>O</sub> = +2.5V, -2.0V	Over temp	46		60			•	dB
		$R_L = 2\Omega$ to GND	T <sub>A</sub> = 25°C	48	53	58				

# DC ELECTRICAL CHARACTERISTICS

 $V_{CC} = \pm 6V$ ,  $T_A = 25$ °C; unless otherwise specified.

						SE5539		
SYMBOL	PARAMETER	TEST CONDITIONS			MIN	ТҮР	MAX	UNITS
Vos	Input offset voltage			Over temp		2	5	mV
				T <sub>A</sub> = 25°C		2	3	}
los	Input offset current			Over temp		0.1	3	μА
				T <sub>A</sub> = 25°C		0.1	1	
lΒ	Input bias current			Over temp	Î	5	20	μА
				T <sub>A</sub> = 25°C		4	10	
CMRR	Common-mode rejection ratio	$V_{CM} = \pm 1$ .	3V, R <sub>S</sub> = 10	00Ω	70	85		dB
lcc+	Positive supply current			Over temp		11	14	mA
				T <sub>A</sub> = 25°C		11	13	
1 <sub>CC</sub> -	Negative supply current			Over temp		8	11	mA
				T <sub>A</sub> = 25°CmA		8	10	
PSRR	Power supply rejection ratio	$\Delta V_{CC} = \pm 1V$		Over temp		300	1000	μV/V
				T <sub>A</sub> = 25°C				
			Over	+Swing	+1.4	+2.0		
Vout	Output voltage swing	$R_L = 150\Omega$ to GND	temp	-Swing	-1.1	-1.7	ſ	V
		and 390Ω to -V <sub>CC</sub>	T <sub>A</sub> =	+Swing	+1.5	+2.0		
			25°C	-Swing	-1.4	-1.8		

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# **AC ELECTRICAL CHARACTERISTICS**

 $V_{CC} = \pm 8V$ ,  $R_L = 150\Omega$  to GND and  $470\Omega$  to  $-V_{CC}$ , unless otherwise specified.

SYMBOL				SE5539			NE5539		
	PARAMETER	TEST CONDITIONS	MIN	ТҮР	MAX	MIN	ТҮР	MAX	UNITS
BW	Gain bandwidth product	A <sub>CL</sub> = 7, V <sub>O</sub> = 0.1 V <sub>P-P</sub>	<del>   </del>	1200			1200		MHz
	Small signal bandwidth	$A_{CL} = 2$ , $R_{L} = 150\Omega^{1}$		110			110		MHz
ts	Settling time	$A_{CL} = 2$ , $R_{L} = 150\Omega^{1}$		15			15		ns
SR	Slew rate	$A_{CL} = 2$ , $R_{L} = 150\Omega^{1}$		600			600		V/µs
<b>t</b> PD	Propagation delay	$A_{CL} = 2$ , $R_L = 150\Omega^1$		7			7		ns
	Full power response	$A_{CL} = 2$ , $R_{L} = 150\Omega^{1}$		48			48		MHz
	Full power response	$A_V = 7$ , $R_L = 150\Omega^1$	<u> </u>	20			20		MHz
	Input noise voltage	$R_S = 50\Omega$ , 1MHz		4	<b>†</b> — — —		4		nV/√Hz
	Input noise current	1MHz		6			6		pA/√Hz

### **NOTES:**

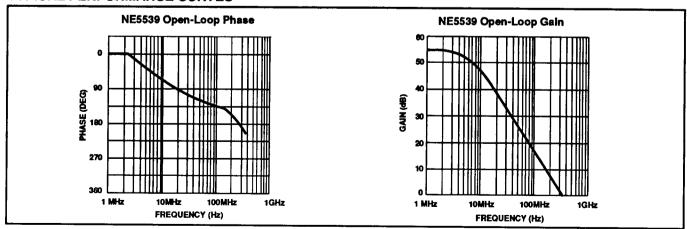
# **AC ELECTRICAL CHARACTERISTICS**

 $V_{CC}$  =  $\pm 6 \text{V},\, R_L$  =  $150 \Omega$  to GND and  $390 \Omega$  to -V  $_{CC},\,$  unless otherwise specified.

SYMBOL				SE5539		
	PARAMETER	TEST CONDITIONS	MIN	ТҮР	MAX	UNITS
BW	Gain bandwidth product	A <sub>CL</sub> = 7		700		MHz
	Small signal bandwidth	A <sub>CL</sub> = 2 <sup>1</sup>		120		MHz
ts	Settling time	A <sub>CL</sub> = 2 <sup>1</sup>		23		ns
SR	Slew rate	A <sub>CL</sub> = 2 <sup>1</sup>		330	<u></u>	V/µs
t <sub>PD</sub>	Propagation delay	A <sub>CL</sub> = 2 <sup>1</sup>	1	4.5		ns
	Full power response	A <sub>CL</sub> = 2 <sup>1</sup>	<b>†</b>	20		MHz

#### **NOTES:**

# **TYPICAL PERFORMANCE CURVES**

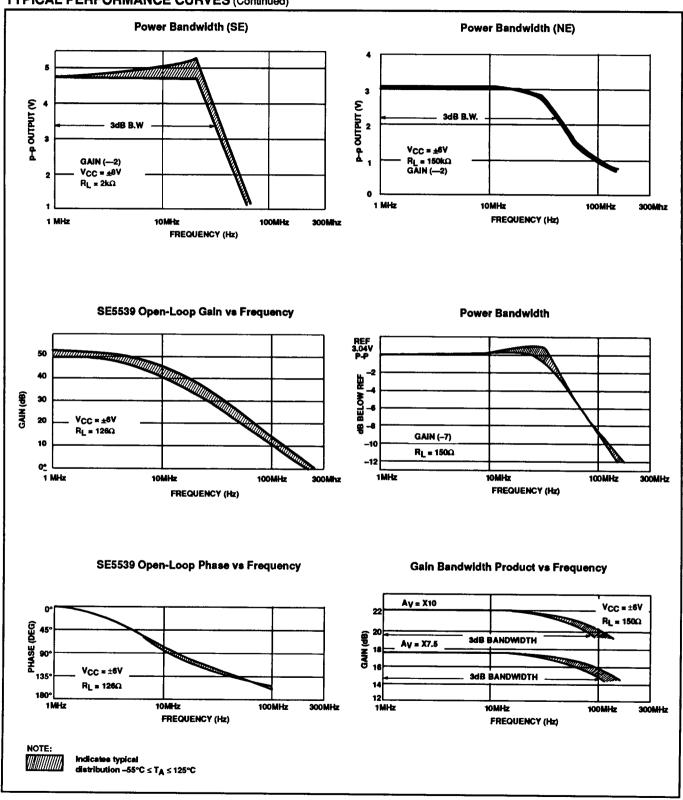


<sup>1.</sup> External compensation.

<sup>1.</sup> External compensation.

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# TYPICAL PERFORMANCE CURVES (Continued)



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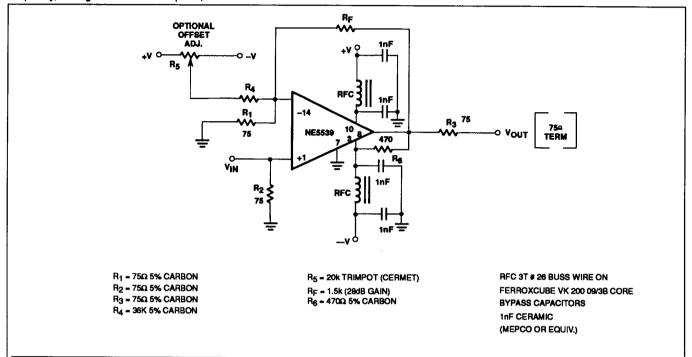
# CIRCUIT LAYOUT CONSIDERATIONS

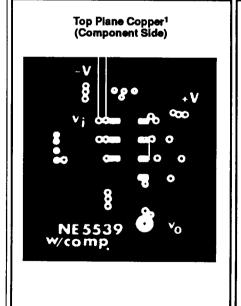
As may be expected for an ultra-high frequency, wide-gain bandwidth amplifier, the

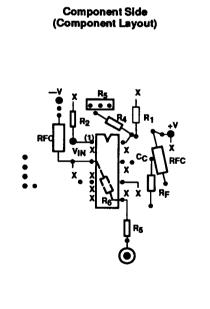
physical circuit is extremely critical.

Bread-boarding is not recommended. A
double-sided copper-clad printed circuit board

will result in more favorable system operation. An example utilizing a 28dB non-inverting amp is shown in 1.







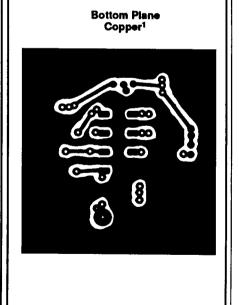


Figure 1. 28dB Non-Inverting Amp Sample PC Layout

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# NE5539 COLOR VIDEO AMPLIFIER

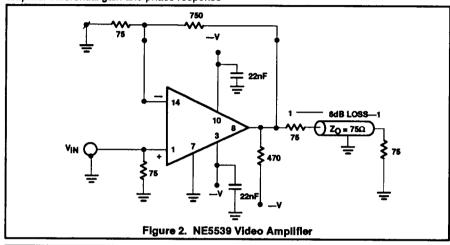
The NE5539 wideband operational amplifier is easily adapted for use as a color video amplifier. A typical circuit is shown in 2 along with vector-scope1 photographs showing the amplifier differential gain and phase response

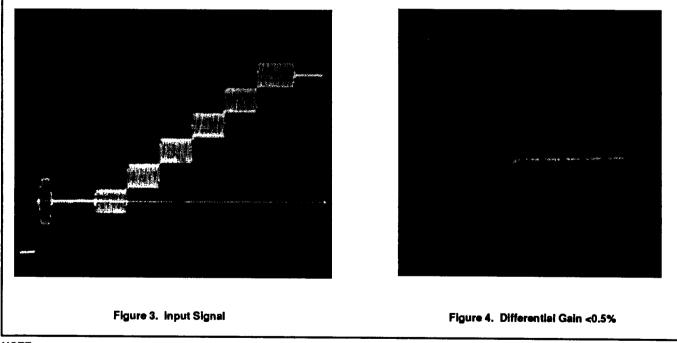
to a standard five-step modulated staircase linearity signal (Figures 3, 4 and 5). As can be seen in 4, the gain varies less than 0.5% from the bottom to the top of the staircase. The maximum differential phase shown in 5 is approximately +0.1°.

The amplifier circuit was optimized for a 75W input and output termionation impedance with a gain of approximately 10 (20dB).

#### NOTE:

 The input signal was 200mV and the output 2V. V<sub>CC</sub> was ±8V.



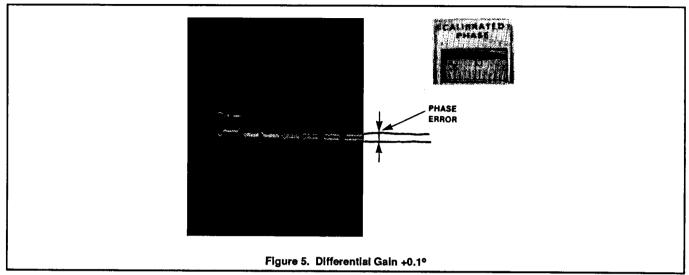


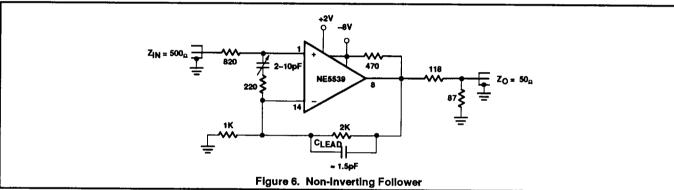
### NOTE:

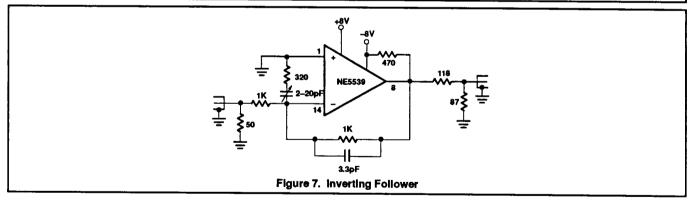
Instruments used for these measurements were Tektronix 146 NTSC test signal generator, 520A NTSC vectorscope, and 1480 waveform monitor.

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Signetics Military Products

# **Packaging Information**

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#### SIGNETICS STANDARD PACKAGE DESCRIPTIONS

All Military package case outlines and physical dimensions conform with the current revision MIL-M-38510, Appendix C, except for package types which are not included in that specification.

The physical dimensions for standard package types which are not included in Appendix C are included herein in Appendix C format. Case outline letters are assigned to these packages according to JEDEC Publication 101 as follows:

- Leadless chip carriers Dual-in-line packages
- Flat packages
- All other configurations

A case outline suffix number is assigned herein for identification purposes only, and is not marked on the product.

Signetics Military products are offered in a wide range of package configurations to optimally fit our customer needs.

- Dual-in-line Packages; Frit glass sealed CERDIP (F package family) with 8-40 leads, and side-brazed ceramic (I package family) with 48-64 leads.
- · Flat Packages; Frit glass sealed alumina CERPAC (W package family) with 14-28 leads, and brazed leaded ceramic (Q package family) with 52 leads.
- · Ceramic Chip Carriers; triple laminated, metal-lidded LCC (G package family) with 20-68 terminals.
- Pin Grid Array; metal-lidded ceramic pin grid (P package family) with 68-100 leads.
- Shown in Table 1 are the case outline letters assigned according to Appendix C of MIL-M-38510 and JEDEC publication 101. Unless otherwise noted, all package types are Configuration 1 and all lead finishes are hot solder dip Finish "A".

Table 1

Package Description	Type Designation	Case Outline	Theta-JC °C/Watt4
8DIP3	D-4	Р	28 28
14DIP3	D-1	С	28
16DIP3	D-2	Ė	28
18DIP3	D-6	v	28
20DIP3	D-8	Ř	28
22DIP4	D-7	Ŵ	28
24DIP3	D-9	Ë	28
24DIP4	D-11	X²	28
24DIP6	D-3	Ĵ	28
28DIP6	D-10		28
40DIP6	D-5	â	28
48DIP6	D-141	$\overline{X^2}$	28
50DIP9	D-12 <sup>1</sup>	Xs	28
64DIP9	D-13 <sup>1</sup>	X2 X3 X5 X5 X5	28
14FLAT	F-2	D F Y2 S K Y2	22
16FLAT	F-5	F	22
18FLAT	F-10	λ <sub>5</sub>	22
20FLAT	F-9	S	22 22
24FLAT	F-6	K	22
28FLAT	F-11	Υ2	22
52FLAT	Y-1 <sup>1</sup>	γ2	22
18LLCC	C-9	U²	20
20LLCC	C-23	2	20
28LLCC	C-4 <sup>3</sup>	2 3 U <sup>2</sup> U <sup>2</sup>	20
32LLCC	C-12	U <sup>2</sup>	20
44LLCC	C-5	U <sup>2</sup>	20
68LLCC	C-7	U2	20
68PGA	P-AB	Z <sup>2</sup> Z <sup>2</sup>	20
84PGA	P-AB	Z <sup>2</sup>	20

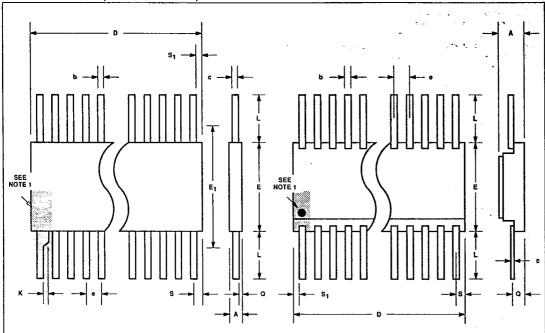
#### NOTES:

- Configuration 2.
  Per JEDEC publication 101.
  Dimension A (LLCC thickness) is 75mils maximum
- See RADC test report RADC-TR-86-97 for thermal resistance confidence and derating.

Packaging Information

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### **CASE OUTLINES Y (FLAT PACKAGES)**



Configuration 1

Configuration 2

### NOTES:

- 1. A lead tab (enlargement) or index dot is located within the shaded area shown at Pin 1. Other pin numbers proceed sequentially from Pin 1 counterclockwise (as viewed from the top of the device.

  2. This dimension allows for off-center lid, meniscus and glass overrun.
- The reference pin spacing is 0.050 between center-lines. Each pin centerline is located within ±0.005 of its logitudinal position relative to the first and last pin numbers.
- 4. This dimension is measured at the point of exit of the lead body.

  5. This dimension applied to all four corner pins.

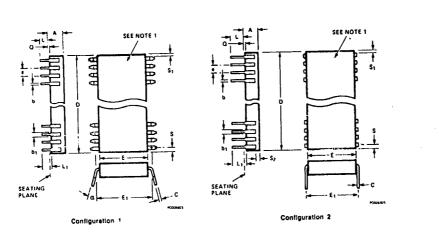
  6. Lead dimensions include 0.003 inch allowance for
- hot solder dip lead finish

OUTLINE	Y1		NOTES
CONFIGURATION	3	2	
NO. LEADS	5	2	
SIG. PKG.	a	P	ľ
SYMBOL	INC	HES	
	Min	Max	
Α	0.045	0.100	
ь	0.015	0.026	6
c	0.008	0.015	6
D	-	1.330	2
E	0.620	0.660	
e	0.050BSC		3
L	0.250	0.370	
Q	0.054	0.0666	4
S	-	0.045	5
S1	0.005	_	5

# Packaging Information

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### CASE OUTLINES X (DUAL IN-LINE PACKAGES)

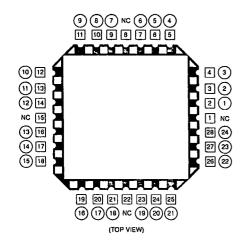


- 1. An index notch is located within the shaded area shown. Pin 1 is adjacent to the notch to the immediate left (as viewed from the top of the device) and other pin numbers proceed sequentially from Pin 1 counterclockwise.
- 2. The minimum limit for Dimension b1 is 0.023 inches for all four corner pins.
- 3. This dimension allows for off-center lid, meniscus, and glass overrun.
- 4. This dimension is measured at the centerline of the leads for Configuration 2.
- 5. The reference pin spacing is 0.100 between centerlines. Each pin centerline is located within ±0.010 of its longitudinal position relative to the first and last pin numbers.
- 6. This dimension is measured from the seating plane to the base plane.
- 7. This dimension applies to all four corner pins.
- 8. Lead dimensions include 0.003 inch allowance for hot solder dip lead finish.

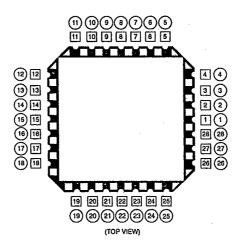
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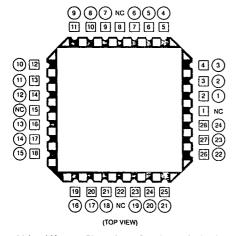
### **LEADLESS CHIP CARRIER (LLCC) PINOUTS**



24-Lead Logic Pinout for 28 Terminal Chip Carrier

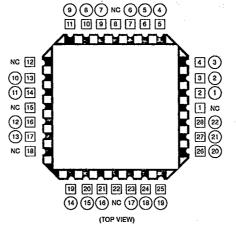


28-Lead Pinout for 28 Terminal Chip Carrier for all Device Types



24-Lead Memory Pinout for 28 Terminal Chip Carrier

- ☐ Chip Carrier Terminal Number
- O Dual In-Line Lead Numbe
- NC = No Connect



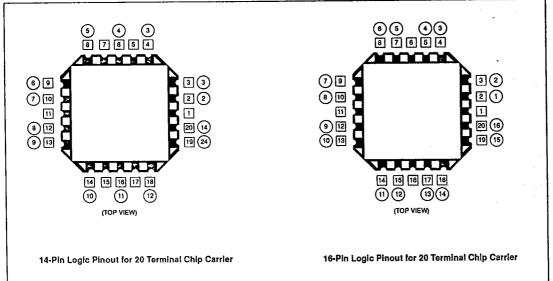
22-Lead Memory Pinout for 28 Terminal Chip Carrier

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### LEADLESS CHIP CARRIER (LLCC) PINOUTS



- ☐ Chip Carrier Terminal Number
- O Dual In-Line Lead Number