

# Tone decoder/phase-locked loop

567

## FEATURES

- Wide frequency range (0.01Hz to 500kHz)
- High stability of center frequency
- Independently controllable bandwidth (up to 14%)
- High out-band signal and noise rejection
- Logic-compatible output with 100mA current sinking capability
- Inherent immunity to false signals
- Frequency adjustment over a 20-to-1 range with an external resistor

## APPLICATIONS

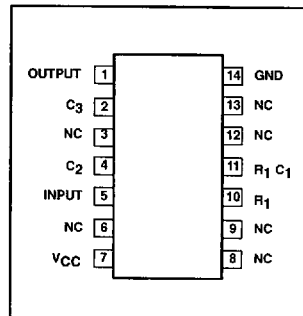
- Touch Tone® decoding
- Carrier-current remote controls
- Ultrasonic controls (remote TV, etc.)
- Communications paging
- Frequency monitoring and control
- Wireless intercom
- Precision oscillator

## DESCRIPTION

The 567 tone and frequency decoder is a highly stable phase-locked loop with synchronous AM lock detection and power output circuitry. Its primary function is to drive a load whenever a sustained frequency within its detection band is present at the

self-biased input. The bandwidth center frequency, and output delay are independently determined by means of four external components.

## PIN CONFIGURATION

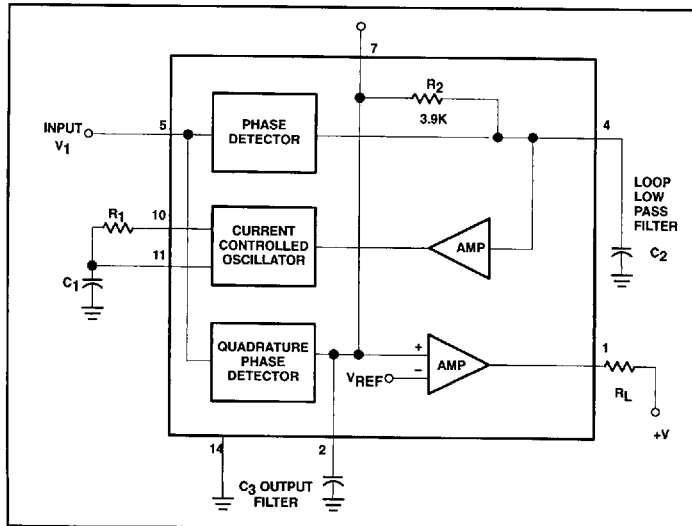


## ORDERING INFORMATION

DESCRIPTION	ORDER CODE	PACKAGE DESIGNATOR*
14-Pin Ceramic DIP	567/BCA	GDIP1-T14

\* MIL-STD 1835 or Appendix A of 1995 Military Data Handbook

## BLOCK DIAGRAM

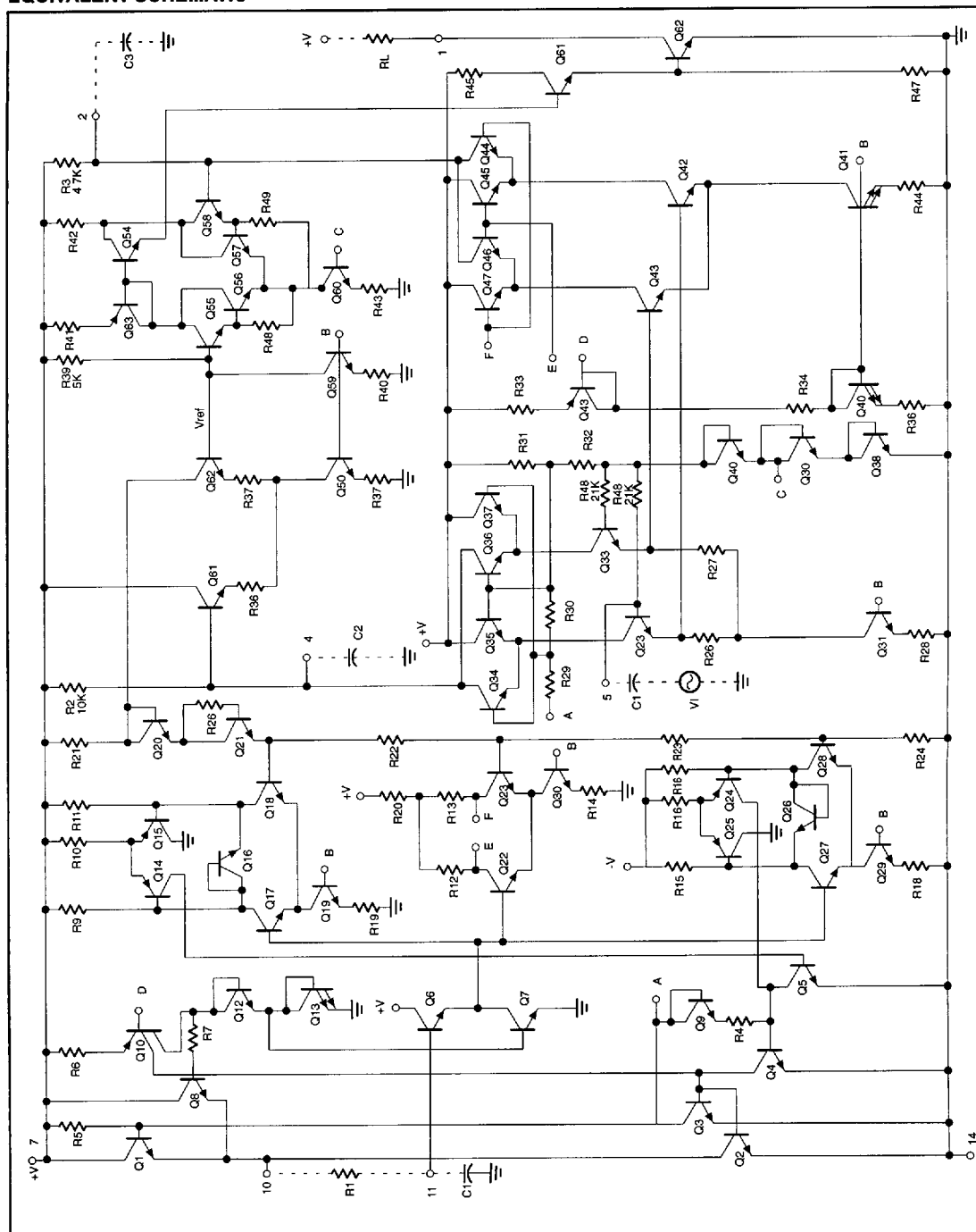


®Touch Tone is a registered trademark of AT & T.

## Tone decoder/phase-locked loop

567

## EQUIVALENT SCHEMATIC



## Tone decoder/phase-locked loop

567

## ABSOLUTE MAXIMUM RATINGS

SYMBOL	PARAMETER	RATING <sup>1</sup>	UNIT
V <sub>CC</sub>	Supply voltage	10	V
V <sub>I</sub>	Positive voltage at input	0.5 + V <sub>S</sub>	V
V <sub>I</sub>	Negative voltage at input	-10	V <sub>DC</sub>
V <sub>O</sub>	Output voltage (collector of output transistor)	15	V <sub>DC</sub>
T <sub>STG</sub>	Storage temperature range	-65 to +150	°C
P <sub>D</sub>	Power dissipation	300	mW

## DC ELECTRICAL CHARACTERISTICS

V<sub>CC</sub> = +5V, unless otherwise specified.

SYMBOL	PARAMETER	TEST CONDITIONS	T <sub>amb</sub> = +25°C			T <sub>amb</sub> = -55°C, +125°C			UNIT
			MIN	TYP	MAX	MIN	TYP	MAX	
Center Frequency <sup>2</sup>									
f <sub>o</sub>	Highest center frequency			500					kHz
Δf <sub>o</sub> /ΔT	Center frequency stability with temperature <sup>3</sup>						35 ±140		ppm/°C
Δf <sub>o</sub>	Center frequency distribution	f <sub>o</sub> = 100kHz ± 1.1/R <sub>1</sub> C <sub>1</sub>	-10	0	+10	-10		+10	%
Δf <sub>o</sub> /ΔV <sub>S</sub>	Center frequency shift with supply voltage	f <sub>o</sub> = 100kHz ± 1.1/R <sub>1</sub> C <sub>1</sub>		0.5	1				%/V
Detection Bandwidth									
DBW	Largest detection bandwidth	f <sub>o</sub> = 100kHz ± 1.1/R <sub>1</sub> C <sub>1</sub>	12	14	16	7		19	% of f <sub>o</sub>
ΔDBW	Largest detection bandwidth skew			2	4			4	% of f <sub>o</sub>
ΔDBW/ΔT	Largest detection bandwidth-variation with temperature	V <sub>I</sub> = 300mV <sub>RMS</sub>					±0.1		%/°C
ΔDBW/ΔV <sub>CC</sub>	Largest detection bandwidth-variation with supply voltage	V <sub>I</sub> = 300mV <sub>RMS</sub>		±2					%/V
Input									
R <sub>IN</sub>	Input resistance <sup>5</sup>		15	20	25				kΩ
V <sub>IN</sub>	Smallest detectable input voltage	I <sub>L</sub> = 100mA, f <sub>i</sub> = f <sub>o</sub>		20	25			50	mV <sub>RMS</sub>
V <sub>IN</sub>	Largest no-output input voltage	I <sub>L</sub> = 100mA, f <sub>i</sub> = f <sub>o</sub>	7	15		5			mV <sub>RMS</sub>
V <sub>OB</sub> /V <sub>IB</sub>	Greatest simultaneous outband signal-to-inband signal ratio			+6					dB
V <sub>1MIN</sub> /EN	Minimum input signal to wideband noise ratio	B <sub>n</sub> = 140kHz		-6					dB
Output									
I <sub>OH</sub>	Fastest on-off cycling rate			f <sub>o</sub> /20					μA
V <sub>OL</sub>	*1" output leakage current	V <sub>B</sub> = 15V		0.01	25			50	μA
	*0" output voltage <sup>6</sup>	I <sub>L</sub> = 30mA		0.2	0.4			0.4	V
		I <sub>L</sub> = 100mA		0.6	1.0			1.2	V
t <sub>f</sub>	Output fall time <sup>4</sup>	R <sub>L</sub> = 50Ω		30					ns
t <sub>r</sub>	Output rise time <sup>4</sup>	R <sub>L</sub> = 50Ω		150					ns
Power Supply									
V <sub>CC</sub>	Operating voltage range		4.75		9.0	4.75		9.0	V
I <sub>CC</sub>	Supply current quiescent			6	8			9.8	mA
	Supply current - activated	R <sub>L</sub> = 20kΩ		11	13			14.5	mA
P <sub>D</sub>	Quiescent power dissipation			30					mW

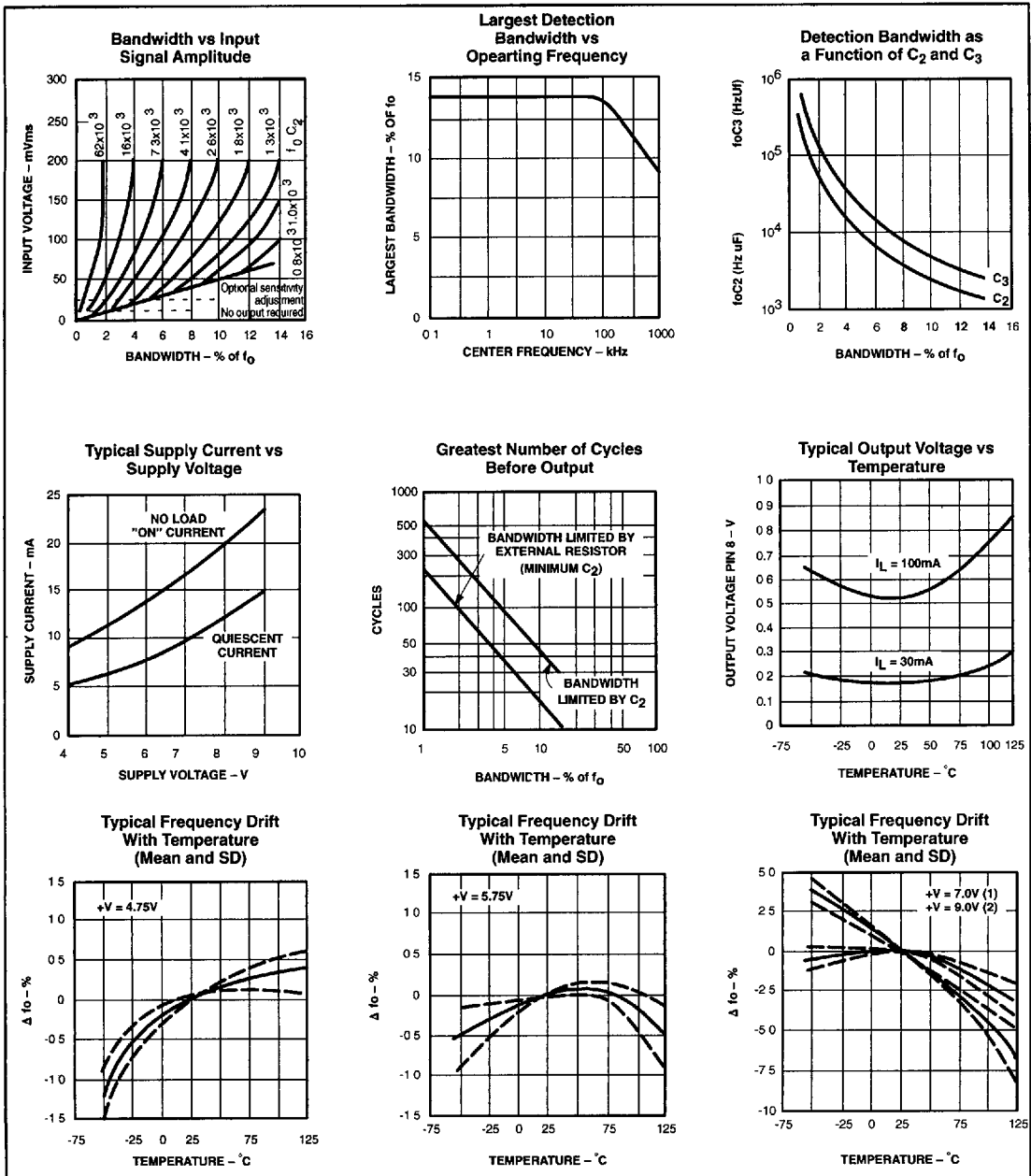
## NOTES:

- Operation beyond limits in this table may impair the useful life of the device.
- Frequency determining resistor R<sub>1</sub> should be between 2 and 20kΩ.
- Applicable over 4.75V to 5.75V. See graphs for more detailed information.
- Pin 8 to Pin 1 feedback R<sub>L</sub> network selected to eliminate pulsing during turn-on and turn-off.
- Guaranteed, but not tested.
- For long term static operation, derate the sink current to 85mA maximum.

## Tone decoder/phase-locked loop

567

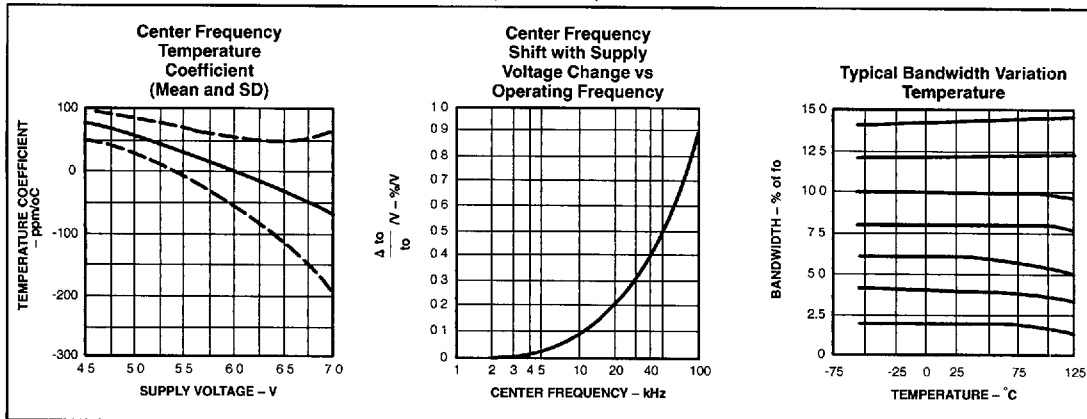
## TYPICAL PERFORMANCE CHARACTERISTICS



## Tone decoder/phase-locked loop

567

## TYPICAL PERFORMANCE CHARACTERISTICS (Continued)



## DESIGN FORMULAS

$$f_0 \approx \frac{1.1}{R_1 C_1}$$

$$BW \approx 1070 \sqrt{\frac{V_1}{f_0 C_2}} \text{ in \% of } f_0$$

Where

 $V_1$  = Input Voltage ( $V_{RMS}$ ) $C_2$  = Low-Pass Filter Capacitor ( $\mu F$ )PHASE-LOCKED LOOP  
TERMINOLOGY CENTER  
FREQUENCY ( $f_0$ )

The free-running frequency of the current-controlled oscillator (CCO) in the absence of an input signal.

## Detection Bandwidth (BW)

The frequency range, centered about  $f_0$ , within which an input signal above the threshold voltage (typically  $20mV_{RMS}$ ) will cause a logical zero state on the output. The detection bandwidth corresponds to the loop capture range.

## Lock Range

The largest frequency range within which an input signal above the threshold voltage will hold a logical zero state on the output.

## Detection Band Skew

A measure of how well the detection band is centered about the frequency,  $f_0$ . The skew is defined as  $(f_{MAX} + f_{MIN} - 2f_0)/2f_0$  where  $f_{MAX}$  and  $f_{MIN}$  are the frequencies corresponding

to the edges of the detection band. The skew can be reduced to zero if necessary by means of an optional centering adjustment.

## OPERATING INSTRUCTIONS

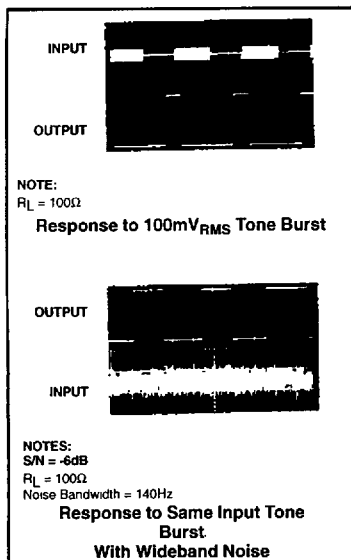
Figure 18 shows a typical connection diagram for the 567. For most applications, the following three-step procedure will be sufficient for choosing the external components  $R_1$ ,  $C_1$ ,  $C_2$  and  $C_3$ .

5. Select  $R_1$  and  $C_1$  for the desired center frequency. for best temperature stability,  $R_1$  should be between  $2k\Omega$  and  $20k\Omega$ , and the combined temperature coefficient of the  $R_1 C_1$  product should have sufficient stability over the projected temperature range to meet the necessary requirements.
6. Select the low pass capacitor,  $C_2$ , by referring to the Bandwidth versus Input Signal Amplitude graph. If the input amplitude variation is known, the appropriate value of  $f_0 C_2$  necessary to give the desired
7. The value of  $C_3$  is generally non-critical.  $C_3$  sets the band edge of a low pass filter which attenuates frequencies outside the detection band to eliminate spurious outputs. If  $C_3$  is too small, frequencies just outside the detection band will switch the output stage on and off at the beat frequency, or the output may pulse on and off during the turn-on transient. If  $C_3$  is too large, turn-on and turn-off of the output stage will be delayed until the voltage on  $C_3$  passes the threshold voltage. (Such delay may be desirable to avoid spurious outputs due to transient frequencies.) A typical min. value for  $C_3$  is  $2C_2$ .

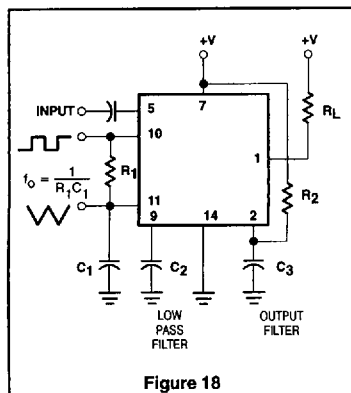
## Tone decoder/phase-locked loop

567

### TYPICAL RESPONSE



8. Optional resistor  $R_2$  sets the threshold for the largest "no output" input voltage. A value of  $130k\Omega$  is used to assure the tested limit of  $10mV_{RMS}$  min. This resistor can be referenced to ground for increased sensitivity. The explanation can be found in the "optional controls" section which follows.



**Figure 18**

### AVAILABLE OUTPUTS (Figure 19)

The primary output is the uncommitted output transistor collector, Pin 1. When an in-band input signal is present, this transistor saturates; its collector voltage being less than 1.0V (typically 0.6V) at full output current (100mA). The voltage at Pin 4 is the phase detector output which is a linear function of frequency over the range of 0.95 to 1.05  $f_0$ .

with a slope of about 20mV per percent of frequency deviation. The average voltage at Pin 2 is, during lock, a function of the inband input amplitude in accordance with the transfer characteristic given. Pin 10 is the controlled oscillator square wave output of magnitude  $(+V - 2V_{BE}) = (+V - 1.4V)$  having a DC average of  $+V/2$ . A 1k $\Omega$  load may be driven from Pin 10. Pin 11 is an exponential

triangle of  $1V_{P-P}$  with an average DC level of  $+V/2$ . Only high impedance loads may be connected to Pin 11 without affecting the CCO duty cycle or temperature stability.

## Tone decoder/phase-locked loop

567

## OPERATING PRECAUTIONS

A brief review of the following precautions will help the user achieve the high level of performance of which the 567 is capable.

1. Operation in the high input level mode (above 200mV) will free the user from bandwidth variations due to changes in the in-band signal amplitude. The input stage is now limiting, however, so that out-band signals or high noise levels can cause an apparent bandwidth reduction as the in-band signal is suppressed. Also, the limiting action will create in-band components from sub-harmonic signals, so the 567 becomes sensitive to signals at  $f_0/3$ ,  $f_0/5$ , etc.
2. The 567 will lock onto signals near  $(2n + 1)f_0$ , and will give an output for signals near  $(4n + 1)f_0$  where  $n = 0, 1, 2$ , etc. Thus, signals at  $5f_0$  and  $9f_0$  can cause an unwanted output. If such signals are anticipated, they should be attenuated before reaching the 567 input.
3. Maximum immunity from noise and output band signals is afforded in the low input level (below 200mV<sub>RMS</sub>) and reduced

$$C_2 = \frac{130}{f} \mu\text{F}$$

$$C_3 = \frac{260}{f} \mu\text{F}$$

In cases where turn-off time can be sacrificed to achieve fast turn-on, the optional sensitivity adjustment circuit can be used to move the quiescent  $C_3$  voltage lower (closer to the threshold voltage). However, sensitivity to beat frequencies, noise and extraneous signals will be increased.

## OPTIONAL CONTROLS (Figure 20)

The 567 has been designed so that, for most applications, no external adjustments are required. Certain applications, however, will

bandwidth operating mode. However, decreased loop damping causes the worst-case lockup time to increase, as shown by the Greatest Number of Cycles Before Output vs Bandwidth graph.

4. Due to the high switching speeds (20ns) associated with 567 operation, care should be taken in lead routing. Lead lengths should be kept to a min. The power supply should be adequately bypassed close to the 567 with a 0.01 $\mu\text{F}$  or greater capacitor; grounding paths should be carefully chosen to avoid ground loops and unwanted voltage variations. Another factor which must be considered is the effect of load energization on the power supply. For example, an incandescent lamp typically draws 10 times rated current at turn-on. This can cause supply voltage fluctuations which could, for example, shift the detection band of narrow-band systems sufficiently to cause momentary loss of lock. The result is a low-frequency oscillation into and out of lock. Such effects can be prevented by supplying heavy load currents from a sep-

arate supply or increasing the supply filter capacitor

## SPEED OF OPERATION

Min. lock-up time is related to the natural frequency of the loop. The lower it is, the longer becomes the turn-on transient. Thus, max. operating speed is obtained when  $C_2$  is at a minimum. When the signal is first applied, the phase may be such as to initially drive the controlled oscillator away from the incoming frequency rather than toward it. Under this condition, which is of course unpredictable, the lock-up transient is at its worst and the theoretical minimum lock-up time is not achievable. We must simply wait for the transient to die out.

The following expressions give the values of  $C_2$  and  $C_3$  which allow highest operating speeds for various band center frequencies. The minimum rate at which digital information may be detected without information loss due to the turn-on transient or output chatter is about 10 cycles per bit, corresponding to an information transfer rate of  $f_0/10$  baud.

## SENSITIVITY ADJUSTMENT

(Figure 20)

When operated as a very narrow band detector (less than 8%), both  $C_2$  and  $C_3$  are made quite large in order to improve noise and outband signal rejection. This will inevitably slow the response time. If, however, the output stage is biased closer to the threshold level, the turn-on time can be improved. This is accomplished by drawing additional current to Terminal 2. Under this condition, the 567 will also give an output for lower-level signals (10mV or lower).

## Tone decoder/phase-locked loop

567

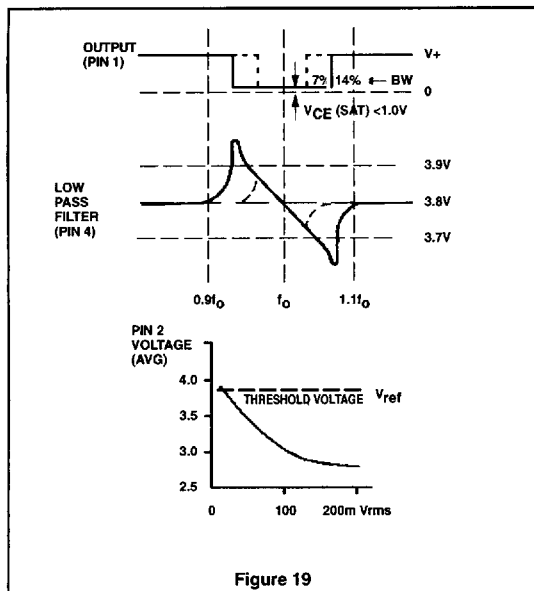


Figure 19

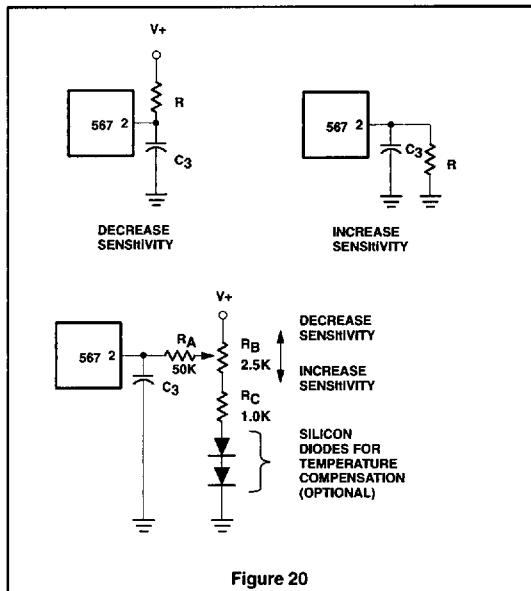


Figure 20

By adding current to Terminal 2, the output stage is biased further away from the threshold voltage. This is most useful when, to obtain maximum operating speed,  $C_2$  and  $C_3$  are made very small. Normally, frequencies just outside the detection band could cause false outputs under this condition. By desensitizing the output stage, the outband beat notes do not feed through to the output stage. Since the input level must be somewhat greater when the output stage is made less sensitive, rejection of third harmonics or in-band harmonics (of lower-frequency signals) is also improved.

**CHATTER PREVENTION (Figure 21)**

Chatter occurs in the output stage when  $C_3$  is relatively small, so that the lock transient and the AC components at the quadrature phase detector (lock detector) output cause the output stage to move through its threshold more than once. Many loads, for example lamps and relays, will not respond to the chatter. However, logic may recognize the chatter as a series of outputs. By feeding the output stage output back to its input (PIN 2) the chatter can be eliminated. Three schemes for doing this are given in Figure 21. All operate by feeding the first output step (either on or off) back to the input, pushing

the input past the threshold until the transient conditions are over. It is only necessary to assure that the feedback time constant is not so large as to prevent operation at the highest anticipated speed. Although chatter can always be eliminated by making  $C_3$  large, the feedback circuit will enable faster operation of the 567 by allowing  $C_3$  to be kept small. Note that if the feedback time constant is made quite large, a short burst at the input frequency can be stretched into a long output pulse. This may be useful to drive, for example, stepping relays.

**DETECTION BAND CENTERING (OR SKEW) ADJUSTMENT**

(Figure 22)

When it is desired to alter the location of the detection band (corresponding to the loop capture range) within the lock range, the circuits shown in Figure 22 can be used. By moving the detection band to one edge of the range, for example, input signal variations will expand the detection band in only one direction. This may prove useful when a strong but undesirable signal is expected on one side or the other of the center frequency. Since  $R_B$  also alters the duty cycle slightly, this method may be used to obtain a precise

duty cycle when the 567 is used as an oscillator.

**ALTERNATE METHOD OF BANDWIDTH REDUCTION**

(Figure 23)

Although a large value of  $C_2$  will reduce the bandwidth, it also reduces the loop damping so as to slow the circuit response time. This may be undesirable. Bandwidth can be reduced by reducing the loop gain. This scheme will improve damping and permit faster operation under narrow-band conditions. Note that the reduced impedance level at Terminal 4 will require that a larger value of  $C_2$  be used for a given filter cutoff frequency. If more than three 567s are to be used, the network of  $R_B$  and  $R_C$  can be eliminated and the  $R_A$  resistors connected together. A capacitor between this junction and ground may be required to shunt high-frequency components.

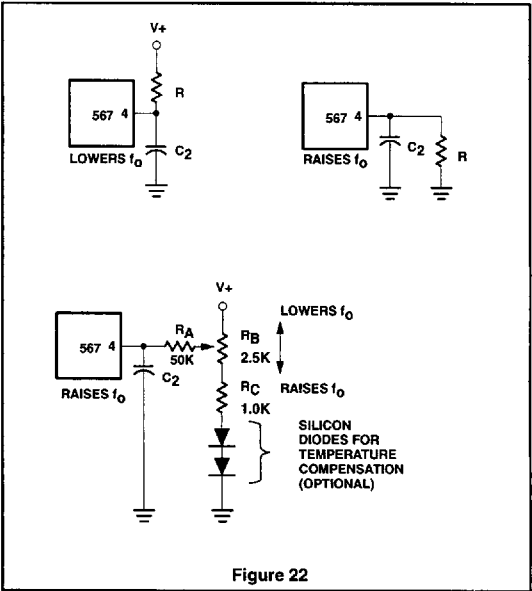
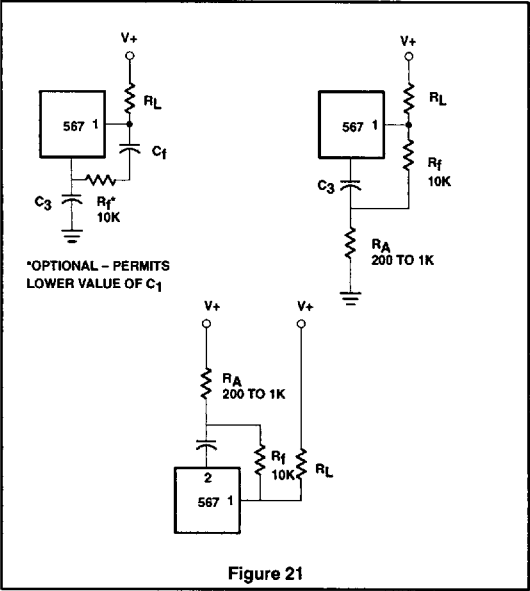
**OUTPUT LATCHING (Figure 24)**

To latch the output on after a signal is received, it is necessary to provide a feedback resistor around the output stage (between Pins 1 and 2). Pin 2 is pulled up to unlatch the output stage.



Tone decoder/phase-locked loop

567



## Tone decoder/phase-locked loop

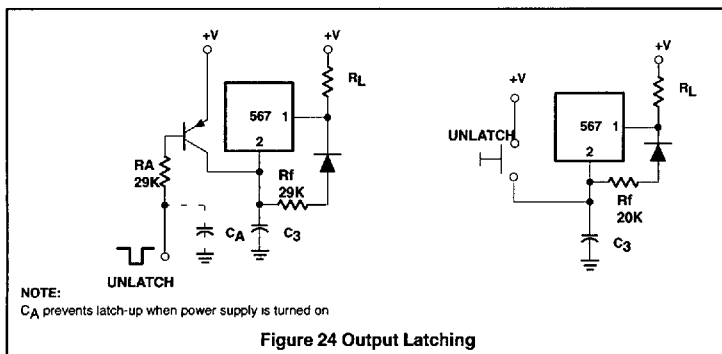
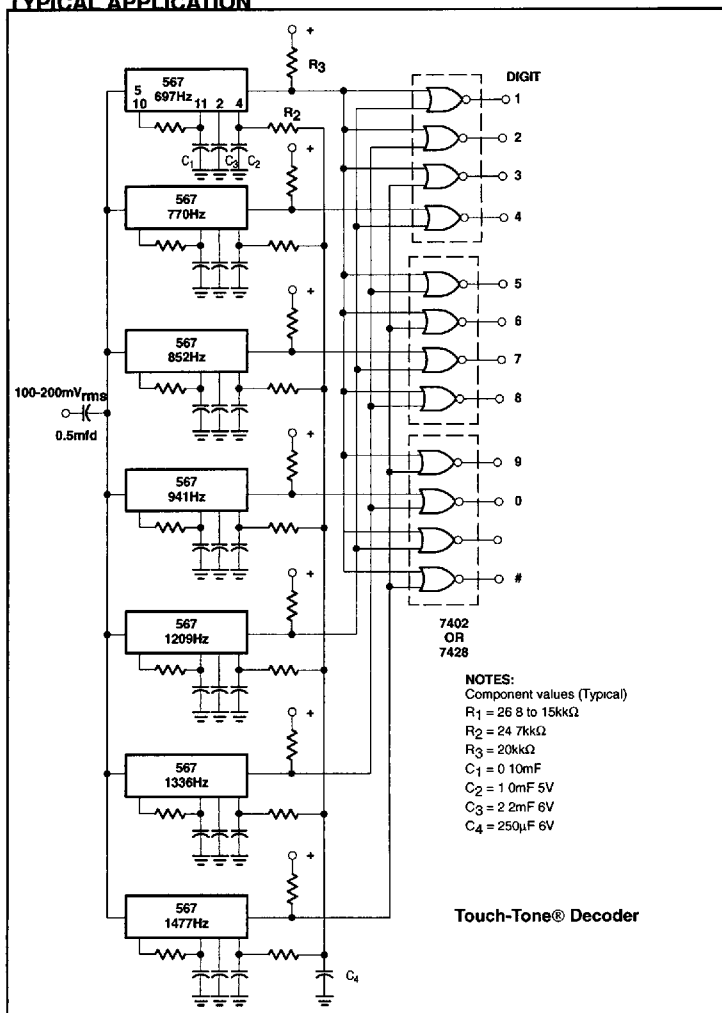
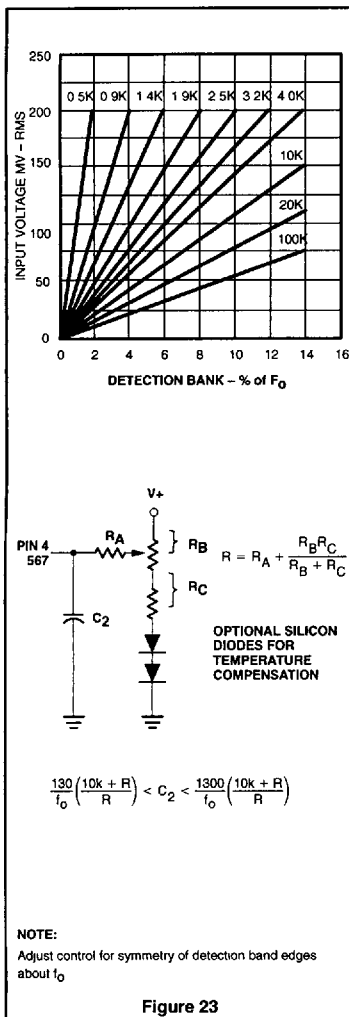
567

**REDUCTION OF C<sub>1</sub> VALUE (Figure 8)** **TYPICAL APPLICATION**

For precision very low-frequency applications, where the value of C<sub>1</sub> becomes large, an overall cost savings may be achieved by inserting a voltage follower between the R<sub>1</sub> C<sub>1</sub> junction and Pin 11, so as to allow a higher value of R<sub>1</sub> and a lower value of C<sub>1</sub> for a given frequency.

**PROGRAMMING**

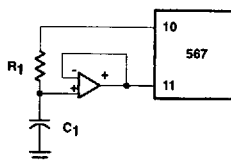
To change the center frequency, the value of R<sub>1</sub> can be changed with a mechanical or solid-state switch, or additional C<sub>1</sub> capacitors may be added by grounding them through saturating npn transistors.



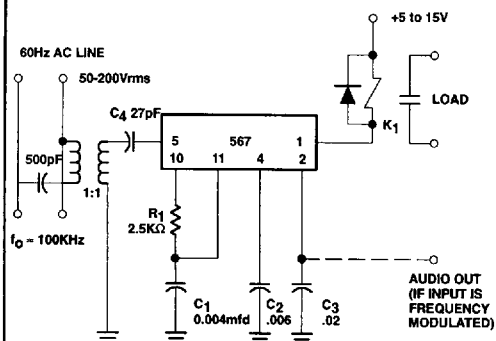
## Tone decoder/phase-locked loop

567

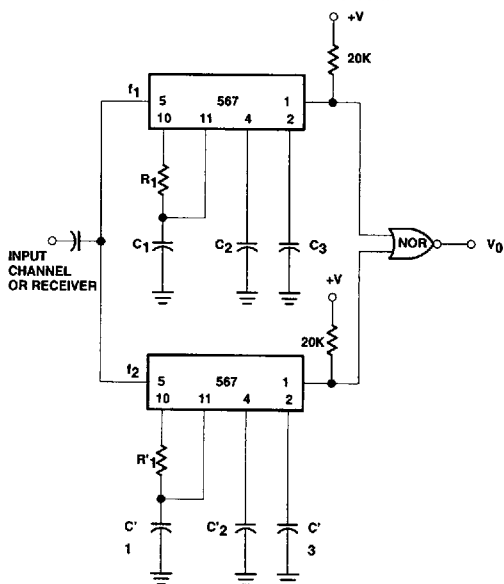
## TYPICAL APPLICATIONS (Continued)



Precision VLF

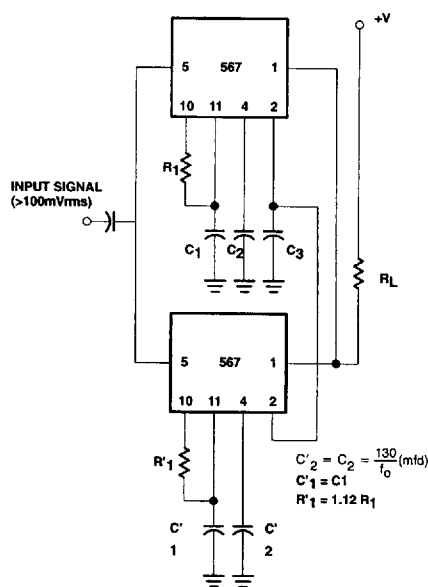


Carrier-Current Remote Control or Intercom

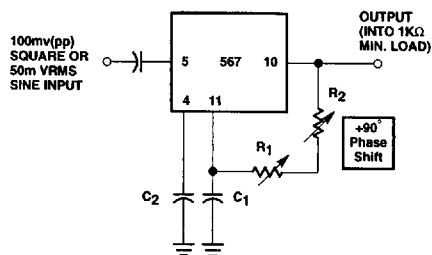


Dual-Tone Decoder

- NOTES:
- 1 Resistor and capacitor values chosen for desired frequencies and bandwidth
  - 2 If  $C_3$  is made large so as to delay turn-on of the top 567, decoding of sequential ( $f_1$   $f_2$ ) tones is possible



24% Bandwidth Tone Decoder



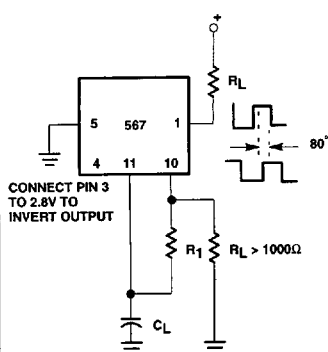
0° to 180° Phase Shifter

- NOTES:
- 1 Resistor and capacitor values chosen for desired frequencies and bandwidth
  - 2 If  $C_3$  is made large so as to delay turn-on of the top 567, decoding of sequential ( $f_1$   $f_2$ ) tones is possible

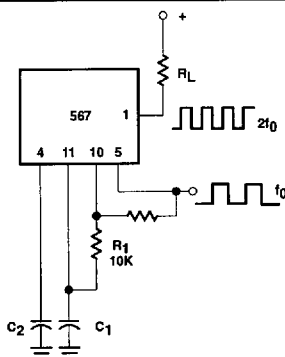
## Tone decoder/phase-locked loop

567

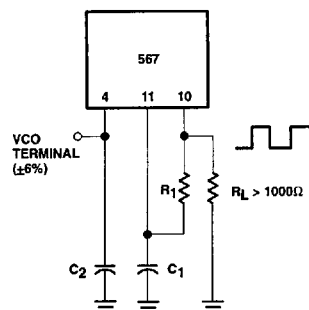
## TYPICAL APPLICATIONS (Continued)



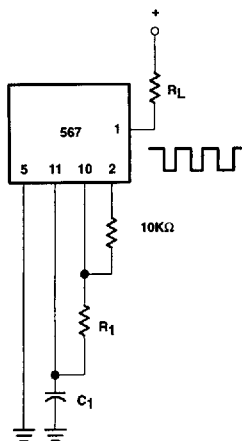
Oscillator with Quadrature Output



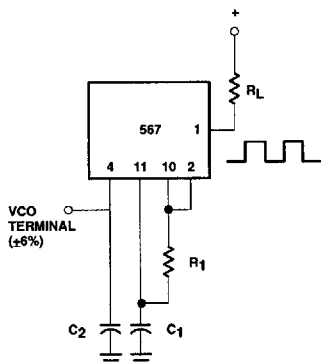
Oscillator with Double Frequency Output



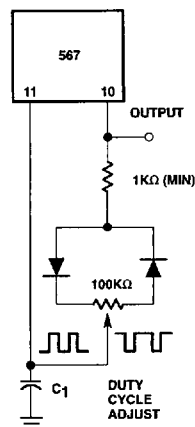
Precision Oscillator with 20ns Switching



Pulse Generator with 25% Duty Cycle



Precision Oscillator to Switch 100mA Loads



Pulse Generator