

57C4500-40/50/65/80

High Density First-in First-out (FIFO)
256x9 CMOS Memory



57C4500-40/50/65/80

Advanced Micro Devices

Advance Information

DISTINCTIVE CHARACTERISTICS

- RAM based FIFO
- 256x9 organization
- Cycle times of 50/65/80/100 nanoseconds
- Asynchronous and simultaneous writes and reads
- Low power consumption – 80 mA maximum
- Status flags – full, half-full, empty
- Retransmit capability
- Expandable in both width and depth
- Increased noise immunity for $\overline{X1}$ - CMOS threshold
- Functional and pin compatible with industry standard devices

GENERAL DESCRIPTION

The 57C4500 is a RAM-based CMOS FIFO that is 256 words deep with 9-bit wide words. It is expandable to any width and/or depth to create much larger FIFOs.

This FIFO can accept data and output data asynchronously and simultaneously at data rates from 0 to 20 MHz. Status flags are provided to signify empty, full, and half-full conditions. The capability also exists to retransmit data from the FIFO.

High Density FIFOs such as the 57C4500 are useful in a wide range of applications. The ability to buffer large transfers of data and the rate adaption capabilities make the 57C4500 useful in communication, image processing, mass storage, DSP, and printing systems.

BLOCK DIAGRAM

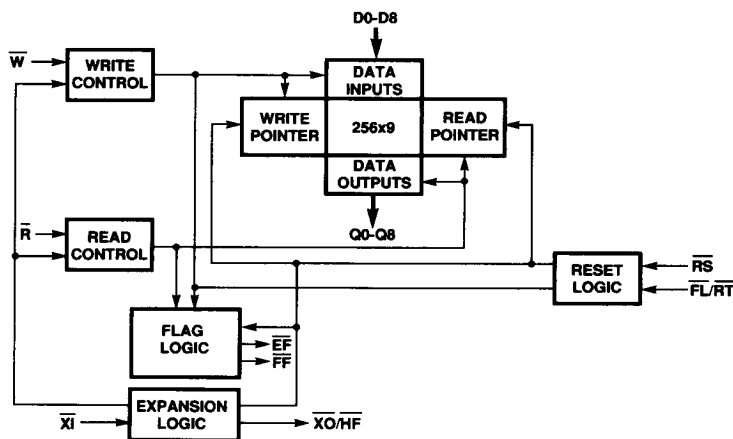


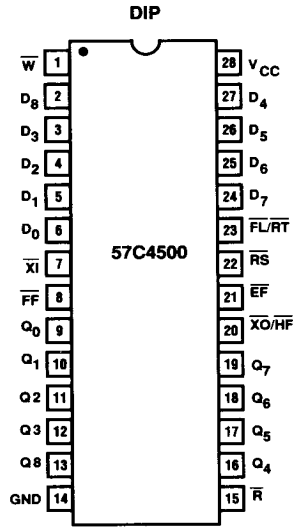
Figure 1.

Publication #	Rev.	Amendment
10907	A	/0
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Advance Information

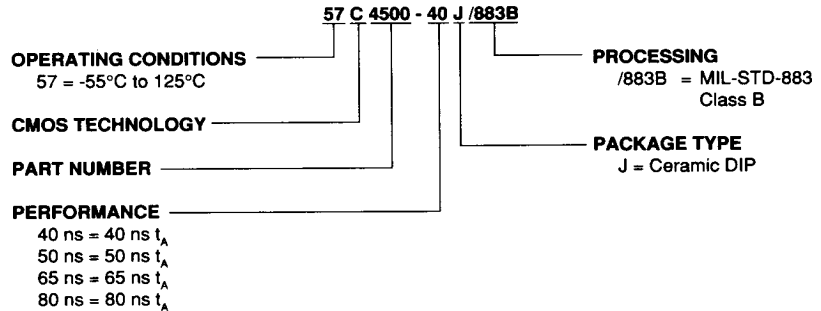
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CONNECTION DIAGRAMS



Pin Designations: $\bar{W}$ = Write
 $\bar{R}$ = Read
 $\bar{RS}$ = Reset
 $\bar{FL}/\bar{RT}$ = First Load/Retransmit
 D_x = Data In
 Q_x = Data Out
 $X1$ = Expansion In
 $X0/HF$ = Expansion Out/Half-Full Flag
 FF = Full Flag
 EF = Empty Flag
 V_{CC} = Supply Voltage
 GND = Ground

ORDERING INFORMATION



ORDERING INFORMATION

Part Number	Description	Package	Temp
57C4500-40	256-word by 9-bit FIFO	J	Mil
57C4500-50			
57C4500-65			
57C4500-80			

Advance Information

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ABSOLUTE MAXIMUM RATINGS

Supply voltage, V_{CC} -0.5 V to +7.0 V
 Input voltage -0.5 V to $V_{CC} + 0.5$ V
 Operating temperature -55°C to +125°C
 Storage temperature -65°C to +150°C
 Power dissipation 2.0 W
 DC output current 50 mA

Stresses above those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent device failure. Functionality at or above these limits is not implied. Exposure to absolute maximum ratings for extended periods may affect device reliability.

DC CHARACTERISTICS Military: $V_{CC} = 5 \text{ V} \pm 10\%$, $T_A = -55^\circ\text{C}$ to $+125^\circ\text{C}$

Parameter Symbol	Parameter Description	57C4500-40 $T_A = 40 \text{ ns}$		57C4500-50 $T_A = 50 \text{ ns}$		57C4500-65 $T_A = 65 \text{ ns}$		57C4500-80 $T_A = 80 \text{ ns}$		Unit
		Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
I_{IL}	Input Leakage Current (any input) (Note 1)	-1	1	-1	1	-1	1	-1	1	μA
I_{IO}	Output Leakage Current (data outputs) (Note 2)	-10	10	-10	10	-10	10	-10	10	μA
V_{IH}	Input High Voltage (all inputs except $\overline{XI}$) (Note 3)	2.0	—	2.0	—	2.0	—	2.0	—	V
V_{IL}	Input Low Voltage (all inputs except $\overline{XI}$) (Note 3)	—	0.8	—	0.8	—	0.8	—	0.8	V
$V_{IH(XI)}$	Input High Voltage, $\overline{XI}$ (Note 3)	3.5	—	3.5	—	3.5	—	3.5	—	V
$V_{IL(XI)}$	Input Low Voltage, $\overline{XI}$ (Note 3)	—	1.5	—	1.5	—	1.5	—	1.5	V
V_{OH}	Output Logic "1" Voltage $I_{OH} = -2 \text{ mA}$	2.4	—	2.4	—	2.4	—	2.4	—	V
V_{OL}	Output Logic "0" voltage $I_{OL} = 8 \text{ mA}$	—	0.4	—	0.4	—	0.4	—	0.4	V
I_{CC1}	Average V_{CC} Power Supply Current (Note 4)	—	80	—	80	—	80	—	80	mA
I_{CC2}	Average Standby Current ($R = \overline{W} = RS = FL/RT = V_{IH}$) (Note 4)	—	25	—	25	—	25	—	25	mA
I_{CC3}	Power Down Current (all inputs = $V_{CC} - 0.2 \text{ V}$) (Note 4)	—	10	—	10	—	10	—	10	mA

- Notes: 1. Measurements with $GND \leq V_{IN} \leq V_{CC}$.
 2. $R \geq V_{IH}$, $GND \leq V_{OUT} \leq V_{CC}$.
 3. These are absolute voltage levels with respect to the ground pins on the device and include all overshoots due to system or tester noise. Do not attempt to test these values without suitable equipment.
 4. I_{CC} measurements are made with outputs open.

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AC CHARACTERISTICS $V_{CC} = 5\text{ V} \pm 10\%$, $T_A = -55^\circ\text{C}$ to $+125^\circ\text{C}$

Parameter Symbol	Parameter Description	57C4500-40 Min. Max.	57C4500-50 Min. Max.	57C4500-65 Min. Max.	57C4500-80 Min. Max.	Unit
Write and Flag Timing						
t_{WC}	Write Cycle Time	50	65	80	100	ns
t_{WPW}	Write Pulse Width	40	50	65	80	ns
t_{WR}	Write Recovery Time	10	15	15	20	ns
t_{DS}	Data Setup Time	25	30	30	40	ns
t_{DH}	Data Hold Time	0	5	10	10	ns
t_{WFF}	Write LOW to Full Flag LOW	35	45	60	60	ns
t_{WHF}	Write LOW to Half-Full Flag LOW	50	65	80	100	ns
t_{WEF}	Write HIGH to Empty Flag HIGH	35	45	60	60	ns
t_{WLZ}	Write pulse HIGH to data bus at LOW Z (Note 1)	10	15	15	20	ns
Read and Flag Timing						
t_{RC}	Read Cycle Time	50	65	80	100	ns
t_A	Access Time	40	50	65	80	ns
t_{RR}	Read Recovery Time	10	15	15	20	ns
t_{RPW}	Read Pulse Width	40	50	65	80	ns
t_{RLZ}	Read pulse LOW to data bus at LOW Z (Note 1)	5	10	10	10	ns
t_{DV}	Data Valid from read pulse HIGH	5	5	5	5	ns
t_{RHZ}	Read pulse HIGH to data bus at HIGH Z (Note 1)	25	30	30	30	ns
t_{RFF}	Read HIGH to Full Flag HIGH	35	45	60	60	ns
t_{RHF}	Read HIGH to Half Full-Flag HIGH	50	65	80	100	ns
t_{REF}	Read LOW to Empty Flag LOW	35	45	60	60	ns
Reset Timing						
t_{RSC}	Reset Cycle Time	50	65	80	100	ns
t_{RS}	Reset Pulse Width	40	50	65	80	ns
t_{RSS}	Reset Setup Time	40	50	65	80	ns
t_{RSR}	Reset Recovery Time	10	15	15	20	ns
t_{EFL}	Reset to Empty Flag LOW	50	65	80	100	ns
t_{HFH}	Reset to Half-Full Flag High	50	65	80	100	ns
t_{FFH}	Reset to Full Flag HIGH	50	65	80	100	ns
Retransmit Timing						
t_{RTC}	Retransmit Cycle Time	50	65	80	100	ns
t_{RT}	Retransmit Pulse Width	40	50	65	80	ns
t_{RTR}	Retransmit Recovery Time	10	15	15	20	ns

Note: 1. Characterized parameters.