Military Low Power FIFOs
64x4 64x5 Memory
12 MHz (Standalone)
57L401D 57L402D 57L4013D

Conforms to Mil-Std-883, Class B

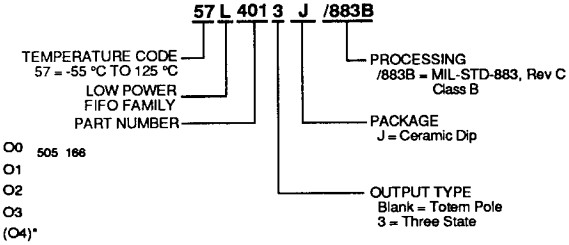
Features/Benefits

- **High-speed 12 MHz shift-in/shift-out data rates**
- **Low power consumption**
- **Choice of 4-bit or 5-bit data width**
- **TTL inputs and outputs**
- **Readily expandable in word width**
- **Structured pinouts. Outputs pins directly opposite corresponding input pins**
- **High-drive capability**
- **Asynchronous operation**
- **Dose rate (transient upset) junction-isolated bipolar process $2x10^{10}$ RADs (Si)/s recovery time of 50 to 70 µs from a 1 µs pulse**
- **Neutron fluence (permanent damage): $1x10^{13}$ N/cm²**

Description

The 57L401D/2D and 574013D are "fall-through" high-speed First-In First-Out (FIFO) memories organized 64 words by 4 bits and 64 words by 5 bits. These FIFOs are expandable in word width. The FIFOs are attractive for many applications such as disk controllers, communication buffers, rate buffers, etc. They feature high-drive (I_{OL} = 12 mA) outputs. The 57L4013D features three-state outputs.

Ordering Information



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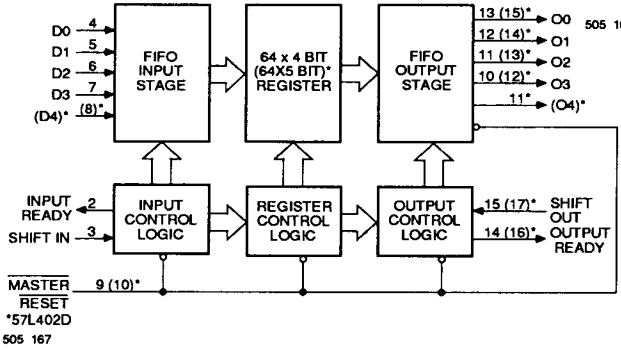
Block Diagram



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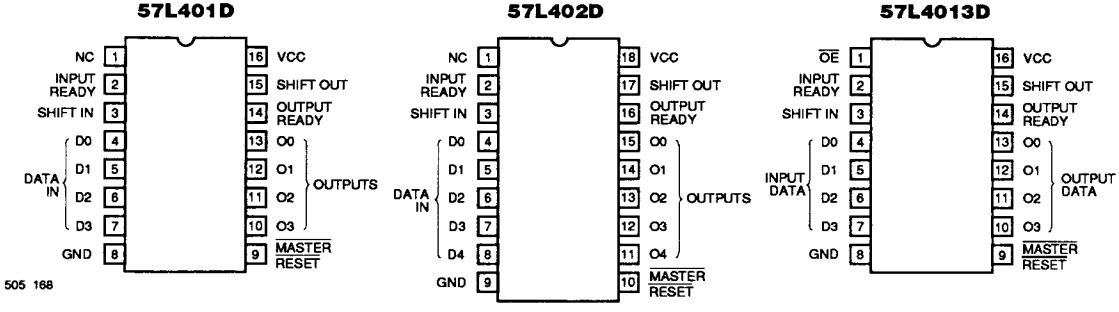
Device Pinouts



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Absolute Maximum Ratings*

Supply voltage, V_{CC} ..... –0.5 V to 7 V
Input voltage range ..... –1.5 V to 7 V
Off-state output voltage ..... –0.5 V to to 5.5 V
Storage temperature ..... –65°C to +150°C

*Note:
Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only, and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods of time may affect reliability.

Operating Conditions

SYMBOL	PARAMETER	FIGURE	MIN	MAX	UNIT
V_{CC}	Supply voltage		4.5	5.5	V
t_{SIH}†	Shift in HIGH time	1	30		ns
t_{SIL}†	Shift in LOW time	1	15		ns
t_{IDS}	Input data setup to SI (Shift In)	1	0		ns
t_{IDH}	Input data hold time to SI (Shift In)	1	35		ns
t_{RIDS}	Input data setup to IR (Input Ready)	3	0		ns
t_{RIDH}	Input data hold time to IR (Input Ready)	3	35		ns
f_{IN}	Shift in rate	1		12	MHz
f_{OUT}	Shift out rate	4		12	MHz
t_{SOH}†	Shift out HIGH time	4	28		ns
t_{SOL}†	Shift out LOW time	4	18		ns
t_{MRW}**	Master Reset pulse	8	40		ns
t_{MRS}***	Master Reset to SI	8	45		ns
V_{IL}*	Low level input voltage			0.8	V
V_{IH}*	High level input voltage		2.0		V
T_A	Operating free-air temperature		–55		°C
T_C	Operating instant-on case temperature			125	°C

* These are absolute voltages with respect to the ground pin on the device and include all overshoots due to system and/or tester noise. Do not attempt to test these values without suitable equipment.
** If the FIFO is not full (IR HIGH) $\overline{MR}$ LOW forces IR LOW, followed by IR returning high when $\overline{MR}$ goes high.
*** t_{MRS} is measured on initial characterization lots only and is not directly tested in production.
† See AC test and high-speed application note.

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Electrical Characteristics Over Operating Conditions

SYMBOL	PARAMETER		TEST CONDITIONS		MIN	MAX	UNIT
V_{IC}	Input clamp voltage		V_{CC} = MIN	I_I = –18 mA		–1.5	V
I_{IL}	Low-level input current		V_{CC} = MAX	V_I = 0.45 V		–250	µA
I_{IH}	High-level input current		V_{CC} = MAX	V_I = 2.4 V		50	µA
I_I	Maximum input current		V_{CC} = MAX	V_I = 5.5 V		1	mA
V_{OL}	Low-level output voltage	Ouput, O	V_{CC} = MIN	I_{OL} = 12 mA		0.5	V
		IR, OR		I_{OL} = 8 ma			
V_{OH}	High-level output voltage	Output, O	V_{CC} = MIN	I_{OH} = –3.0 mA	2.4		V
		IR, OR		I_{OH} = –0.9 mA			
I_{OS}†	Output short-circuit current		V_{CC} = MAX	V_O = 0 V	–20	–90	mA
I_{OZL}	Off-state output current (57L4013D only)		V_{CC} = MAX	V_O = 0.4 V		–50	µA
I_{OZH}				V_O = 2.4 V		+50	
I_{CC}	Supply current		V_{CC} = MAX All inputs low. All outputs open.			120	mA

† Not more than one output should be shorted at a time and duration of the short circuit should not exceed one second.

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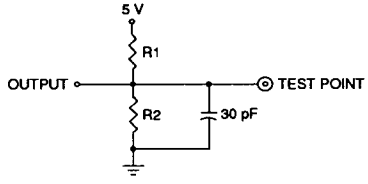
Standard Test Load*



Input Pulse Amplitude = 3 V
Input Rise and Fall Time (10% – 90%) = 2.5 ns
Measurements made at 1.5 V

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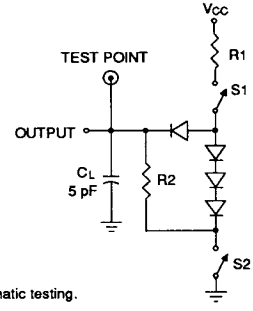
Three State Test Load*



*Equivalent test loads may be used for automatic testing.

I_{OL}	R1	R2
12 mA	390 Ω	760 Ω
8 mA	600 Ω	1200 Ω

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Switching Characteristics Over Operating Conditions

SYMBOL	PARAMETER	FIGURE	MIN	MAX	UNIT
t_{IRL}†	Shift In ↑ to Input Ready LOW	1		50	ns
t_{IRH}†	Shift In ↓ to Input Ready HIGH	1		30	ns
t_{ORL}†	Shift Out ↑ to Output Ready LOW	4		55	ns
t_{ORH}†	Shift Out ↓ Output Ready HIGH	4		55	ns
t_{ODH}†	Output Data Hold (previous word)	4	10		ns
t_{ODS}	Output Data Shift (next word)	4		50	ns
t_{PT}	Data throughput	3, 6		2.0	µs
t_{MRORL}	Master Reset ↓ to Output Ready LOW	8		65	ns
t_{MRIRH}*	Master Reset ↑ to Input Ready HIGH	8		35	ns
t_{MRIRL}*	Master Reset ↓ to Input Ready LOW	8		55	ns
t_{MRO}	Master Reset ↓ to Output LOW	8		75	ns
t_{IPH}	Input ready pulse HIGH	3	15		ns
t_{OPH}	Output ready pulse HIGH	6	20		ns
t_{ORD}	Output ready ↑ to Data Valid	4		0	ns
t_{PHZ}**	Output disable delay (57L4013D only)	A		35	ns
t_{PLZ}**				35	
t_{PZL}	Output Enable Delay (57L4013D only)	A		35	ns
t_{PZH}				45	

† See AC test and high-speed application note.
* If the FIFO is not full (IR HIGH), $\overline{MR}$ LOW forces IR LOW, followed by IR returning high when $\overline{MR}$ goes high.
** Actual test limits may be different to compensate for ATE.

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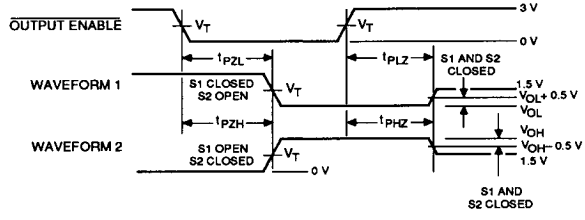

Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control.

Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.

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Figure A. Enable and Disable (57L4013D Only)

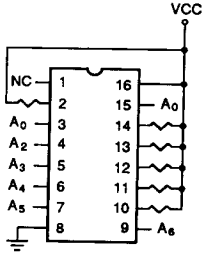
Military Case Outlines

PACKAGE OUTLINE LETTER	CONFORMS TO MIL-M-38510 APPENDIX C CASE
16J	D-2
18J	D-6

505029B

Burn-In Circuitry
Dynamic Burn-In

57L401D



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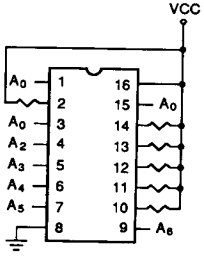
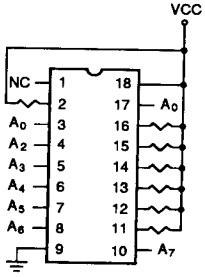
57L4013D



57L402D



$T_{ambient}$ = 125°C
V_{cc} = 5.25 ± 0.25 V
Square wave pulses on A0 to A8 are:
1. 50% ± 15% duty cycle
2. Logic "0" = –1 V to 0.7 V
3. Logic "1" = 2.4 V to V_{cc}
4. Frequency of each address is to be one-half of each preceding input, with A0 beginning at 100 kHZ.
   e.g. A0 = 100 kHz
   A1 = 50 kHz ± 10%
   A2 = 25 kHz ± 10%
   An = 1/2 An–1 ± 10%, etc.

Functional Description

Data Input

After power up the Master Reset is pulsed low (Figure 8) to prepare the FIFO to accept data in the first location. Master reset must be applied prior to use to ensure proper operation. When Input Ready (IR) is HIGH the first location is ready to accept data from the D_x inputs. Data then present at the data inputs is entered into the first location when the Shift-In (SI) is brought HIGH. An SI HIGH signal causes the IR to go LOW. Once data is entered into the first cell, the transfer of data from any full cell to the adjacent (downstream) empty cell is automatic, activated by an on-chip control. Thus data will stack up at the end of the device while empty locations will "bubble" to the front. t_{PT} defines the time required for the first data to travel from input to the output of a previously empty device. When SI is brought LOW and the FIFO is not full, IR will go HIGH, indicating more room is available. If the memory is full, IR will remain LOW. The FIFO should always be cleared by using master reset.

Data Output

Data is read from the Ox outputs. When data is shifted to the output stage, Output Ready (OR) goes HIGH, indicating the presence of valid data. When the OR is HIGH, data may be shifted out by bringing the Shift Out (SO) HIGH. A HIGH signal at SO causes the OR to go LOW. Valid data is maintained while the SO is HIGH. When SO is brought LOW the upstream data, provided the upstream stage has valid data, is shifted to the output stage, OR goes HIGH. If the FIFO is emptied, OR stays LOW and Data output will not be valid.

Input Ready and Output Ready may also be used as status signals indicating that the FIFO is completely full (Input Ready stays LOW for at least t_{PT}) or completely empty (Output Ready stays LOW for at least t_{PT}).

AC Test and High-Speed App. Notes

Since the FIFO is a very-high-speed device, care must be exercised in the design of the hardware and the timing utilized within the design. The internal shift rate of the FIFO typically exceeds 20 MHz operation. Device grounding and decoupling is crucial to correct operation as the FIFO will respond to very small glitches due to long reflective lines, high capacitances and/or poor supply decoupling and grounding. We recommend a monolithic ceramic capacitor 0.1 µF directly between V_{CC} and GND with very short lead length. In addition, care must be exercised in how the timing is set up and how the parameters are measured. For example, since an AND gate function is associated with both the Shift-In-Input-Ready combination, as well as the Shift-Out-Output-Ready combination, timing measurements may be misleading, i.e., rising edge of the Shift-In pulse is not recognized until Input Ready is HIGH. If Input Ready is not high due to (a) too high a frequency, or (b) FIFO being full or effected by Master Reset, the Shift-In activity will be ignored. This will affect the device from a functional standpoint, and will also cause the "effective" timing of Input Data Hold time (T_{IDH}) and the next activity of Input Ready (T_{IRL}) to be extended relative to Shift-In going HIGH. This same type of situation occurs with T_{ORL} and T_{ORH} as related to Shift-Out. For high-speed applications, proper grounding technique is essential.

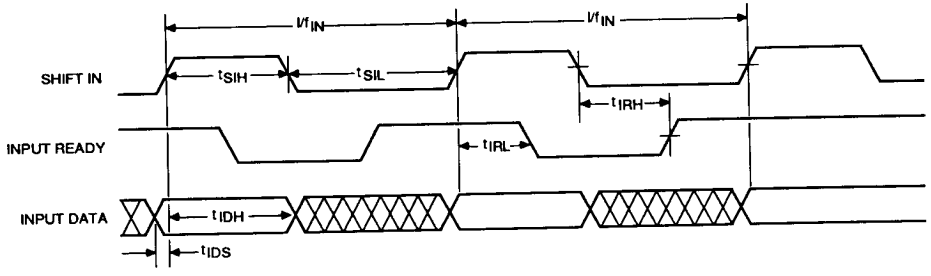
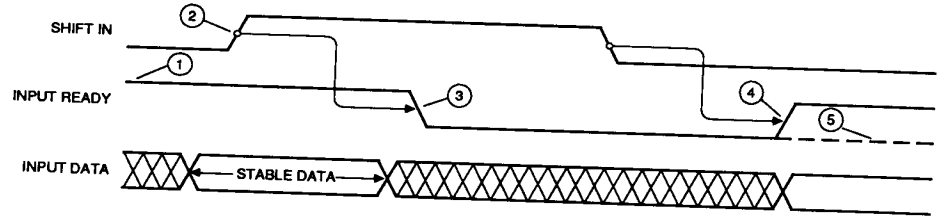


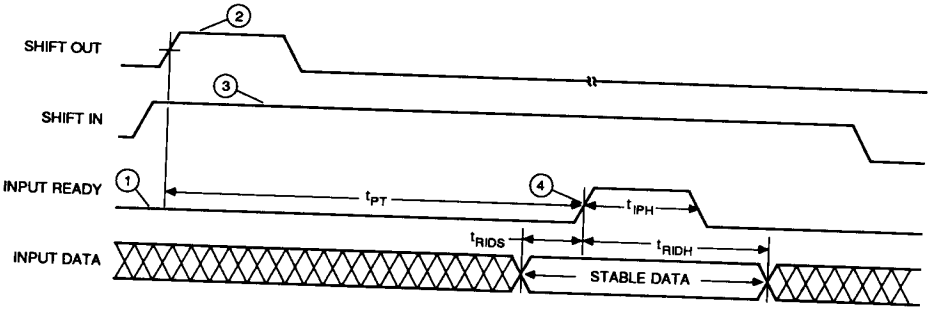
Figure 1. Input Timing



(1) Input Ready HIGH indicates space is available and a Shift-In pulse may be applied.
(2) Input Data is loaded into the first word. The Data from the first word is released for "fall through" to second word.
(3) Input Ready goes LOW indicating the first word is full.
(4) Shift-In going LOW allows Input Ready to sense the status of the first word. The first word is now empty as indicated by Input Ready HIGH.
(5) If the second word is already full then the data remains at the first word. Since the FIFO is now full Input Ready remains low.

505 154 Note: Shift-in pulses applied while Input Ready is LOW will be ignored (See Figure 3).

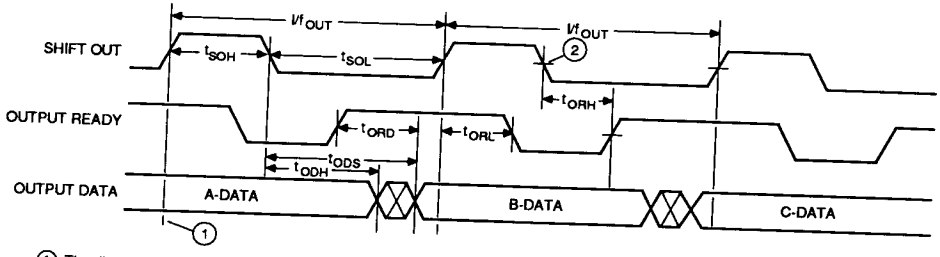
Figure 2. The Mechanism of Shifting Data Into the FIFO



(1) FIFO is initially full.
(2) Shift Out pulse is applied. An empty location starts "bubbling" to the front.
(3) Shift in is held HIGH.

505 175 (4) As soon as Input Ready becomes HIGH the Input Data is loaded into the first word.

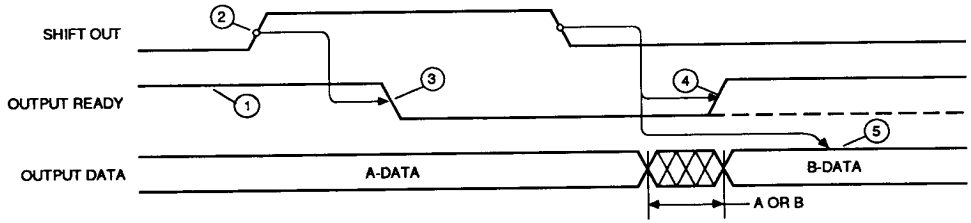
Figure 3. Data Is Shifted In Whenever Shift In and Input Ready Are Both HIGH



(1) The diagram assumes that at this time, words 63, 62 and 61 are loaded with A, B and C Data, respectively.

505 176 (2) Output data changes on the falling edge of SO after a valid Shift-Out Sequence, i.e., OR and SO ar both high together.

Figure 4. Output Timing



(1) Ouput Ready HIGH indicates that data is available and a Shift-Out pulse may be applied.
(2) Shift-Out goes HIGH causing the contents of word 62 (B-DATA) to be released for fall through to word 63. Output data remains as valid A-Data while Shift-Out is HIGH.
(3) Output Ready goes LOW.
(4) Shift-out goes LOW causing Output Ready to go HIGH and new data (B) to appear at the data outputs.
(5) If the FIFO has only one word loaded (A-Data) then Output Ready stays LOW and the output data becomes invalid.

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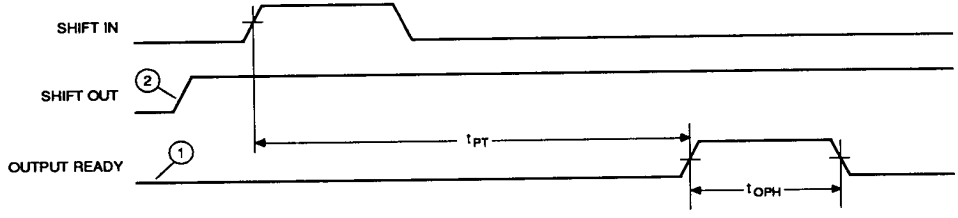
Figure 5. The Mechanism of Shifting Data Out of the FIFO



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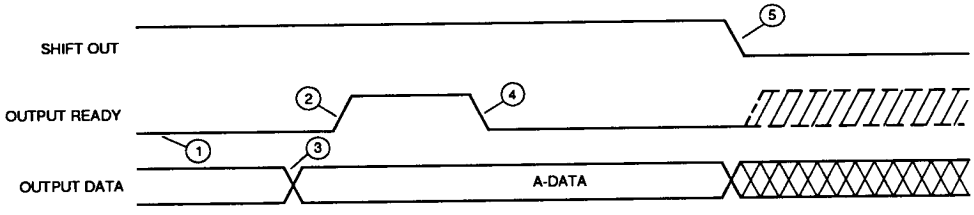
(1) FIFO is initially empty
(2) Shift Out held HIGH.

Figure 6. t_{PT} and t_{OPH} Specification



(1) Word 63 is empty.
(2) Output Ready goes HIGH indicating arrival of the new data.
(3) New data (A) arrives at the outputs (word 63).
(4) Since Shift Out is held HIGH, Output Ready goes immediately LOW.
(5) As soon as Shift Out goes LOW the Output Data is subject to change. Output Ready will go HIGH or LOW depending on whether there are any additional upstream words in the FIFO.

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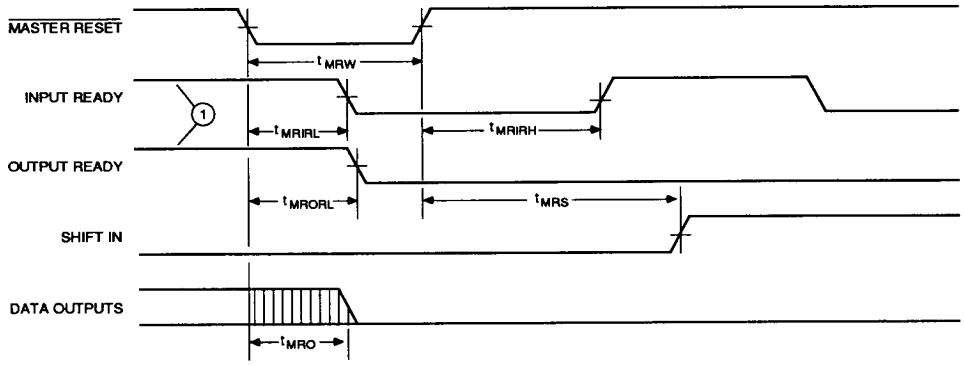
Figure 7. Data Is Shifted Out Whenever Shift Out and Output Ready Are Both HIGH



505 180 ① FIFO is initially full.

Figure 8. Master Reset Timing