REVISIONS			
LTR	DESCRIPTION	DATE (YR-MO-DA)	APPROVED
D	Add device types 03 and 04. Add test circuit. Editorial changes thougout.	90-03-05	W. Heckman
E	Change 1.3. Convert to one part-one part number format.	91-02-08	W. Heckman
F	Changes in accordance with NOR 5962-R323-92	92-09-26	Monica L. Poelking
G	Changes in accordance with NOR 5962-R052-93	92-12-18	Monica L. Poelking
H	Add device types 05-08. Add packages M, U, and V. Add class N designator. Editorial changes thoughout.	96-08-23	Monica L. Poelking

CURRENT CAGE CODE 67268

THE ORIGINAL FIRST PAGE OF THIS DRAWING HAS BEEN REPLACED.

REV															
SHEET															
REV	H	H	H	H	H	H	H	H	H	H					
SHEET	15	16	17	18	19	20	21	22	23	24					

REV STATUS OF SHEETS															
REV	H	H	H	H	H	H	H	H	H	H	H	H	H	H	
SHEET	1	2	3	4	5	6	7	8	9	10	11	12	13	14	

PMIC N/A

PREPARED BY Greg A Pitz

DEFENSE SUPPLY CENTER COLUMBUS
COLUMBUS, OHIO 43216

STANDARD MICROCIRCUIT DRAWING

THIS DRAWING IS AVAILABLE FOR USE BY ALL DEPARTMENTS AND AGENCIES OF THE DEPARTMENT OF DEFENSE

AMSC N/A

CHECKED BY Wm J. Johnson

APPROVED BY Michael A. Frye

DRAWING APPROVAL DATE 86-02-14

REVISION LEVEL H

MICROCIRCUIT, DIGITAL, CMOS 8-BIT CONTROL-ORIENTED MICROCOMPUTER/MICROCONTROLLER, MONOLITHIC SILICON

SIZE	CAGE CODE	
A	14933	85064

SHEET 1 OF 24

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5962-E361-96

1. SCOPE

1.1 Scope. This drawing documents three product assurance class levels consisting of space application (device class V), high reliability (device classes M and Q), and nontraditional performance environment (device class N). A choice of case outlines and lead finishes are available and are reflected in the Part or Identifying Number (PIN). When available, a choice of Radiation Hardness Assurance (RHA) levels are reflected in the PIN. For device class N, the user is cautioned to assure that the device is appropriate for the application environment.

1.2 PIN. The PIN is as shown in the following example:

5962	-	85064	01	M	M	X
Federal stock class designator	RHA designator (see 1.2.1)		Device type (see 1.2.2)	Device class designator (see 1.2.3)	Case outline (see 1.2.4)	Lead finish (see 1.2.5)

________ V ________/
Drawing number

1.2.1 RHA designator. Device classes N, Q, and V RHA marked devices meet the MIL-PRF-38535 specified RHA levels and are marked with the appropriate RHA designator. Device class M RHA marked devices meet the MIL-PRF-38535, appendix A specified RHA levels and are marked with the appropriate RHA designator. A dash (-) indicates a non-RHA device.

1.2.2 Device type(s). The device type(s) identify the circuit function as follows:

Device type	Generic number	Circuit function
01	80C31BH	8-bit microcontroller (3.5 to 12 MHz)
02	80C51BH	8-bit microcontroller with a mask programmable ROM (3.5 to 12 MHz)
03	80C31BH-16	8-bit microcontroller (3.5 to 16 MHz)
04	80C51BH-16	8-bit microcontroller with a mask programmable ROM (3.5 to 16 MHz)
05	80C31BH	8-bit microcontroller (3.5 to 12 MHz)
06	80C51BH	8-bit microcontroller with a mask programmable ROM (3.5 to 12 MHz)
07	80C31BH-16	8-bit microcontroller (3.5 to 16 MHz)
08	80C51BH-16	8-bit microcontroller with a mask programmable ROM (3.5 to 16 MHz)

1.2.3 Device class designator. The device class designator is a single letter identifying the product assurance level as follows:

Device class	Device requirements documentation
M	Vendor self-certification to the requirements for MIL-STD-883 compliant, non-JAN class level B microcircuits in accordance with MIL-PRF-38535, appendix A
N	Certification and qualification to MIL-PRF-38535 with a nontraditional performance environment 1/
Q or V	Certification and qualification to MIL-PRF-38535

1/ Any device outside the traditional performance environment; e.g., an operating temperature range of -55°C to +125°C and which requires hermetic packaging.

1.2.4 Case outline(s). The case outline(s) are as designated in MIL-STD-1835 and as follows:

Outline letter	Descriptive designator	Terminals	Package style
M	GQCC1-J44	44	"J" leaded chip carrier
Q	GDIP1-T40 or CDIP2-T40	40	Dual-in-line package
U	MS-011-AC 2/	40	Plastic dual-in-line package
V	MS-018-AC 2/	44	Plastic "J" leaded chip carrier
X	CQCC1-N44	44	Square chip carrier package
Y	(See figure 1)	52	Flat package

1.2.5 Lead finish. The lead finish is as specified in MIL-PRF-38535 for device classes N, Q, and V or MIL-PRF-38535, appendix A for device class M.

1.3 Absolute maximum ratings. 3/

Supply voltage range (referenced to ground)	+6.5 V dc maximum
Maximum power dissipation (P_D)	200 mW
Voltage (any pin) to V_{SS}	-0.5 V dc to V_{CC} +0.5 V dc
Storage temperature range (T_{STG})	-65°C to +150°C
Maximum junction temperature (T_J)	+200°C
Lead temperature (soldering 5 seconds) (T_S)	+300 °C
Thermal resistance junction-to-case (θ_{JC}):	
Case M, Q, and X	See MIL-STD-1835
Case Y	20°C/W
Case U	15°C/W
Case V	14°C/W

1.4 Recommended operating conditions.

Operating supply voltage range (V_{CC})	4 V dc to +6 V dc
Maximum low level input voltage (except EA)	0.2 V_{CC} - 0.25 V dc
(EA)	0.2 V_{CC} - 0.45 V dc
Maximum high level input voltage (except XTAL1, RST)	0.2 V_{CC} + 1.1 V dc
(XTA1, RST)	0.7 V_{CC} + 0.2 V dc
Case operating temperature range (T_C)	
Device types 01, 02, 03, and 04	-55°C to +125°C
Device types 05, 06, 07, and 08	-40°C to +85°C
Oscillator frequency	
Device types 01, 02, 05, and 06	3.5 MHz to 12 MHz
Device types 03, 04, 07, and 08	3.5 MHz to 16 MHz

1.5 Digital logic testing for device classes Q and V.

Fault coverage measurement of manufacturing logic tests (MIL-STD-883, test method 5012) --------- XX percent 4/

2/ See JEDEC Publication 95.
3/ Stresses above the absolute maximum rating may cause permanent damage to the device. Extended operation at the maximum levels may degrade performance and affect reliability.
4/ Values will be added when they become available.

2. APPLICABLE DOCUMENTS

2.1 Government specification, standards, and handbooks. The following specification, standards, and handbooks form a part of this drawing to the extent specified herein. Unless otherwise specified, the issues of these documents are those listed in the issue of the Department of Defense Index of Specifications and Standards (DoDISS) and supplement thereto, cited in the solitation.

SPECIFICATION

MILITARY

MIL-PRF-38535 - Integrated Circuits, Manufacturing, General Specification for.

STANDARDS

MILITARY

MIL-STD-883 - Test Methods and Procedures for Microelectronics.
MIL-STD-973 - Configuration Management.
MIL-STD-1835 - Microcircuit Case Outlines.

HANDBOOKS

MILITARY

MIL-HDBK-103 - List of Standard Microcircuit Drawings (SMD's).
MIL-HDBK-780 - Standard Microcircuit Drawings.

(Unless otherwise indicated, copies of the specification, standards, bulletin, and handbook are available from the Standardization Document Order Desk, 700 Robbins Avenue, Building 4D, Philadelphia, PA 19111-5094.)

2.2 Non-Government publication. The following document forms a part of this document to the extent specified herein. Unless otherwise specified, the issues of the documents which are DoD adopted are those listed in the issue of the DODISS cited in the sloicitaion. Unless otherwise specified, the issues of documents not listed in the DODISS are the issues of the documents cited in the solicitation.

ELECTRONICS INDUSTRIES ASSOCIATION (EIA)

JEDEC Publication 95 - Registered and Standard Outlines for Semiconductor Devices.

(Applications for copies should be addressed to the Electronic Industry Association, 2500 Wilson Boulevard, Arlington, VA 2201-3834).

2.3 Order of precedence. In the event of a conflict between the text of this drawing and the references cited herein, the text of this drawing takes precedence. Nothing in this document, however, supersedes applicable laws and regulations unless a specific exemption has been obtained.

3. REQUIREMENTS

3.1 Item requirements. The individual item requirements for device classes N, Q, and V shall be in accordance with MIL-PRF-38535 and as specified herein or as modified in the device manufacturer's Quality Management (QM) plan. The modification in the QM plan shall not affect the form, fit, or function as described herein. The individual item requirements for device class M shall be in accordance with MIL-PRF-38535, appendix A for non-JAN class level B devices and as specified herein.

3.2 Design, construction, and physical dimensions. The design, construction, and physical dimensions shall be as specified in MIL-PRF-38535 and herein for device classes N, Q, and V or MIL-PRF-38535, appendix A and herein for device class M.

3.2.1 Case outline(s). The case outline(s) shall be in accordance with 1.2.4 herein and figure 1.

3.2.2 Terminal connections. The terminal connections shall be as specified on figure 2.

3.2.3 Block diagram. The block diagram(s) shall be as specified on figure 3.

3.2.4 Radiation exposure circuit. The radiation exposure circuit shall be as specified when available.

3.3 Electrical performance characteristics and postirradiation parameter limits. Unless otherwise specified herein, the electrical performance characteristics and postirradiation parameter limits are as specified in table I and shall apply over the full case operating temperature range.

3.4 Electrical test requirements. The electrical test requirements shall be the subgroups specified in table II. The electrical tests for each subgroup are defined in table I.

3.5 Marking. The part shall be marked with the PIN listed in 1.2 herein. In addition, the manufacturer's PIN may also be marked as listed in MIL-HDBK-103. For packages where marking of the entire SMD PIN number is not feasible due to space limitations, the manufacturer has the option of not marking the "5962-" on the device. For RHA product using this option, the RHA designator shall still be marked. Marking for device classes N, Q, and V shall be in accordance with MIL-PRF-38535. Marking for device class M shall be in accordance with MIL-PRF-38535, appendix A.

3.5.1 Certification/compliance mark. The certification mark for device classes N, Q, and V shall be a "QML" or "Q" as required in MIL-PRF-38535. The compliance mark for device class M shall be a "C" as required in MIL-PRF-38535, appendix A.

3.6 Certificate of compliance. For device classes N, Q, and V, a certificate of compliance shall be required from a QML-38535 listed manufacturer in order to supply to the requirements of this drawing (see 6.6.1 herein). For device class M, a certificate of compliance shall be required from a manufacturer in order to be listed as an approved source of supply in MIL-HDBK-103 (see 6.6.2 herein). The certificate of compliance submitted to DSCC-VA prior to listing as an approved source of supply for this drawing shall affirm that the manufacturer's product meets, for device classes N, Q, and V, the requirements of MIL-PRF-38535 and herein or for device class M, the requirements of MIL-PRF-38535, appendix A and herein.

3.7 Certificate of conformance. A certificate of conformance as required for device classes N, Q, and V in MIL-PRF-38535 or for device class M in MIL-PRF-38535, appendix A shall be provided with each lot of microcircuits delivered to this drawing.

3.8 Notification of change for device class M. For device class M, notification to DSCC-VA of change of product (see 6.2 herein) involving devices acquired to this drawing is required for any change as defined in MIL-STD-973.

3.9 Verification and review for device class M. For device class M, DSCC, DSCC's agent, and the acquiring activity retain the option to review the manufacturer's facility and applicable required documentation. Offshore documentation shall be made available onshore at the option of the reviewer.

3.10 Microcircuit group assignment for device class M. Device class M devices covered by this drawing shall be in microcircuit group number 105 (see MIL-PRF-38535, appendix A).

3.11 User mask program. For devices 02, 04, 06, and 08 since the ROM is memory programmed by the manufacturer in a variety of configurations, the contracting activity shall provide an altered item drawing describing the mask program to be used by the manufacturer. This drawing shall consist of the desired mask program supplied on one or more of the following media: Truth table, floppy disk, or EPROM.

3.12 PIN supersession information. The PIN supersession information shall be as specified in the appendix.

TABLE I. Electrical performance characteristics.

Test	Symbol	Conditions 1/ V_{CC} = 5 V ±20% unless otherwise specified	Group A subgroups	Device type	Limits		Unit
					Min	Max	
Output low voltage (ports 1,2,3)	V_{OL}	I_{OL} = 1.6 mA 2/	1,2,3	All		0.45	V
Output low voltage (port 0, ALE, PSEN)	V_{OL1}	I_{OL} = 3.2 mA 2/	1,2,3	All		0.45	V
Output high voltage (ports 1,2,3)	V_{OH}	I_{OH} = -60 µA, V_{CC} = 5 V ±10%	1,2,3	All	2.4		V
		I_{OH} = -25 µA, V_{CC} = 5 V ±10%			0.75 V_{CC}		
		I_{OH} = -10 µA, V_{CC} = 5 V ±10%			0.90 V_{CC}		
Output high voltage (port 0 in external bus mode, ALE, PSEN)	V_{OH1}	I_{OH} = -400 µA, V_{CC} = 5 V ±10%	1,2,3	All	2.4		V
		I_{OH} = -150 µA, V_{CC} = 5 V ±10%			0.75 V_{CC}		
		I_{OH} = -40 µA, V_{CC} = 5 V ±10% 3/			0.90 V_{CC}		
Logical 0 input current (ports 1, 2, 3)	I_{IL}	V_{IN} = 0.45 V	1,2,3	All		-75	µA
Logical 1 to 0 transition current (ports 1, 2, 3)	I_{TL}	V_{IN} = 2 V	1,2,3	All		-750	µA
Input leakage current (port 0, EA)	I_{LI}	0.45 < V_{IN} < V_{CC}	1,2,3	All		±10	µA
Supply current during operation 4/	I_{CC1}	3.5 MHz, V_{CC} 4 V 3.5 MHz, V_{CC} 5 V 5/ 3.5 MHz, V_{CC} 6 V 8.0 MHz, V_{CC} 4 V 5/ 8.0 MHz, V_{CC} 5 V 5/ 8.0 MHz, V_{CC} 6 V 5/ 12 MHz, V_{CC} 4 V 12 MHz, V_{CC} 5 V 5/ 12 MHz, V_{CC} 6 V	1,2,3	All		4.3 5.7 7.5 8.3 11 14 12 16 20	mA
Supply current during operation	I_{CC2}	16 MHz, V_{CC} 4 V 16 MHz, V_{CC} 5 V 5/ 16 MHz, V_{CC} 6 V	1,2,3	03,04 07,08		16 21 25	mA

See footnotes at end of table.

TABLE I. Electrical performance characteristics - Continued.

Test	Symbol	Conditions 1/ V_{CC} = 5 V ±20% unless otherwise specified	Group A subgroups	Device type	Limits Min	Limits Max	Unit
Supply current during idle mode 6/	I_{CC3}	3.5 MHz, V_{CC} 4 V 3.5 MHz, V_{CC} 5 V 5/ 3.5 MHz, V_{CC} 6 V 8.0 MHz, V_{CC} 4 V 5/ 8.0 MHz, V_{CC} 5 V 5/ 8.0 MHz, V_{CC} 6 V 5/ 12 MHz, V_{CC} 4 V 12 MHz, V_{CC} 5 V 5/ 12 MHz, V_{CC} 6 V	1,2,3	All		1.1 1.6 2.2 1.8 2.7 3.7 2.5 3.7 5.0	mA
	I_{CC4}	16 MHz, V_{CC} 4 V 16 MHz, V_{CC} 5 V 5/ 16 MHz, V_{CC} 6 V		03,04 07,08		4.0 5.5 7.0	
Power down current	I_{PD}	V_{CC} 2 V to 6 V 7/	1,2,3	All		75	µA
Reset pulldown resistor	R_{RST}		1,2,3	All	50	150	kΩ
Pin capacitance	C_{IO}	See 4.4.1c	4	All		10	pF
Functional tests		See 4.4.1d	7,8	All			
Oscillator frequency	$1/t_{CLCL}$		9,10,11	01,02 05,06	3.5	12	MHz
				03,04 07,08	3.5	16	
ALE pulse width	t_{LHLL}	C_L = 100 pF for port 0, ALE, and $\overline{PSEN}$ C_L = 80 pF for all other outputs (see figure 4)	9,10,11	All	$2t_{CLCL-55}$		ns
Address valid to ALE low	t_{AVLL} 8/				$t_{CLCL-70}$		
Address hold after ALE low	t_{LLAX}				$t_{CLCL-50}$		
ALE low to valid instruction in	t_{LLIV}					$4t_{CLCL-115}$	
ALE low to $\overline{PSEN}$ low	t_{LLPL}				$t_{CLCL-55}$		
$\overline{PSEN}$ pulse width	t_{PLPH}				$3t_{CLCL-60}$		
$\overline{PSEN}$ low to valid instruction in	t_{PLIV}					$3t_{CLCL-120}$	
Input instruction hold after $\overline{PSEN}$	t_{PXIX}				0		
Input instruction float after $\overline{PSEN}$	t_{PXIZ}					$t_{CLCL-120}$	

See footnotes at end of table.

TABLE I. Electrical performance characteristics - Continued.

Test	Symbol	Conditions 1/ V_{CC} = 5 V ±20% unless otherwise specified	Group A subgroups	Device type	Limits		Unit
					Min	Max	
Address to valid instruction in	t_{AVIV}	C_L = 100 pF for port 0, ALE, and PSEN C_L = 80 pF for all other outputs (see figure 4)	9,10,11	All		$5t_{CLCL}$-120	ns
$\overline{PSEN}$ low to address float	t_{PLAZ}					25	
$\overline{RD}$ pulse width	t_{RLRH}				$6t_{CLCL}$-100		
$\overline{WR}$ pulse width	t_{WLWH}				$6t_{CLCL}$-100		
$\overline{RD}$ low to valid data in	t_{RLDV}					$5t_{CLCL}$-185	
Data hold after RD	t_{RHDX}				0		
Data float after RD	t_{RHDZ}					$2t_{CLCL}$-85	
ALE low to valid data in	t_{LLDV}					$8t_{CLCL}$-170	
Address valid to data in	t_{AVDV}					$9t_{CLCL}$-185	
ALE low to $\overline{RD}$ or WR low	t_{LLWL}				$3t_{CLCL}$-65	$3t_{CLCL}$+65	
Address to $\overline{RD}$ or WR low	t_{AVWL}				$4t_{CLCL}$-145		
Data valid to WR transition	t_{QVWX}				t_{CLCL}-75		
Data holds after WR	t_{WHQX}				t_{CLCL}-65		
$\overline{RD}$ low to address float	t_{RLAZ}					0	
$\overline{RD}$ or $\overline{WR}$ high to high	t_{WHLH}				t_{CLCL}-65	t_{CLCL}+65	
External clock high time	t_{CHCX}				20		
External clock low time	t_{CLCX}				20		
External clock rise time	t_{CLCH} 9/					20	
External clock fall time	t_{CHCL} 9/					20	
Serial port clock cycle time	t_{XLXL} 5/				$12t_{CLCL}$		

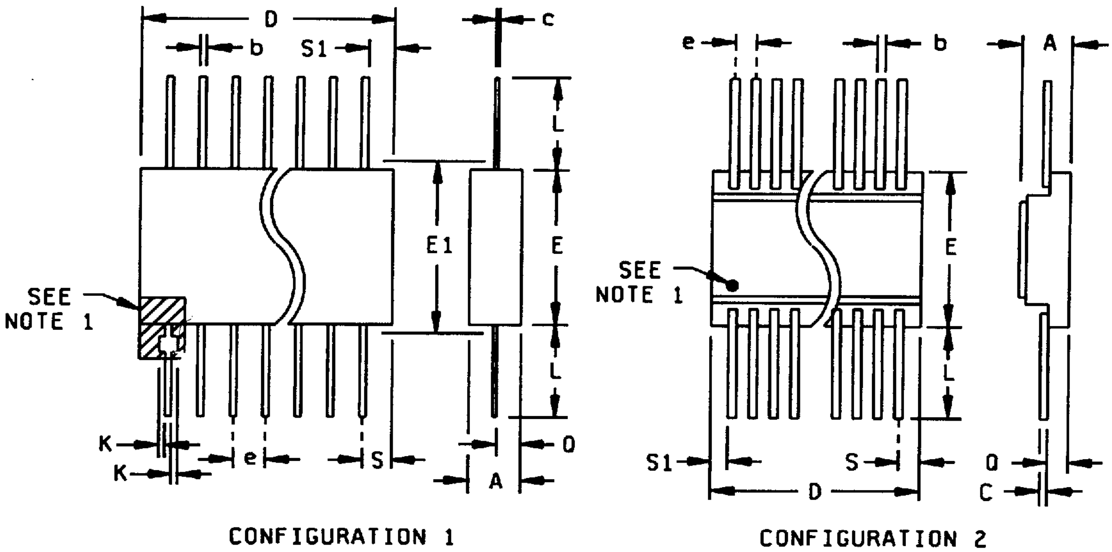
See footnotes at end of table.

TABLE I. Electrical performance characteristics - Continued.

Test	Symbol	Conditions 1/ V_{CC} = 5 V ±20% unless otherwise specified	Group A subgroups	Device type	Limits		Unit
					Min	Max	
Output datà setup to clock rising edge	t_{QVXH} 5/	C_L = 100 pF for port 0, ALE, and PSEN C_L = 80 pF for all other outputs (see figure 4)	9,10,11	All	$10t_{CLCL-133}$		ns
Output data hold after clock rising edge	t_{XHQX} 5/				$2t_{CLCL-117}$		
Input data hold after clock rising edge	t_{XHDX} 5/				0		
Clock rising edge to input data valid	t_{XHDV} 5/					$10t_{CLCL-133}$	

1/ Unless otherwise specified, all testing to be performed using worst case conditions. The operating temperature shall be as specified in section 1.4.
2/ Capacitive loading on ports 0 and 2 may cause spurious noise pulses to be superimposed on the V_{OL} of ALE and ports 1 and 3. The noise is due to external bus capacitance discharging into the port 0 and port 2 pins when these pins make 1-to-0 transitions during bus operations. In the worst cases (capacitive loading > 100 pF), the noise pulse on the ALE line may exceed 0.8 V. In such cases it may be desirable to qualify ALE with a Schmitt Trigger, or use an address latch with a Schmitt Trigger STROBE input.
3/ Capacitive loading on ports 0 and 2 may cause the V_{OH} on ALE and $\overline{PSEN}$ to momentarily fall below the 0.9 V_{CC} specification when the address bits are stabilizing.
4/ I_{CC} is measured with all output pins disconnected; XTAL1 driven with t_{CLCH}, t_{CHCL} = 5 ns, V_{IL} = V_{SS} + 0.5 V, I_{CC} would be slightly higher if a crystal oscillator is used.
5/ Shall be guaranteed if not tested to the limits specified.
6/ Idle I_{CC} is measured with all output pins disconnected; XTAL1 driven with t_{CLCH}, t_{CHCL} = 5 ns, V_{IL} = V_{SS} + 0.5 V, XTAL2 N.C.; Port 0 = V_{CC}; EA = RST = V_{SS}.
7/ Power down I_{CC} is measured with all output pins disconnected; EA = PORT, 0 = V_{CC}; XTAL2 N C.; RST = V_{SS}.
8/ When using timing equations, the minimum value shall be not less than 5 ns.
9/ Due to test equipment limitations, actual tested values may differ from those specified, but specified limits are guaranteed.

Case Y



Ltr	Inches		Millimeters		Notes
	Min	Max	Min	Max	
A	.045	.100	1.14	2.54	
b	.015	.023	0.38	0.58	
c	.008	.012	0.20	0.30	
D		1.330		33.78	2
E	.620	.660	15.75	16.76	
E1					2
e	.050 BSC		1.27 BSC		3

Symbol	Inches		Millimeters		Notes
	Min	Max	Min	Max	
K					
L	.250	.370	6.35	9.40	
Q	.054	.066	1.37	16.76	4
S		.045		1.14	
S1	.005		0.13		
∝					

NOTES:
1. A pin 1 tab (enlargement) is located with the shaded area shown and adjacent to the package body. Other pin numbers proceed sequentially from pin 1 counterclockwise (as viewed from the top of the device).
2. This dimension allows for off-center lid, meniscus, and glass overrun.
3. The reference pin spacing is 0.050 between centerlines. Each pin centerline is located within ±0.005 of its longitudinal position relative to the first and last pin numbers.
4. This dimension is measured at the point of exit of the lead body.

FIGURE 1. Case outline

Case Q, U

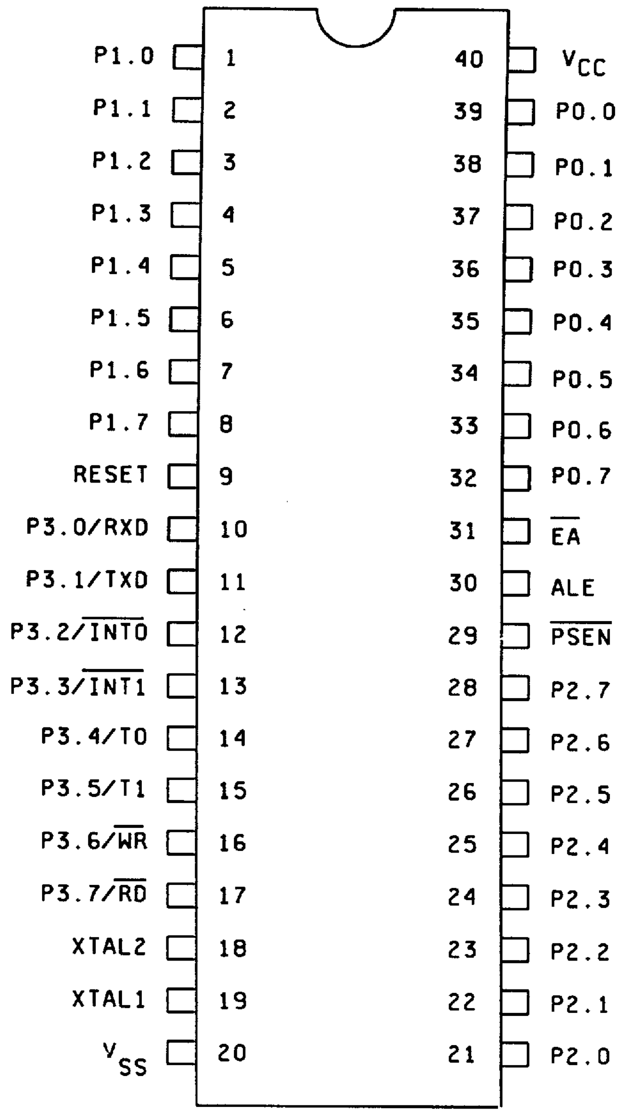


FIGURE 2. Terminal connections.

STANDARD MICROCIRCUIT DRAWING DEFENSE SUPPLY CENTER COLUMBUS COLUMBUS, OHIO 43216	SIZE A		85064
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Case M, X and V

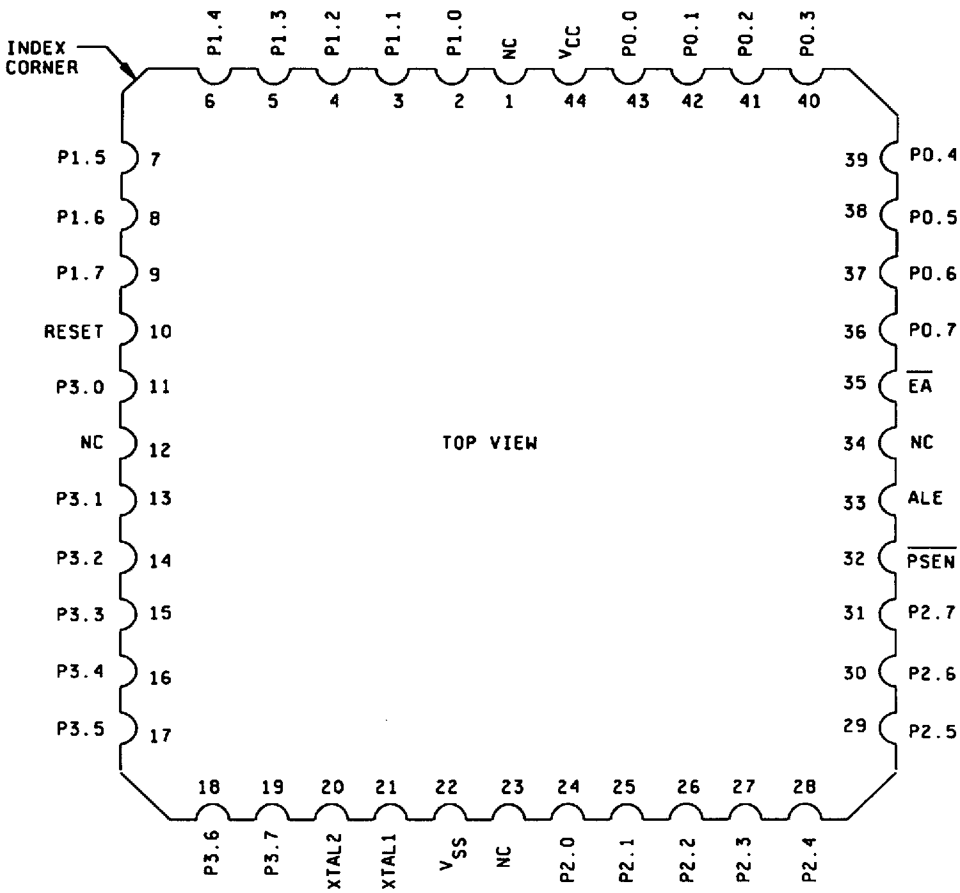

FIGURE 2. Terminal connections - Continued.

Case Y

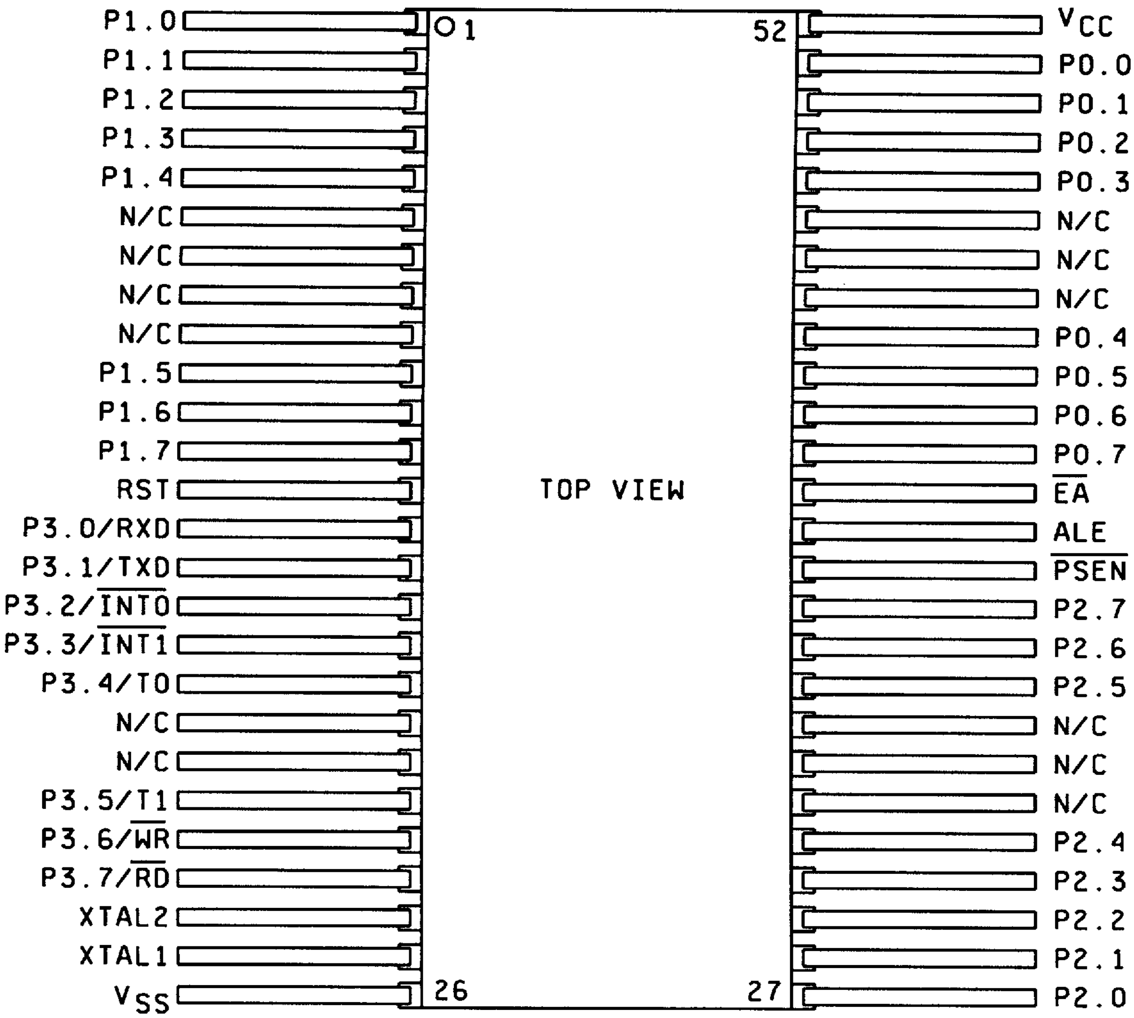

FIGURE 2. Terminal connections - Continued.

STANDARD MICROCIRCUIT DRAWING DEFENSE SUPPLY CENTER COLUMBUS COLUMBUS, OHIO 43216	SIZE **A**		**85064**
		REVISION LEVEL	SHEET **13**

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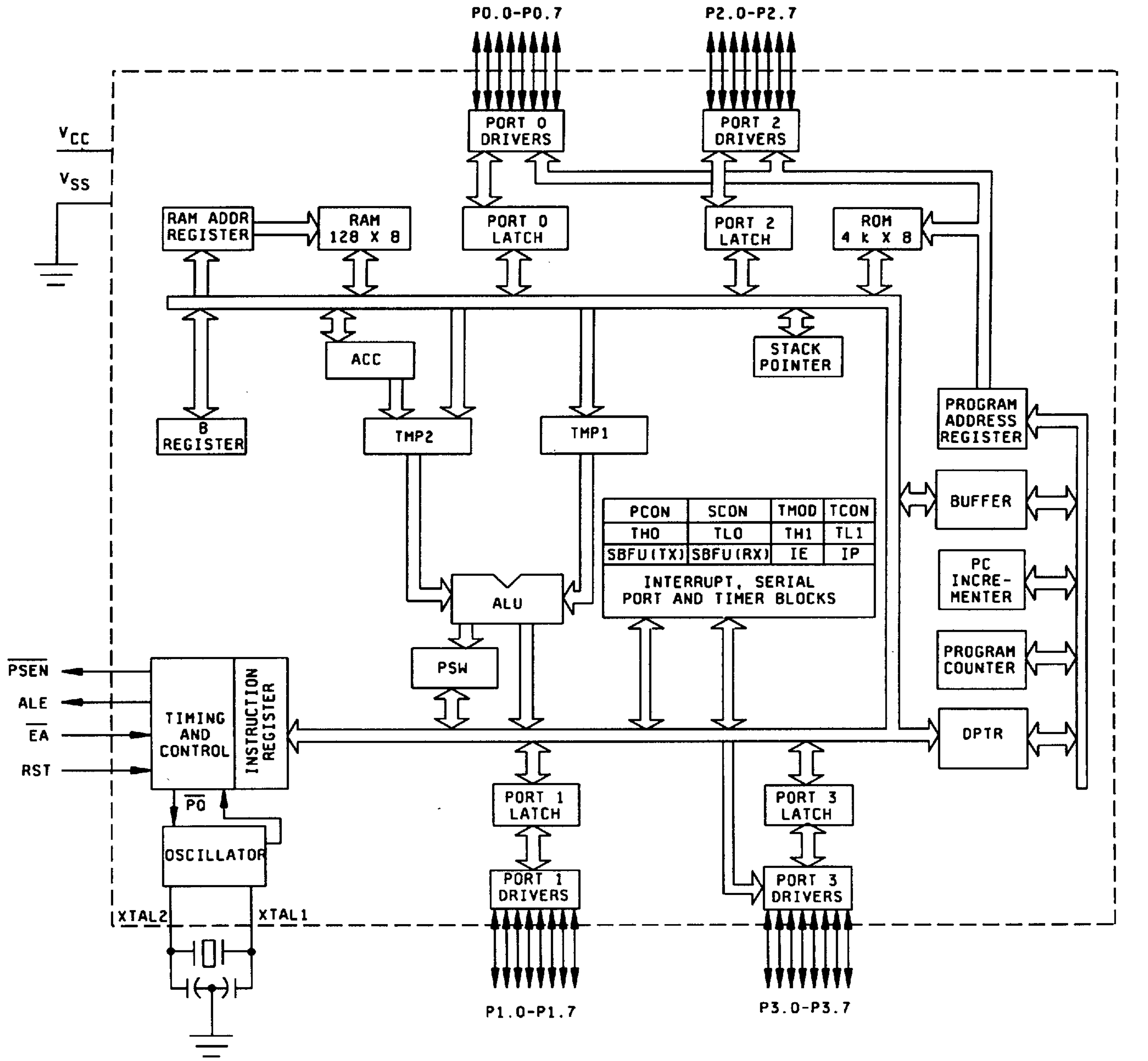
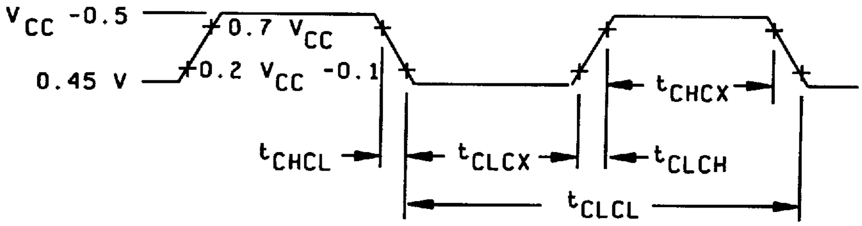
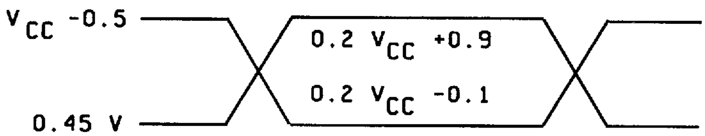


Mode	Program memory	ALE	PSEN	Port 0	Port 1	Port 2	Port 3
Idle	Internal	1	1	Data	Data	Data	Data
Idle	External	1	1	Float	Data	Address	Data
Power down	Internal	0	0	Data	Data	Data	Data
Power down	External	0	0	Float	Data	Data	Data

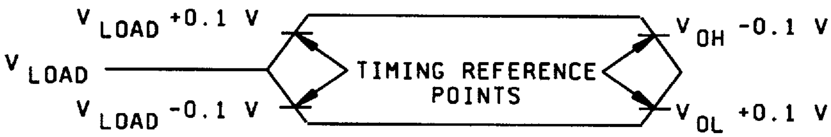
FIGURE 3. Block diagram.



EXTERNAL CLOCK DRIVE WAVEFORM



AC TESTING: INPUT, OUTPUT WAVEFORMS

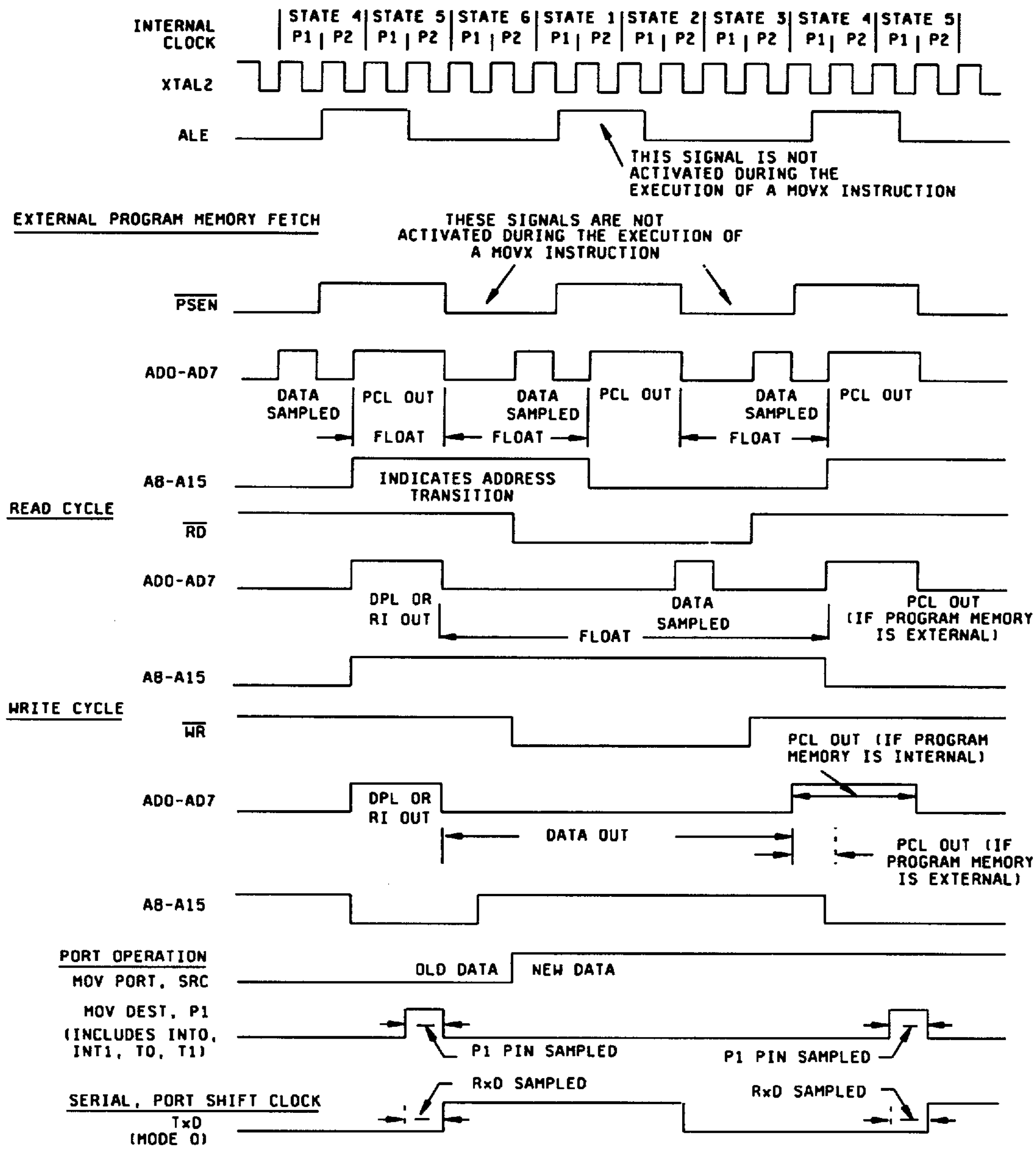


FLOAT WAVEFORM

NOTES:

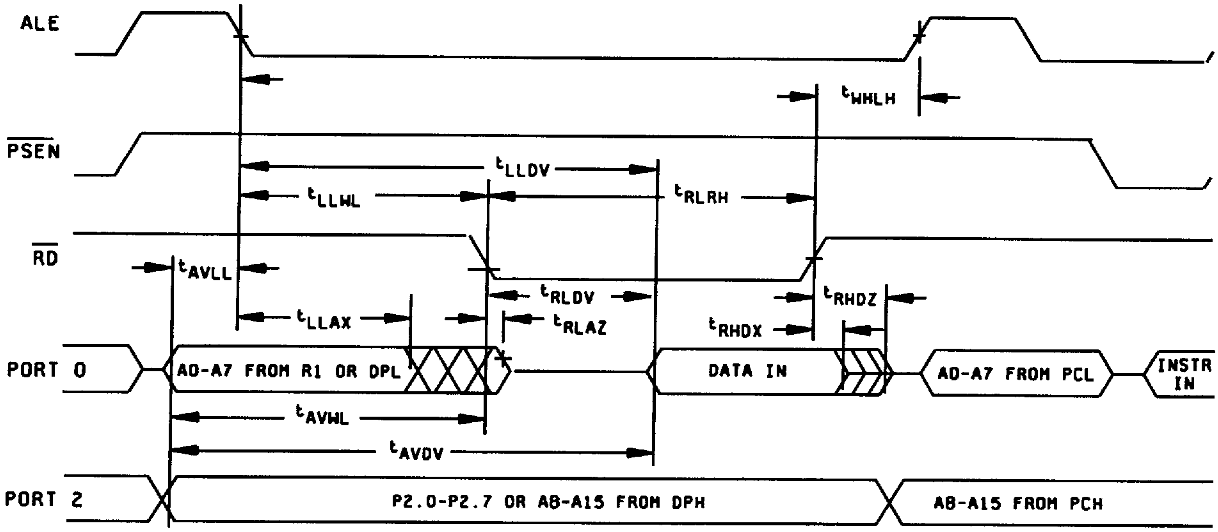
1. AC inputs during testing are driven at V_{CC} - 0.5 for a logic "1" and 0.45 V for a logic "0". Timing measurements are made at V_{IH} minimum for a logic "1" and V_{IL} maximum for a logic "0".
2. For timing purposes a port pin is no longer floating when a 100 mV change from load voltage occurs and begins to float when a 100 mV change from the loaded V_{OH}/V_{OL} level occurs.
3. $I_{OL}/I_{OH} \geq \pm 20$ mA.

FIGURE 4. Switching waveforms and test circuit.

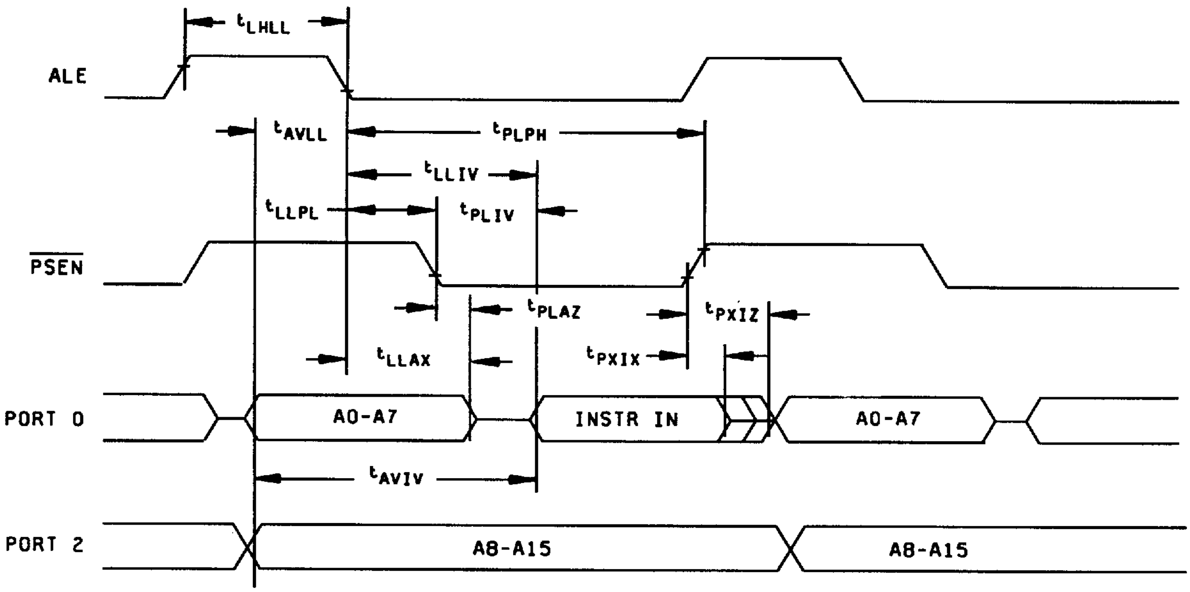


NOTE: This diagram indicates when signals are clocked internally. The time it takes the signals to propagate to the pins, however ranges from 25 to 125 ns. This propagation delay is dependent on variables such as temperature and pin loading. Propagation also varies from output to output and component to component. Typically though, (T_A = +25°C, fully loaded) RD and WR propagation delays are approximately 50 ns.
The other signals are typically 85 ns. Propagation delays are incorporated in the ac specifications.

FIGURE 4. Switching waveforms and test circuit - Continued.

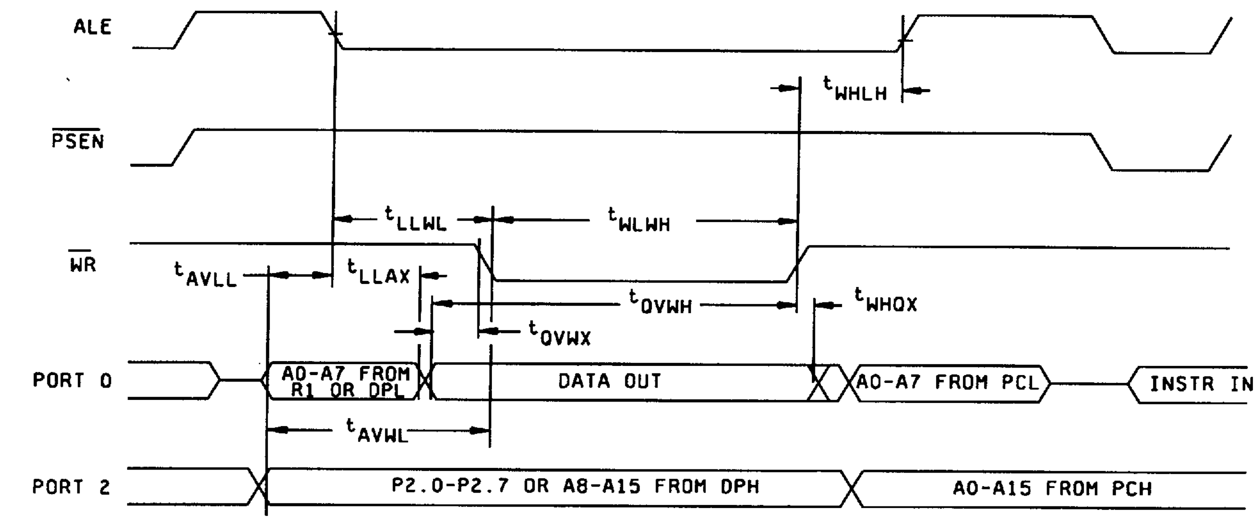


EXTERNAL DATA MEMORY READ CYCLE

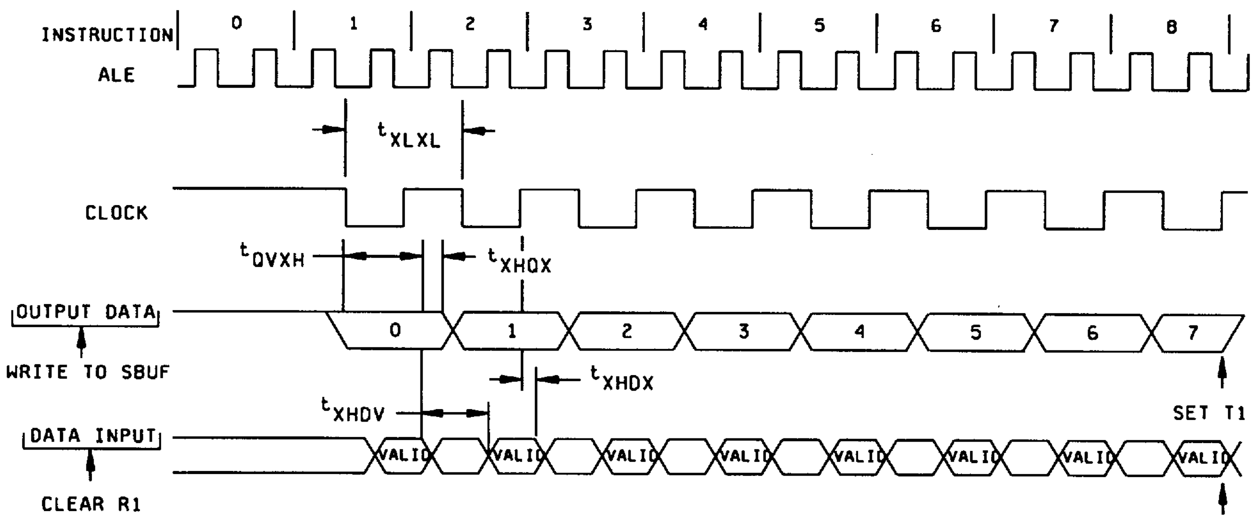


EXTERNAL PROGRAM MEMORY READ CYCLE

FIGURE 4. Switching waveforms and test circuit - Continued.

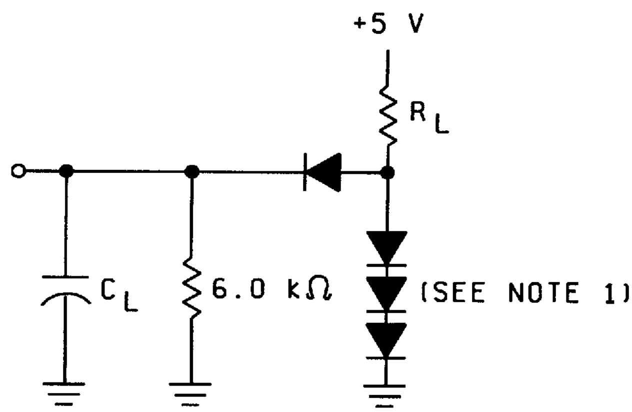


EXTERNAL DATA MEMORY WRITE CYCLE



SHIFT REGISTER MODE TIMING WAVEFORMS

FIGURE 4. Switching waveforms and test circuit - Continued.



Output	R_L	C_L
Port 0, ALE, $\overline{\text{PSEN}}$	1.2 kΩ	100 pF
All other outputs	2.4 kΩ	80 pF

NOTES:
1. All diodes are 1N914 or equivalent.
2. C_L includes tester and fixture capacitance.

FIGURE 4. Switching waveforms and test circuit - Continued.

4. QUALITY ASSURANCE PROVISIONS

4.1 Sampling and inspection. For device classes N, Q, and V, sampling and inspection procedures shall be in accordance with MIL-PRF-38535 or as modified in the device manufacturer's Quality Management (QM) plan. The modification in the QM plan shall not affect the form, fit, or function as described herein. For device class M, sampling and inspection procedures shall be in accordance with MIL-PRF-38535, appendix A.

4.2 Screening. For device classes N, Q, and V, screening shall be in accordance with MIL-PRF-38535, and shall be conducted on all devices prior to qualification and technology conformance inspection. For device class M, screening shall be in accordance with method 5004 of MIL-STD-883, and shall be conducted on all devices prior to quality conformance inspection.

4.2.1 Additional criteria for device class M.

a. Burn-in test, method 1015 of MIL-STD-883.

(1) Test condition A, B, C, or D. The test circuit shall be maintained by the manufacturer under document revision level control and shall be made available to the preparing or acquiring activity upon request. The test circuit shall specify the inputs, outputs, biases, and power dissipation, as applicable, in accordance with the intent specified in test method 1015 of MIL-STD-883.

(2) T_A = +125°C, minimum.

b. Interim and final electrical test parameters shall be as specified in table II herein.

c. For devices 02, 04, 06, and 08, all devices shall be mask programmed to the requirements of the altered item drawing prior to the initiation of any testing.

4.2.2 Additional criteria for device classes N, Q, and V.

a. The burn-in test duration, test condition and test temperature, or approved alternatives shall be as specified in the device manufacturer's QM plan in accordance with MIL-PRF-38535. The burn-in test circuit shall be maintained under document revision level control of the device manufacturer's Technology Review Board (TRB) in accordance with MIL-PRF-38535 and shall be made available to the acquiring or preparing activity upon request. The test circuit shall specify the inputs, outputs, biases, and power dissipation, as applicable, in accordance with the intent specified in test method 1015 of MIL-STD-883.

b. Interim and final electrical test parameters shall be as specified in table II herein.

c. Additional screening for device class V beyond the requirements of device class Q shall be as specified in MIL-PRF-38535, appendix B.

4.3 Qualification inspection for device classes N, Q, and V. Qualification inspection for device classes N, Q, and V shall be in accordance with MIL-PRF-38535. Inspections to be performed shall be those specified in MIL-PRF-38535 and herein for groups A, B, C, D, and E inspections (see 4.4.1 through 4.4.4).

4.4 Conformance inspection. Technology conformance inspection for classes N, Q, and V shall be in accordance with MIL-PRF-38535 including groups A, B, C, D, and E inspections and as specified herein except where option 2 of MIL-PRF-38535 permits alternate in-line control testing. Quality conformance inspection for device class M shall be in accordance with MIL-PRF-38535, appendix A and as specified herein. Inspections to be performed for device class M shall be those specified in method 5005 of MIL-STD-883 and herein for groups A, B, C, D, and E inspections (see 4.4.1 through 4.4.4).

4.4.1 Group A inspection.

a. Tests shall be as specified in table II herein.

b. Subgroups 5 and 6 in table I, method 5005 of MIL-STD-883 shall be omitted.

c. Subgroup 4 (C_{IO}, measurement) shall be measured only for the initial test and after process or design changes which may affect input capacitance. A minimum sample size of 5 devices with zero rejects shall be required.

d. For device class M, subgroups 7 and 8 tests shall be sufficient to verify the functionality of the device. For device classes N, Q, and V, subgroups 7 and 8 shall include verifying the functionality of the device; these tests shall have been fault graded in accordance with MIL-STD-883, test method 5012 (see 1.5 herein).

4.4.2 Group C inspection. The group C inspection end-point electrical parameters shall be as specified in table II herein.

TABLE II. Electrical test requirements.

Test requirements	Subgroups (in accordance with MIL-STD-883, method 5005, table I)	Subgroups (in accordance with MIL-PRF-38535, table III)		
	Device class M	Device class N	Device class Q	Device class V
Interim electrical parameters (see 4.2)				1,7,9
Final electrical parameters (see 4.2)	1,2,3,7,8, 9,10,11 1/	1,2,3,7,8, 9,10,11 1/	1,2,3,7,8, 9,10,11 1/	1,2,3,7,8, 9,10,11 2/
Group A test requirements (see 4.4)	1,2,3,4,7,8,9,10,11	1,2,3,4,7,8,9, 10,11	1,2,3,4,7,8,9, 10,11	1,2,3,4,7,8,9, 10,11
Group C end-point electrical parameters (see 4.4)	2,8A,10	2,8A,10	2,8A,10	2,8A,10
Group D end-point electrical parameters (see 4.4)	2,8A,10	2,8A,10	2,8A,10	2,8A,10
Group E end-point electrical parameters (see 4.4)	1,7,9	1,7,9	1,7,9	1,7,9

1/ PDA applies to subgroup 1.
2/ PDA applies to subgroups 1 and 7.

4.4.2.1 Additional criteria for device class M. Steady-state life test conditions, method 1005 of MIL-STD-883:

a. Test condition A, B, C, or D. The test circuit shall be maintained by the manufacturer under document revision level control and shall be made available to the preparing or acquiring activity upon request. The test circuit shall specify the inputs, outputs, biases, and power dissipation, as applicable, in accordance with the intent specified in test method 1005 of MIL-STD-883.

b. T_A = +125°C, minimum.

c. Test duration: 1,000 hours, except as permitted by method 1005 of MIL-STD-883.

4.4.2.2 Additional criteria for device classes N, Q, and V. The steady-state life test duration, test condition and test temperature, or approved alternatives shall be as specified in the device manufacturer's QM plan in accordance with MIL-PRF-38535. The test circuit shall be maintained under document revision level control by the device manufacturer's TRB, in accordance with MIL-PRF-38535, and shall be made available to the acquiring or preparing activity upon request. The test circuit shall specify the inputs, outputs, biases, and power dissipation, as applicable, in accordance with the intent specified in test method 1005 of MIL-STD-883.

4.4.3 Group D inspection. The group D inspection end-point electrical parameters shall be as specified in table II herein.

4.4.4 Group E inspection. Group E inspection is required only for parts intended to be marked as radiation hardness assured (see 3.5 herein).

a. End-point electrical parameters shall be as specified in table II herein.

b. For device classes N, Q, and V, the devices or test vehicle shall be subjected to radiation hardness assured tests as specified in MIL-PRF-38535 for the RHA level being tested. For device class M, the devices shall be subjected to radiation hardness assured tests as specified in MIL-PRF-38535, appendix A for the RHA level being tested. All device classes must meet the postirradiation end-point electrical parameter limits as defined in table I at T_A = +25°C ±5°C, after exposure, to the subgroups specified in table II herein.

c. When specified in the purchase order or contract, a copy of the RHA delta limits shall be supplied.

5. PACKAGING

5.1 Packaging requirements. The requirements for packaging shall be in accordance with MIL-PRF-38535 for device classes N, Q, and V or MIL-PRF-38535, appendix A for device class M.

6. NOTES

6.1 Intended use. Microcircuits conforming to this drawing are intended for use for Government microcircuit applications (original equipment), design applications, and logistics purposes.

6.1.1 Replaceability. Microcircuits covered by this drawing will replace the same generic device covered by a contractor-prepared specification or drawing.

6.1.2 Substitutability. Device class Q devices will replace device class M devices.

6.2 Configuration control of SMD's. All proposed changes to existing SMD's will be coordinated with the users of record for the individual documents. This coordination will be accomplished in accordance with MIL-STD-973 using DD Form 1692, Engineering Change Proposal.

6.3 Record of users. Military and industrial users should inform Defense Supply Center Columbus when a system application requires configuration control and which SMD's are applicable to that system. DSCC will maintain a record of users and this list will be used for coordination and distribution of changes to the drawings. Users of drawings covering microelectronic devices (FSC 5962) should contact DSCC-VA, telephone (614) 692-0525.

6.4 Comments. Comments on this drawing should be directed to DSCC-VA, Columbus, Ohio 43216-5000, or telephone (614) 692-0674.

6.5 Abbreviations, symbols, and definitions. The abbreviations, symbols, and definitions used herein are defined in MIL-PRF-38535 and MIL-STD-1331 and as follows:

Pin symbol	Description
Port 0	Port 0 is an 8-bit open drain bidirectional I/O port. Port 0 pins that have 1's written to them float, and in that state can be used as high-impedance inputs. Port 0 is also the multiplexed low-order address and data bus during accesses to external program and data memory. In this application it uses strong internal pullups when emitting 1's. Port 0 also outputs the code bytes during program verification in the 02 and 04 devices. External pullups are required during program verification.
Port 1	Port 1 is an 8-bit bidirectional I/O port with internal pullups. Port 1 pins that have 1's written to them are pulled high by the internal pullups, and in that state can be used as inputs. As inputs, port 1 pins that are externally being pulled low will source current (I_{IL}), because of the internal pullups. Port 1 also receives the low-order address bytes during program verification.
Port 2	Port 2 is an 8-bit bidirectional I/O port with internal pullups. Port 2 pins that have 1's written to them are pulled high by the internal pullups, and in that state can be used as inputs. As inputs, port 2 pins that are externally being pulled low will source current (I_{IL}), because of the internal pullups. Port 2 emits the high-order address byte during fetches from external program memory and during accesses to external data memory that use 16-bit addresses (MOVX at DPTR). In this application it uses strong internal pullups when emitting 1's. During accesses to external data memory that used 8-bit addresses (MOVX at Ri), port 2 emits the contents of the P2 special function register.
Port 3	Port 3 is an 8-bit bidirectional I/O port with internal pullups. Port 3 pins that have 1's written to them are pulled high by the internal pullups, and in that state can be used as inputs. As inputs, port 3 pins that are externally being pulled low will source current (I_{IL}), because of the pullups. Port 3 also serves the functions of various special features of the MCS-51 family, as listed below:

Pin symbol   Description - Continued.

Port pin	Alternate function
P3.0	RXD (serial input port)
P3.1	TXD (serial output port)
P3.2	$\overline{INT0}$ (external interrupt 0)
P3.3	$\overline{INT1}$ (external interrupt 1)
P3.4	T0 (timer 0 external input)
P3.5	T1 (timer 1 external input)
P3.6	$\overline{WR}$ (external data memory write strobe)
P3.7	$\overline{RD}$ (external data memory read strobe)

RST   Reset input. A high on this pin for two machine cycles while the oscillator is running resets the device. An internal diffused resistor to V_{SS} permits power-on reset using only an external capacitor to V_{CC}.

ALE   Address latch enable output pulse for latching the low byte of the address during accesses to external memory.

In normal operation, ALE is emitted at a constant rate of 1/6 the oscillator frequency, and may be used for external timing or clocking purposes. Note, however, that one ALE pulse is skipped during each access to external data memory.

$\overline{PSEN}$ Program store enable is the read strobe to external program memory. When the 02, 04, 06, and 08 devices are executing code from external program memory, PSEN is activated twice each machine cycle, except that two PSEN activations are skipped during each access to external data memory. PSEN is not activated during fetches from internal program memory.

$\overline{EA}$ External access enable. $\overline{EA}$ must be externally held low in order to enable the device to fetch code from external program memory locations 0000H to 0FFFH. If EA is held high the device executes from internal program memory unless the program counter contains an address greater than 0FFFH.

XTAL1   Output from the inverting oscillator amplifier and input to the internal block generator circuits.

XTAL2   Output from the inverting oscillator amplifier.

6.6 Sources of supply.

6.6.1 Sources of supply for device classes N, Q, and V. Sources of supply for device classes N, Q, and V are listed in QML-38535. The vendors listed in QML-38535 have submitted a certificate of compliance (see 3.6 herein) to DSCC-VA and have agreed to this drawing.

6.6.2 Approved sources of supply for device class M. Approved sources of supply for class M are listed in MIL-HDBK-103. The vendors listed in MIL-HDBK-103 have agreed to this drawing and a certificate of compliance (see 3.6 herein) has been submitted to and accepted by DSCC-VA.

APPENDIX

PIN SUPERSESSION INFORMATION

10. SCOPE

10.1 Scope This appendix contains the PIN supersession information to support the one part-one part number system. For new system designs, after the date of this document the NEW PIN shall be used in lieu of the OLD PIN. This is a mandatory part of the document. The information contained herein is intended for compliance. Th PIN supersession data shall be as follows:

20. APPLICABLE DOCUMENTS

This section is not applicable to this appendix.

30. SUPERSESSION DATA

NEW PIN	OLD PIN
5962-8506401MQX	8506401QX
5962-8506401MXX	8506401XX
5962-8506401MYX	8506401YX
5962-8506402MQX	8506402QX
5962-8506402MXX	8506402XX
5962-8506402MYX	8506402YX
5962-8506403MQX	8506403QX
5962-8506403MXX	8506403XX
5962-8506403MYX	8506403YX
5962-8506404MQX	8506404QX
5962-8506404MXX	8506404XX
5962-8506404MYX	8506404YX

STANDARD MICROCIRCUIT DRAWING SOURCE APPROVAL BULLETIN

DATE: 96-08-23

Approved sources of supply for SMD 85064 are listed below for immediate acquisition only and shall be added to MIL-HDBK-103 during the next revision. MIL-HDBK-103 will be revised to include the addition or deletion of sources. The vendors listed below have agreed to this drawing and a certificate of compliance has been submitted to and accepted by DSCC-VA. This bulletin is superseded by the next dated revision of MIL-HDBK-103.

Standard microcircuit drawing PIN 1/	Vendor CAGE number	Vendor similar PIN 2/
5962-8506401MQA	18324 34649	80C31BH/BQA MD80C31BH
5962-8506401MXA	18324 34649	80C31BH/BUA MR80C31BH
5962-8506401MYA	18324	80C31BH/BYA
5962-8506401NUA	18324	80C31BH/CN40A
5962-8506401NVA	18324	80C31BH/CA44A
5962-8506402MQA	18324 34649	80C51BH/BQA MD80C51BH
5962-8506402MXA	18324 34649	80C51BH/BUA MR80C51BH
5962-8506402MYA	18324	80C51BH/BYA
5962-8506402NUA	18324	80C51BH/CN40A
5962-85064O2NVA	18324	80C51BH/CA44A
5962-8506403MQA	18324 34649	80C31BH-16/BQA MD80C31BH-16
5962-8506403MXA	18324 34649	80C31BH-16/BUA MR80C31BH-16
5962-8506403MYA	18324	80C51BH-16/BYA
5962-8506403NUA	18324	80C31BH-16/CN40A
5962-8506403NVA	18324	80C31BH-16/CN44A
5962-8506404MQA	18324 34649	80C51BH-16/BQA MD80C31BH-16
5962-8506404MXA	18324 34649	80C51BH-16/BUA MR80C31BH-16

See footnotes at end of table.

Standard microcircuit drawing PIN 1/	Vendor CAGE number	Vendor similar PIN 2/
5962-8506404MYA	18324	80C51BH-16/BYA
5962-8506404NUA	18324	80C51BH-16/CN40A
5962-8506404NVA	18324	80C51BH-16/CN44A
5962-8506405NUA	18324	80C31BH/IN40A
5962-8506405NVA	18324	80C31BH/IA44A
5962-8506406NUA	18324	80C51BH/IN40A
5962-8506406NVA	18324	80C51BH/IA44A
5962-8506407NUA	18324	80C31BH-16/IN40A
5962-8506407NVA	18324	80C31BH-16/IA44A
5962-8506408NUA	18324	80C51BH-16/IN40A
5962-8506408NVA	18324	80C51BH-16/IA44A

1/ The lead finish shown for each PIN representing a hermetic package is the most readily available from the manufacturer listed for that part. The device manufacturers listed herein are authorized to supply alternate lead finishes "A", "B", or "C" at their discretion. Contact the listed approved source of supply for further information.

2/ Caution. Do not use this number for item acquisition. Items acquired to this number may not satisfy the performance requirements of this drawing.

Vendor CAGE number	Vendor name and address
18324	Philip Semiconductor 811 East Arques Avenue Sunnyvale, CA 94088
34649	Intel Corporation 3065 Bowers Avenue Santa Clara, CA 95051 Point of contact: 5000 West Williams Field Road Chandler, AZ 85224

The information contained herein is disseminated for convenience only and the Government assumes no liability whatsoever for any inaccuracies in the information bulletin.