REVISIONS			
LTR	DESCRIPTION	DATE (YR-MO-DA)	APPROVED
A	Add (LCC) leadless chip carrier for device types 03 and 04. Make corrections to figures 1 and 2.	1987 JUNE 18	M.A. Frye
B	Add device type 05. Make changes to table I, table II, figure 2, figure 3, and editorial changes throughout drawing. Add ESDS paragraph.	1988 OCT 28	M.A. Frye

CURRENT CAGE CODE 67268

REV																								
SHEET																								
REV																								
SHEET																								
REV STATUS OF SHEETS	REV	B	B	B	B	B	B	B	B	A	B	B						B						
	SHEET	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17						

PMIC N/A

STANDARDIZED MILITARY DRAWING

THIS DRAWING IS AVAILABLE FOR USE BY ALL DEPARTMENTS AND AGENCIES OF THE DEPARTMENT OF DEFENSE

AMSC N/A

PREPARED BY: Rick Office

CHECKED BY: Ray Monnin

APPROVED BY: M.A. Frye

DRAWING APPROVAL DATE: 30 MAY 1986

REVISION LEVEL: B

DEFENSE ELECTRONICS SUPPLY CENTER
DAYTON, OHIO 45444

MICROCIRCUITS, DIGITAL, 64K X 8-BIT, UV EPROM, MONOLITHIC SILICON

SIZE	CAGE CODE	
A	14933	5962-85135

SHEET 1 OF 17

DESC FORM 193-1
SEP 87

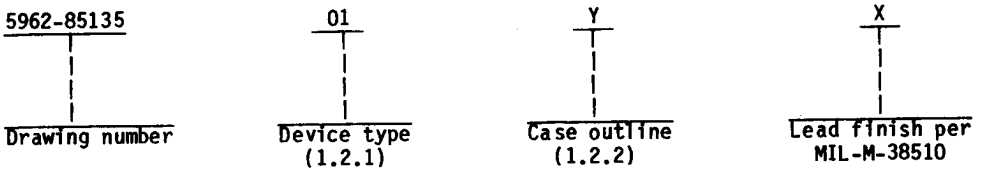
* U.S. GOVERNMENT PRINTING OFFICE: 1987 — 748-129/60912

5962-E855

1. SCOPE

1.1 Scope. This drawing describes device requirements for class B microcircuits in accordance with 1.2.1 of MIL-STD-883, "Provisions for the use of MIL-STD-883 in conjunction with compliant non-JAN devices".

1.2 Part number. The complete part number shall be as shown in the following example:



1.2.1 Device types. The device types shall identify the circuit function as follows:

Device type	Generic number	Circuit	Access time
01	27512-25	64K x 8-bit UVEPROM	250 ns
02	27512-35	64K x 8-bit UVEPROM	350 ns
03	27512-30	64K x 8-bit UVEPROM	300 ns
04	27512-45	64K x 8-bit UVEPROM	450 ns
05	27512-20	64K x 8-bit UVEPROM	200 ns

1.2.2 Case outlines. The case outlines shall be as designated in appendix C of MIL-M-38510, and as follows:

Outline letter	Case outline
Y	D-10 (28-pin, 1.490" x .610" x .232") dual-in-line package 1/
Z	C-12 (32-terminal, .560" x .458" x .120") rectangular chip carrier package 1/

1.3 Absolute maximum ratings.

Storage temperature range	-65°C to +150°C
All input or output voltages 2/	+6.5 V dc to -0.6 V dc
Voltage on pin 24 2/	+13.5 V dc to -0.6 V dc
$\overline{OE}$/Vpp supply voltage 2/	+14.0 V dc to -0.6 V dc
Maximum power dissipation (P_D)	825 mW at 5.5 V dc
Lead temperature (soldering, 10 seconds)	300°C
Thermal resistance, junction-to-case (θ_{JC}) Cases Y and Z	See MIL-M-38510, appendix C
Junction temperature (T_J)	200°C

1.4 Recommended operating conditions.

Case operating temperature range	-55°C to +125°C
Supply voltage (V_{CC})	+4.5 V dc to +5.5 V dc

1/ Lid shall be transparent to permit ultraviolet light erasure.
2/ Voltages shall be measured with respect to ground.

2. APPLICABLE DOCUMENTS

2.1 Government specification and standard. Unless otherwise specified, the following specification and standard, of the issue listed in that issue of the Department of Defense Index of Specifications and Standards specified in the solicitation, form a part of this drawing to the extent specified herein.

SPECIFICATION

MILITARY

MIL-M-38510 - Microcircuits, General Specification for.

STANDARD

MILITARY

MIL-STD-883 - Test Methods and Procedures for Microelectronics.

(Copies of the specification and standard required by manufacturers in connection with specific acquisition functions should be obtained from the contracting activity or as directed by the contracting activity.)

2.2 Order of precedence. In the event of a conflict between the text of this drawing and the references cited herein, the text of this drawing shall take precedence.

3. REQUIREMENTS

3.1 Item requirements. The individual item requirements shall be in accordance with 1.2.1 of MIL-STD-883, "Provisions for the use of MIL-STD-883 in conjunction with compliant non-JAN devices" and as specified herein.

3.2 Design, construction, and physical dimensions. The design, construction, and physical dimensions shall be as specified in MIL-M-38510 and herein.

3.2.1 Logic diagram. The logic diagram shall be as specified on figure 1.

3.2.2 Terminal connections. The terminal connections shall be as specified on figure 2.

3.2.3 Truth table. The truth table shall be as specified on figure 3.

3.2.3.1 Unprogrammed or erased devices. The truth table for unprogrammed devices shall be as specified on figure 3.

3.2.3.2 Programmed devices. The requirements for supplying programmed devices are not part of this drawing.

3.2.4 Case outline. The case outline shall be in accordance with 1.2.2 herein.

3.3 Electrical performance characteristics. Unless otherwise specified, the electrical performance characteristics are as specified in table I and apply over the full case operating temperature range.

3.4 Marking. Marking shall be in accordance with MIL-STD-883 (see 3.1 herein). The part shall be marked with the part number listed in 1.2 herein. In addition, the manufacturer's part number may also be marked as listed in 6.4 herein.

TABLE I. Electrical performance characteristics.

Test	Symbol	Conditions $-55°C \le T_C \le +125°C$ $4.5\ V \le V_{CC} \le 5.5\ V$	Group A subgroups	Device type	Limits		Unit
					Min	Max	
Input load current	I_{LI}	$V_{IN} = 5.5\ V$	1, 2, 3	All		10	µA
Output leakage current	I_{LO}	$V_{OUT} = 5.5\ V$	1, 2, 3	All		10	µA
V_{CC} standby current	I_{CC1}	$\overline{CE} = V_{IH}$	1, 2, 3	All		40	mA
V_{CC} current (active)	I_{CC2}	$\overline{CE} = \overline{OE}/V_{PP} = V_{IL}$	1, 2, 3	All		150	mA
Input low voltage	V_{IL}		1, 2, 3	All	-0.1 1/	+0.8	V
Input high voltage	V_{IH}		1, 2, 3	All	2.0	V_{CC} +1 1/	V
Output low voltage	V_{OL}	$I_{OL} = 2.1\ mA$	1, 2, 3	All		0.45	V
Output high voltage	V_{OH}	$I_{OH} = -400\ µA$	1, 2, 3	All	2.4		V
Address to output delay	t_{ACC}	$\overline{CE} = \overline{OE}/V_{PP} = V_{IL}$ 2/	9, 10, 11	01 02 03 04 05		250 350 300 450 200	ns
$\overline{CE}$ to output delay	t_{CE}	$\overline{OE}/V_{PP} = V_{IL}$ 2/	9, 10, 11	01 02 03 04 05		250 350 300 450 200	ns
$\overline{OE}$ to output delay	t_{OE}	$\overline{CE} = V_{IL}$ 2/	9, 10, 11	01 02, 03 04 05		100 120 150 75	ns
$\overline{OE}/V_{PP}$ high to output float	t_{DF} 1/	$\overline{CE} = V_{IL}$ 2/	9, 10, 11	01 02, 03 04 05		60 105 130 55	ns

See footnotes at end of table.

TABLE I. Electrical performance characteristics - Continued.

Test	Symbol	Conditions $-55°C \le T_C \le +125°C$, $4.5\ V \le V_{CC} \le 5.5\ V$	Group A subgroups	Device type	Limits Min	Limits Max	Unit
Output hold from addresses $\overline{CE}$ or $\overline{OE}$ whichever occurred first	t_{OH} 1/	$\overline{CE} = \overline{OE}/Vpp = V_{IL}$ 2/	9, 10, 11	All	0		ns
Input capacitance except $\overline{OE}/Vpp$	C_{IN1}	$V_{IN} = 0\ V$ See 4.3.1c	4	All		7	pF
Output capacitance	C_{OUT}	$V_{OUT} = 0\ V$ See 4.3.1c	4	All		12	pF
$\overline{OE}/Vpp$ input capacitance	C_{IN2}	$V_{OUT} = 0\ V$ See 4.3.1c	4	All		20	pF

1/ May not be tested, but shall be guaranteed to the limits specified in table I.
2/ See figures 4 and 5.

3.5 Processing EPROMS. All testing requirements and quality assurance provisions herein shall be satisfied by the manufacturer prior to delivery.

3.5.1 Erasure of EPROMS. When specified, devices shall be erased in accordance with the procedures and characteristics specified in 4.4.

3.5.2 Programmability of EPROMS. When specified, devices shall be programmed to the specified pattern using the procedures and characteristics specified in 4.5 and table III.

3.5.3 Verification of erasure of programmability of EPROMS. When specified, devices shall be verified as either programmed to the specified pattern or erased. As a minimum, verification shall consist of performing a functional test (subgroup 7) to verify that all bits are in the proper state. Any bit that does not verify to be in the proper state shall constitute a device failure, and shall be removed from the lot.

3.6 Certificate of compliance. A certificate of compliance shall be required from a manufacturer in order to be listed as an approved source of supply in 6.4. The certificate of compliance submitted to DESC-ECS prior to listing as an approved source of supply shall state that the manufacturer's product meets the requirements of MIL-STD-883 (see 3.1 herein) and the requirements herein.

3.7 Certificate of conformance. A certificate of conformance as required in MIL-STD-883 (see 3.1 herein) shall be provided with each lot of microcircuits delivered to this drawing.

3.8 Notification of change. Notification of change to DESC-ECS shall be required in accordance with MIL-STD-883 (see 3.1 herein).

3.9 Verification and review. DESC, DESC's agent, and the acquiring activity retain the option to review the manufacturer's facility and applicable required documentation. Offshore documentation shall be made available onshore at the option of the reviewer.

4. QUALITY ASSURANCE PROVISIONS

4.1 Sampling and inspection. Sampling and inspection procedures shall be in accordance with section 4 of MIL-M-38510 to the extent specified in MIL-STD-883 (see 3.1 herein).

4.2 Screening. Screening shall be in accordance with method 5004 of MIL-STD-883, and shall be conducted on all devices prior to quality conformance inspection. The following additional criteria shall apply:

a. Burn-in test (method 1015 of MIL-STD-883).

(1) Test condition A, B, C, or D using the circuit submitted with the certificate of compliance (see 3.5 herein).

(2) T_A = +125°C, minimum.

b. Interim and final electrical test parameters shall be as specified in table II herein, except interim electrical parameter tests prior to burn-in are optional at the discretion of the manufacturer.

c. A data retention stress test shall be included as part of the screening procedure and shall consist of the following steps:

Margin test method A.

(1) Program greater than 95 percent of the bit locations, including the slowest programming cell (see 3.5.2).

(2) Bake, unbiased, for 12 hours at 200°C.

(3) Perform a margin test using $V_m = V_{CC}$ = 6.0 V at 25°C using loose timing.

(4) Erase device, then program 45 percent to 50 percent of the bits to a worst case speed pattern.

(5) Perform dynamic burn-in (see 4.2a).

(6) Perform a margin test using $V_m = V_{CC}$ = 6.0 V at 25°C.

(7) Perform 100 percent electrical testing at +125°C, +25°C, and -55°C.

(8) Erase device (see 3.5.1), except devices submitted for groups A, B, C, and D.

(9) Verify erasure (see 3.5.3).

Margin test method B.

(1) Program greater than 95% of the bit locations, including the slowest programming cell (see 3.5.2). The remaining cells shall provide a worst case speed pattern.

(2) Bake, unbiased, for 72 hours at +140°C to screen for data retention lifetime.

(3) Perform a margin test using V_m = +5.9 at 25°C using loose timing (i.e., t_{ACC} = 1 µs).

(4) Perform dynamic burn-in (see 4.2a).

(5) Margin at V_m = +5.9 V.

(6) Perform electrical tests (see 4.2).

(7) Erase (see 3.5.1), except devices submitted for groups A, B, C, and D testing.

(8) Verify erasure (see 3.5.3).

4.3 Quality conformance inspection. Quality conformance inspection shall be in accordance with method 5005 of MIL-STD-883 including groups A, B, C, and D inspections. The following additional criteria shall apply.

4.3.1 Group A inspection.

a. Tests shall be as specified in table II herein.

b. Subgroups 5 and 6 in table I, method 5005 of MIL-STD-883 shall be omitted.

c. Subgroup 4 (C_{IN} and C_{OUT} measurement) shall be measured only for the initial test and after process design changes which may affect capacitance.

d. All devices selected for testing shall have the EPROM programmed with a checkerboard pattern or equivalent. After completion of all testing, the devices shall be erased and verified (except devices submitted for group C and D testing).

e. Subgroups 7 and 8 shall consist of verifying the EPROM pattern specified.

4.3.2 Groups C and D inspections.

a. End-point electrical parameters shall be as specified in table II herein.

b. Steady-state life test conditions, method 1005 of MIL-STD-883.

(1) Test condition A, B, C, or D using the circuit submitted with the certificate of compliance (see 3.6 herein).

(2) T_A = +125°C, minimum.

(3) Test duration: 1,000 hours, except as permitted by and method 1005 of MIL-STD-883.

4.4 Erasing procedures. The recommended erasure procedure is exposure to shortwave ultraviolet light which has a wavelength of 2537 Angstroms (Å). The integrated dose (i.e., UV intensity x exposure time) for erasure should be a minimum of fifteen (15) Ws/cm^2. The erasure time with this dosage is approximately 15 to 20 minutes using an ultraviolet lamp with a 1200 $\mu W/cm^2$ power rating. The device should be placed within one inch of the lamp tubes during erasure. The maximum integrated dose the device can be exposed to without damage is 7258 Ws/cm^2 (1 week at 12000 $\mu W/cm^2$). Exposure of the device to high intensity UV light for long periods may cause permanent damage.

4.5 Programming procedures for method A. The programming characteristics in table III and the following procedures shall be used for programming the device.

a. Connect the device in the electrical configuration for programming the waveforms of figure 6 and programming characteristics of table III shall apply.

b. Initially and after each erasure all bits are in the "1" state. Information is introduced by selectively programming "0" into the desired bit locations. A programmed "0" can be changed to a "1" by ultraviolet light erasure (see 4.4).

c. Programming occurs when the $\overline{OE}$/Vpp input is at 12.5 V and $\overline{CE}$ is at TTL low.

TABLE II. Electrical test requirements.

MIL-STD-883 test requirements	Subgroups (per method 5005, table I)
Interim electrical parameters (method 5004)	---
Final electrical test parameters (method 5004)	1*, 2, 3, 7*, 8, 9, 10, 11
Group A test requirements (method 5005)	1, 2, 3, 7, 8, 9, 10, 11**
Groups C and D end-point electrical parameters (method 5005)	2, 8 (125°C), 10

* PDA applies to subgroup 1 (see 4.2c).
** Subgroups 10 and 11, if not tested, shall be guaranteed to the specified limits in table I.

4.6 Electrostatic discharge sensitivity inspection. Electrostatic discharge sensitivity (ESDS) testing shall be performed in accordance with MIL-STD-883, method 3015, and MIL-M-38510. The option to categorize devices as ESD sensitive without performing the test is not allowed. Only those device types that pass ESDS testing at 1,000 volts or greater shall be considered as conforming to the requirements of this drawing. ESDS testing shall be measured only for initial testing and after process or design changes which may effect ESDS classification.

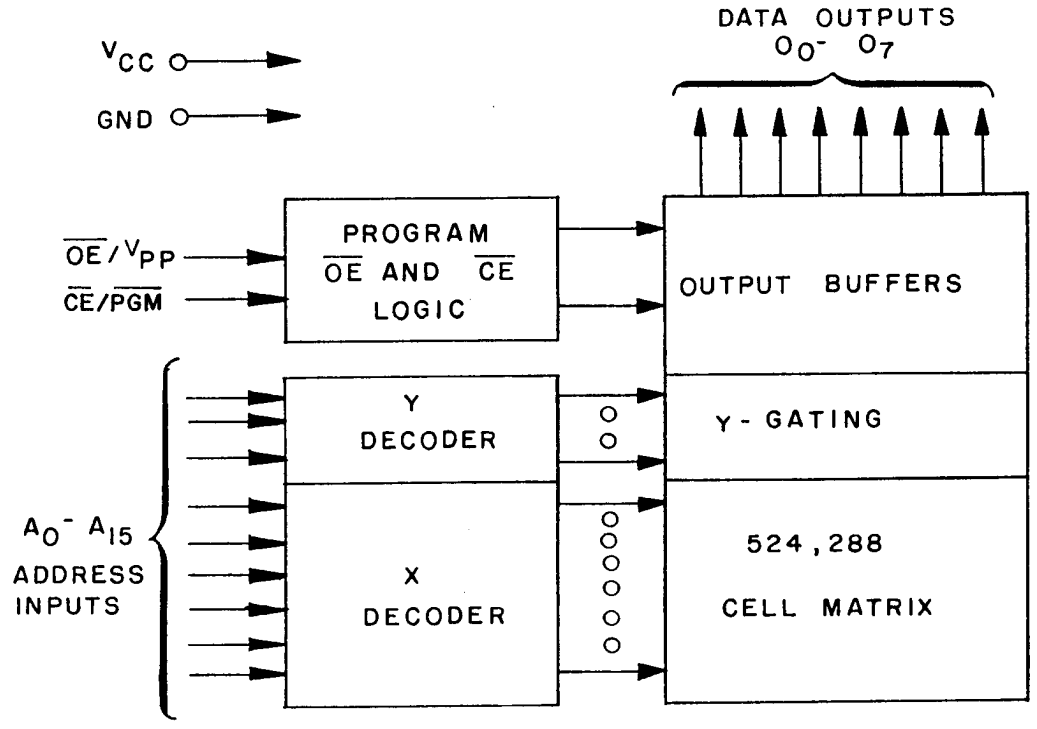
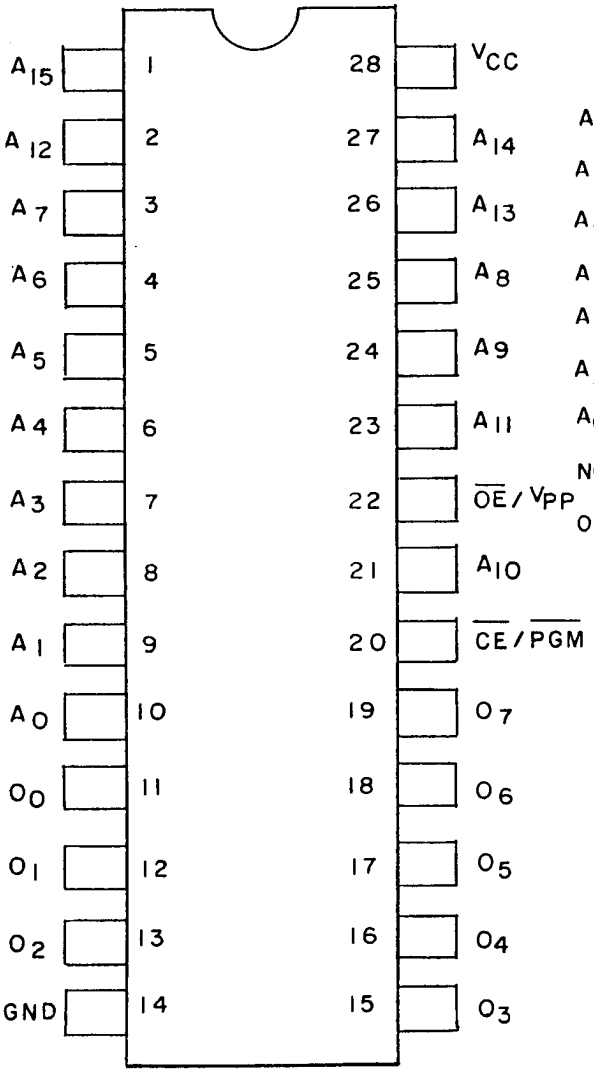
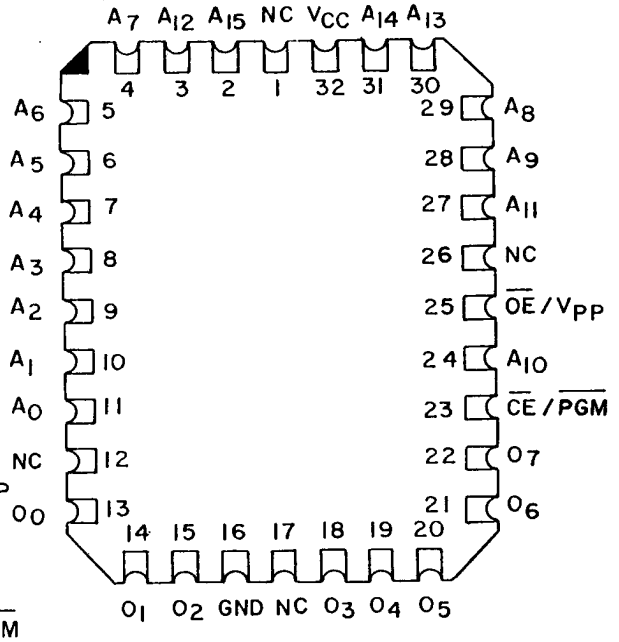


FIGURE 1. Block diagram.

CASE Y



CASE Z



Pin Names

A_0-A_{15}	Addresses
$\overline{CE}/\overline{PGM}$	Chip Enable
$\overline{OE}/V_{pp}$	Output Enable/V_{pp}
O_0-O_7	Outputs

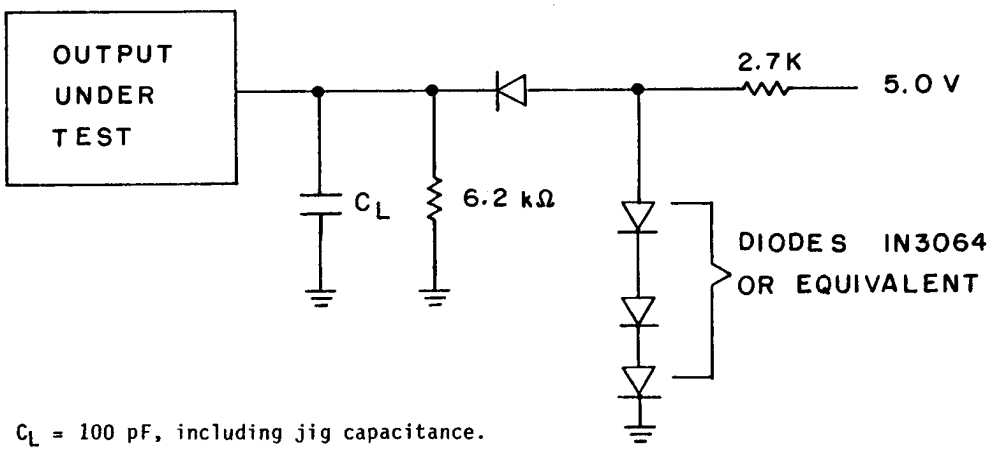
FIGURE 2. Terminal connections.

Mode \ Pins	$\overline{CE}$	$\overline{OE}/V_{PP}$	A_9	V_{CC}	Outputs
Read	V_{IL}	V_{IL}	X	V_{CC}	D_{OUT}
Output Disable	V_{IL}	V_{IH}	X	V_{CC}	High Z
Standby	V_{IH}	X	X	V_{CC}	High Z
Intelligent Programming	V_{IL}	V_{PP}	X	V_{CC}	D_{IN}
Program Inhibit	V_{IH}	V_{PP}	X	V_{CC}	High Z
Intelligent Identifier	V_{IL}	V_{IL}	V_H	V_{CC}	Code

NOTES:
1. X can be V_{IH} or V_{IL}
2. V_H = 12.0 V ±0.5 V

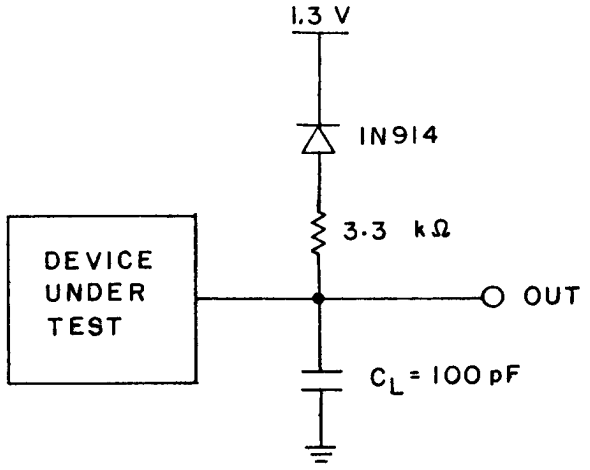
FIGURE 3. Truth table.

Circuit A



C_L = 100 pF, including jig capacitance.

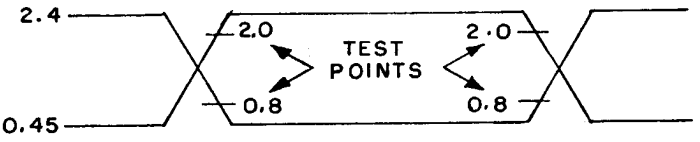
Circuit B



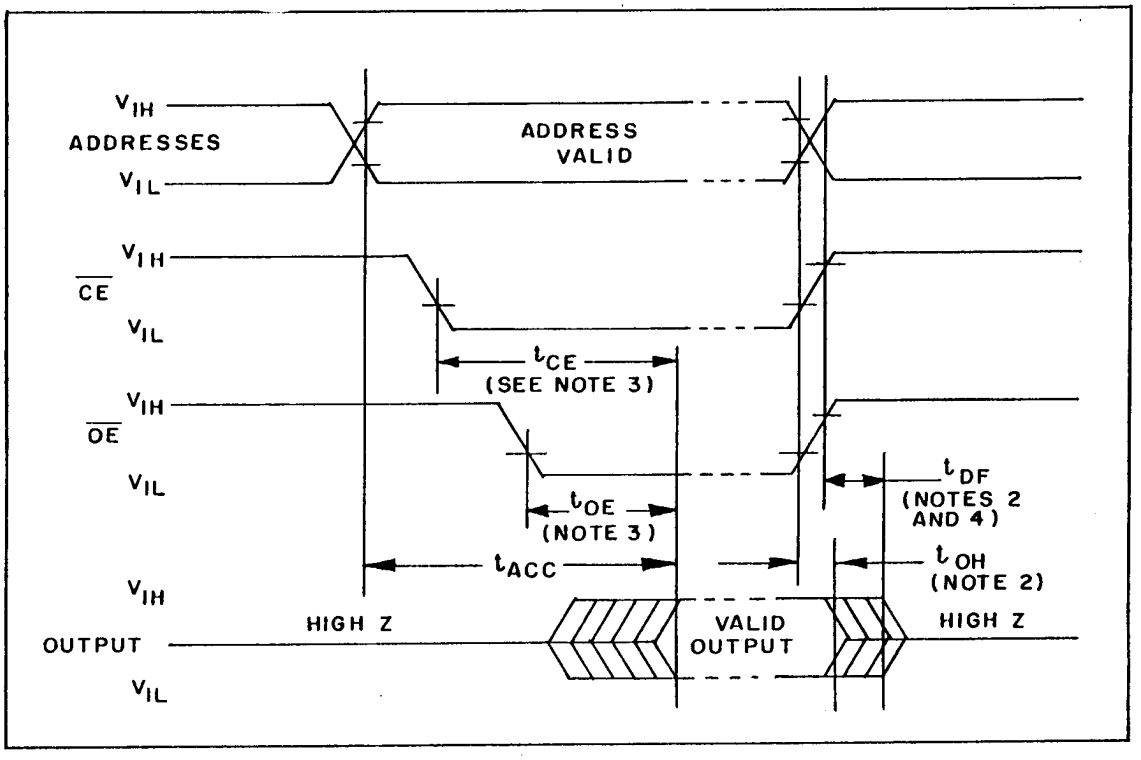
C_L = 100 pF, INCLUDING JIG CAPACITANCE

FIGURE 4. Switching test circuits.

AC TESTING INPUT/OUTPUT WAVEFORM

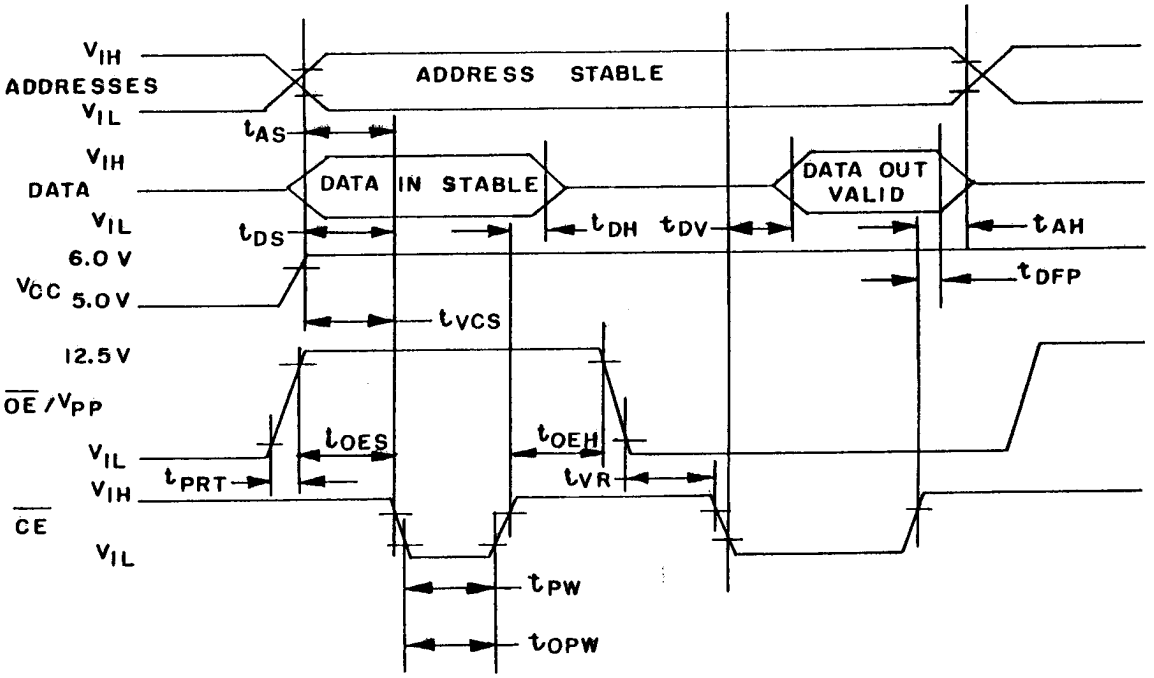


AC TESTING INPUTS ARE DRIVEN AT 2.4 V FOR A LOGIC "1" AND .045 V FOR A LOGIC "0". TIMING MEASUREMENTS ARE MADE AT 2.0 V FOR A LOGIC "1" AND 0.8 V FOR A LOGIC "0".



NOTES:
1. Typical values are for T_A = 25°C and nominal supply voltages.
2. This parameter is only sampled and is not 100% tested.
3. $\overline{OE}/V_{pp}$ may be delayed up to $t_{CE}-t_{OE}$ after the falling edge of $\overline{CE}$ without impact on t_{CE}.
4. t_{DF} is specified from $\overline{OE}/V_{pp}$ or $\overline{CE}$, whichever occurs first.

FIGURE 5. AC waveforms.



NOTES:
1. The input timing reference level is 0.8 V for a V_{IL} and 2.0 V for a V_{IH}.
2. t_{OE} and t_{DFP} are characteristics of the device but must be accommodated by the programmer.

FIGURE 6. Programming waveforms.

TABLE III. Programming characteristics for method A.

Parameter	Symbol	Conditions 1/ T_A = 25°C ±5°C, V_{CC} = 6.0 V ±0.25 V, $\overline{OE}/V_{PP}$ = 12.5 V ±0.5 V	Group A subgroups	Limits		Unit
				Min	Max	
Input current (all inputs)	I_{LI}	$V_{IN} = V_{IL}$ or V_{IH}			10	µA
Input low level (all inputs)	V_{IL}			-0.1	0.8	V
Input high level	V_{IH}			2.0	V_{CC} +1	V
Output low voltage during verify	V_{OL}	I_{OL} = 2.1 mA			0.45	V
Output high voltage during verify	V_{OH}	I_{OH} = -400 µA		2.4		V
V_{CC} supply current	I_{CC2}				150	mA
Vpp supply current (program)	I_{PP2}	$\overline{CE} = V_{IL}$			50	mA
A9 intelligent identifier voltage	V_{ID}			11.5	12.5	V
Address setup time	t_{AS}			2		µs
$\overline{OE}$/Vpp setup time	t_{OES}			2		µs
$\overline{OE}$/Vpp hold time	t_{OEH}			2		µs
Data setup time	t_{DS}			2		µs
Address hold time	t_{AH}			0		µs
Data hold time	t_{DH}			2		µs
Output enable to output float delay	t_{DFP} 2/			0	130	ns

See footnotes at end of table.

TABLE III. Programming characteristics for method A - Continued.

Parameter	Symbol	Conditions 1/ T_A = 25°C ±5°C, V_{CC} = 6.0 V ±0.25 V, $\overline{OE}/V_{PP}$ = 12.5 V ±0.5 V	Group A subgroups	Limits		Unit
				Min	Max	
V_{CC} setup time	t_{VCS}			2		µs
$\overline{CE}$ initial program pulse width	t_{PW} 3/			0.95	1.05	ms
$\overline{CE}$ overprogram pulse width	t_{OPW} 4/			2.85	78.75	ms
Data valid from $\overline{CE}$	t_{DV}				1	µs
$\overline{OE}/V_{PP}$ recovery time	t_{VR}			2		µs
$\overline{OE}/V_{PP}$ pulse rise time during programming	t_{PRT}			50		ns

1/ V_{CC} must be applied simultaneously or before $\overline{OE}/V_{PP}$ and removed simultaneously or after $\overline{OE}/V_{PP}$.
2/ This parameter is only sampled and is not 100 percent tested. Output float is defined as the point where data is no longer driven, see timing diagram.
3/ Initial program pulse width tolerance is 1 ms ±5 percent.
4/ The length of the overprogram pulse may vary from 2.85 ms to 78.75 ms as a function of the iteration counter value X.

5. PACKAGING

5.1 Packaging requirements. The requirements for packaging shall be in accordance with MIL-M-38510.

6. NOTES

6.1 Intended use. Microcircuits conforming to this drawing are intended for use when military specifications do not exist and qualified military devices that will perform the required function are not available for OEM application. When a military specification exists and the product covered by this drawing has been qualified for listing on QPL-38510, the device specified herein will be inactivated and will not be used for new design. The QPL-38510 product shall be the preferred item for all applications.

6.2 Replaceability. Replaceability is determined as follows:

a. Microcircuits covered by this drawing will replace the same generic device covered by a contractor-prepared specification or drawing.

b. When a QPL source is established, the part numbered device specified in this drawing will be replaced by the microcircuit identified as part number M38510/2700XB.

6.3 Comments. Comments on this drawing should be directed to DESC-ECS, Dayton, OH 45444, or telephone 513-296-5375.

6.4 Approved sources of supply. Approved sources of supply are listed herein. Additional sources will be added as they become available. The vendors listed herein have agreed to this drawing and a certificate of compliance (see 3.6 herein) has been submitted to DESC-ECS.

Military drawing part number	Vendor CAGE number	Vendor similar part number 1/	Replacement military specification part number	Margin test method	Switching test circuit
5962-8513501YX	34649 34335	MD27512-25/B AM27512-25/BXA	M38510/27002BYX	B A	B A
5962-8513502YX	34649	MD27512-35/B	M38510/27001BYX	B	B
5962-8513503YX 5962-8513503ZX	34335 34335	AM27512-30/BXA AM27512-30/BUA		A A	A A
5962-8513504YX 5962-8513504ZX	34335 34335	AM27512-45/BXA AM27512-45/BUA		A A	A A
5962-8513505YX	34649	MD27512-20/B	M38510/27003BYX	B	B

1/ Caution: Do not use this number for item acquisition. Items acquired to this number may not satisfy the performance requirements of this drawing.

Vendor CAGE number	Vendor name and address
34335	Advanced Micro Devices 901 Thompson Place P. O. Box 3453 Sunnyvale, CA 94088
34649	Intel Corporation 3065 Bowers Avenue Santa Clara, CA 95051