REVISIONS			
LTR	DESCRIPTION	DATE (YR-MO-DA)	APPROVED
E	Removed vendor CAGE numbers 18324, 27014, and 34335. Added devices 21 and 22. Updated document format, editorial changes throughout.	96-06-13	M. A. Frye

REV																			
SHEET																			
REV	E	E	E	E															
SHEET	15	16	17	18															

REV STATUS OF SHEETS	REV	E	E	E	E	E	E	E	E	E	E	E	E	E
	SHEET	1	2	3	4	5	6	7	8	9	10	11	12	13	14

PMIC N/A

STANDARD MICROCIRCUIT DRAWING

THIS DRAWING IS AVAILABLE FOR USE BY ALL DEPARTMENTS AND AGENCIES OF THE DEPARTMENT OF DEFENSE

AMSC N/A

PREPARED BY
JAMES JAMISON

CHECKED BY
CHARLES REUSING

APPROVED BY
MICHAEL A. FRYE

DRAWING APPROVAL DATE
86-06-20

REVISION LEVEL
E

DEFENSE ELECTRONICS SUPPLY CENTER
DAYTON, OHIO 45444

MICROCIRCUIT, MEMORY, BIPOLAR, PROGRAMMABLE LOGIC ARRAY, MONOLITHIC SILICON

SIZE	CAGE CODE	
A	67268	5962-85155

SHEET 1 OF 18

DESC FORM 193
JUL 94

5962-E396-96

DISTRIBUTION STATEMENT A. Approved for public release; distribution is unlimited.

1. SCOPE

1.1 Scope. This drawing describes device requirements for MIL-STD-883 compliant, non-JAN class level B microcircuits in accordance with MIL-PRF-38535, appendix A.

1.2 Part or Identifying Number (PIN). The complete PIN shall be as shown in the following example:

5962-85155	01	R	X
Drawing number	Device type (1.2.1)	Case outline (1.2.2)	Lead finish per (1.2.3)

1.2.1 Device type(s). The device type(s) shall identify the circuit function as follows:

Device type	Generic number	Circuit function
01	PAL16L8-20	16-input 8-output AND-OR invert gate array
02	PAL16R8-20	16-input 8-output registered AND-OR gate array
03	PAL16R6-20	16-input 6-output registered AND-OR gate array
04	PAL16R4-20	16-input 4-output registered AND-OR gate array
05	PAL16L8-30	16-input 8-output AND-OR invert gate array
06	PAL16R8-30	16-input 8-output registered AND-OR gate array
07	PAL16R6-30	16-input 6-output registered AND-OR gate array
08	PAL16R4-30	16-input 4-output registered AND-OR gate array
09	PAL16L8-15	16-input 8-output AND-OR invert gate array
10	PAL16R8-15	16-input 8-output registered AND-OR gate array
11	PAL16R6-15	16-input 6-output registered AND-OR gate array
12	PAL16R4-15	16-input 4-output registered AND-OR gate array
13	PAL16L8A-12	16-input 8-output AND-OR invert gate array
14	PAL16R8A-12	16-input 8-output registered AND-OR gate array
15	PAL16R6-12	16-input 6-output registered AND-OR gate array
16	PAL16R4-12	16-input 4-output registered AND-OR gate array
17	PAL16L8-10	16-input 8-output AND-OR invert gate array
18	PAL16R8-10	16-input 8-output registered AND-OR gate array
19	PAL16R6-10	16-input 6-output registered AND-OR gate array
20	PAL16R4-10	16-input 4-output registered AND-OD gate array
21	PAL16R8-7	16-input 8-output registered AND-OR gate array
22	PAL16R4-7	16-input 4-output registered AND-OD gate array

1.2.2 Case outline(s). The case outline(s) are as designated in MIL-STD-1835 and as follows:

Outline letter	Descriptive designator	Terminals	Package style
R	GDIP1-T20	20-lead	dual-in-line package
	CDIP1-T20	20-lead	dual-in-line package
S	CDFP5-F20 1/	20-lead	flat package
2	CQCC1-N20	20-terminal	square chip carrier package

1/ Inactive for new design. Acceptable only for use in equipment designed or redesigned on or before 29 November 1986.

1.2.3 Lead finish. The lead finish is as specified in MIL-PRF-38535, appendix A.

1.3 Absolute maximum ratings.

Supply voltage range 2/	-0.5 V dc to 7.0 V dc
Input voltage range 2/ 3/	-0.5 V dc to 5.5 V dc
Storage temperature range	-65°C to +150°C
Lead temperature (soldering, 10 seconds)	+260°C
Thermal resistance, junction-to-case (Θ_{JC}) 4/	See MIL-STD-1835
Applied voltage to a disabled output range 2/ 3/	-0.5 V dc to 5.5 V dc
Maximum power dissipation (P_D) 5/:	
Device types 01, 02, 03, and 04	1.1 W
Device types 05, 06, 07, and 08	0.6 W
Device types 09, 10, 11, 12, 13, 14, and 15 thru 20-	1.2 W
Maximum junction temperature (T_J)	+175°C

1.4 Recommended operating conditions.

Supply voltage range (V_{CC})	4.5 V dc minimum to 5.5 V dc maximum
Minimum high level input voltage (V_{IH})	2.0 V dc
Maximum low level input voltage (V_{IL})	0.8 V dc
Maximum high level output current (I_{OH})	-2.0 mA dc
Maximum low level output current (I_{OL})	12.0 mA dc
Case operating temperature range	-55°C to +125°C

2. APPLICABLE DOCUMENTS

2.1 Government specification, standards, and handbooks. The following specification, standards, and handbooks form a part of this drawing to the extent specified herein. Unless otherwise specified, the issues of these documents are those listed in the issue of the Department of Defense Index of Specifications and Standards (DoDISS) and supplement thereto, cited in the solicitation.

SPECIFICATION

MILITARY

MIL-PRF-38535 - Integrated Circuits, Manufacturing, General Specification for.

STANDARDS

MILITARY

MIL-STD-883 - Test Methods and Procedures for Microelectronics.
MIL-STD-973 - Configuration Management.
MIL-STD-1835 - Microcircuit Case Outlines.

2/ These ratings apply except for programming pins during a programming cycle.
3/ To ensure high speed operation, input logic levels must be maintained within these conditions.
4/ Heat sinking is recommended to reduce the junction temperature.
5/ Must withstand the added P_D due to short-circuit test; e.g., I_{OS}.

HANDBOOKS

MILITARY

MIL-HDBK-103 - List of Standard Microcircuit Drawings (SMD's).
MIL-HDBK-780 - Standard Microcircuit Drawings.

(Unless otherwise indicated, copies of the specification, standards, and handbooks are available from the Standardization Document Order Desk, 700 Robbins Avenue, Building 4D, Philadelphia, PA 19111-5094.)

2.2 Order of precedence. In the event of a conflict between the text of this drawing and the references cited herein, the text of this drawing takes precedence. Nothing in this document, however, supersedes applicable laws and regulations unless a specific exemption has been obtained.

3. REQUIREMENTS

3.1 Item requirements. The individual item requirements shall be in accordance with MIL-PRF-38535, appendix A for non-JAN class level B devices and as specified herein. Product built to this drawing that is produced by a Qualified Manufacturer Listing (QML) certified and qualified manufacturer or a manufacturer who has been granted transitional certification to MIL-PRF-38535 may be processed as QML product in accordance with the manufacturers approved program plan and qualifying activity approval in accordance with MIL-PRF-38535. This QML flow as documented in the Quality Management (QM) plan may make modifications to the requirements herein. These modifications shall not affect form, fit, or function of the device. These modifications shall not affect the PIN as described herein. A "Q" or "QML" certification mark in accordance with MIL-PRF-38535 is required to identify when the QML flow option is used.

3.2 Design, construction, and physical dimensions. The design, construction, and physical dimensions shall be as specified in MIL-PRF-38535, appendix A and herein.

3.2.1 Case outlines. The case outlines shall be in accordance with 1.2.2 herein.

3.2.2 Terminal connections. The terminal connections shall be as specified on figure 1.

3.2.3 Truth table.

3.2.3.1 Unprogrammed devices. The truth table for unprogrammed devices for contracts involving no altered item drawing shall be as specified on figure 2. When required in groups A, B, or C (see 4.3.1c), the devices shall be programmed by the manufacturer prior to test. A minimum of 50 percent of the total number of fuses shall be programmed) or to any altered item drawing pattern which programs at least 25 percent of the total number of fuses programmed.

3.2.3.2 Programmed devices. The truth table for programmed devices shall be as specified by an attached altered item drawing.

3.2.4 Switching waveforms and test circuit. The switching waveforms and test circuit shall be as specified on figure 4.

3.3 Electrical performance characteristics. Unless otherwise specified herein, the electrical performance characteristics are as specified in table I and shall apply over the full (case or ambient) operating temperature range.

3.4 Electrical test requirements. The electrical test requirements shall be the subgroups specified in table II. The electrical tests for each subgroup are described in table I.

3.5 Marking. Marking shall be in accordance with MIL-PRF-38535, appendix A. The part shall be marked with the PIN listed in 1.2 herein. In addition, the manufacturer's PIN may also be marked as listed in MIL-HDBK-103 (see 6.6 herein). For packages where marking of the entire SMD PIN number is not feasible due to space limitations, the manufacturer has the option of not marking the "5962-" on the device.

3.6 Processing options. Since the device is capable of being programmed by either the manufacturer or the user to result in a wide variety of configurations, two processing options are provided for selection in the contract, using an altered item drawing.

3.6.1 Unprogrammed device delivered to the user. All testing shall be verified through group A testing as defined in 3.2.3.1 and table II. It is recommended that users perform subgroups 7 and 9 after programming to verify the specific program configuration.

3.6.2 Manufacturer-programmed device delivered to the user. All testing requirements and quality assurance provisions herein, including the requirements of the altered item drawing shall be satisfied by the manufacturer prior to delivery.

3.7 Certificate of compliance. A certificate of compliance shall be required from a manufacturer in order to be listed as an approved source of supply in MIL-HDBK-103 (see 6.6 herein). The certificate of compliance submitted to DESC-EC prior to listing as an approved source of supply shall affirm that the manufacturer's product meets the requirements of MIL-PRF-38535, appendix A and the requirements herein.

3.8 Certificate of conformance. A certificate of conformance as required in MIL-PRF-38535, appendix A shall be provided with each lot of microcircuits delivered to this drawing.

3.9 Notification of change. Notification of change to DESC-EC shall be required in accordance with MIL-PRF-38535, appendix A.

3.10 Verification and review. DESC, DESC's agent, and the acquiring activity retain the option to review the manufacturer's facility and applicable required documentation. Offshore documentation shall be made available onshore at the option of the reviewer.

3.8 Certificate of conformance. A certificate of conformance as required in MIL-STD-883 (see 3.1 herein) shall be provided with each lot of microcircuits delivered to this drawing.

3.9 Notification of change. Notification of change to DESC-EC shall be required in accordance with MIL-STD-883 (see 3.1 herein).

3.10 Verification and review. DESC, DESC's agent, and the acquiring activity retain the option to review the manufacturer's facility and applicable required documentation. Offshore documentation shall be made available onshore at the option of the reviewer.

4. QUALITY ASSURANCE PROVISIONS

4.1 Sampling and inspection. Sampling and inspection procedures shall be in accordance with MIL-PRF-38535, appendix A.

4.2 Screening. Screening shall be in accordance with method 5004 of MIL-STD-883, and shall be conducted on all devices prior to quality conformance inspection. The following additional criteria shall apply:

a. Burn-in test, method 1015 of MIL-STD-883.

(1) Test condition A, B, C, or D using the circuit submitted with the certificate of compliance (see 3.7 herein).

(2) T_A = +125°C, minimum.

b. Interim and final electrical test parameters shall be as specified in table II herein, except interim electrical parameter tests prior to burn-in are optional at the discretion of the manufacturer.

TABLE I. Electrical performance characteristics.

Test	Symbol	Conditions $4.5\ V \le V_{CC} \le 5.5\ V$ $-55^{o}C \le T_C \le +125^{o}C$ unless otherwise specified		Group A Subgroups	Device type	Limits		Unit
						Min	Max	
Input clamp voltage	V_{IC}	V_{CC} = 4.5 V, I_I = -18 mA		1, 2, 3	All		-1.5	V
High Level output voltage	V_{OH}	V_{CC} = 4.5 V, V_{IL} 4.5 V, V_{IH} 2.0 V, I_{OH} = -2 mA		1, 2, 3	01,02, 04-20	2.4		V
					03,21, 22	2.3		
Low level output voltage	V_{OL}	V_{CC} = 4.5 V, V_{IL} 4.5 V, V_{IH} 2.0 V, I_{OL} = 12 mA		1, 2, 3	All		0.5	V
High level input voltage	V_{IH}			1, 2, 3	All	2		V
Low level input voltage	V_{IL}			1, 2, 3	All		0.8	V
High level input current	I_{IH}	V_{CC} = 5.5 V, V_I = 2.4 V	Pins CLK and $\overline{OE}$	1, 2, 3	02,03,04, 06,07,08, 10,11,12, 14,15,16, 18,19,20		50	μA
			All others except I/O		All		25	
			All I/O ports		01,03, 04,05, 07,08, 09,11, 12,13, 15,16, 17,19, 20,21, 22		100	
Low level input current	I_{IL}	V_{CC} = 5.5 V, V_{IL} = 0.4 V		1, 2, 3	All		-0.25	mA
Input current	I_I	V_{CC} = 5.5 V, V_I = 5.5 V		1, 2, 3	All		1	mA
Output current short circuit 1/	I_{OS}	V_{CC} = 5.5 V, V_O = 0.5 V		1, 2, 3	01-16	-30	-250	mA
					17-22	-30	-130	

See footnotes at end table.

TABLE I. Electrical performance characteristics.

Test	Symbol	Conditions $4.5\ V \le V_{CC} \le 5.5\ V$, $-55^{o}C \le T_C \le +125^{o}C$ unless otherwise specified		Group A Subgroups	Device type	Limits		Unit
						Min	Max	
Off-state output current	I_{OZL}	V_{CC} = 5.5 V, V_O = 0.4 V	Outputs	1, 2, 3	All		-100	µA
			I/O ports				-250	
Off-state output current	I_{OZH}	V_{CC} = 5.5 V, V_O = 2.4 V		1, 2, 3	All		100	µA
Supply current	I_{CC}	V_{CC} = 5.5 V, V_I = 0 V Outputs open		1, 2, 3	01-04		190	mA
					05-08		105	
					09-20		220	
					21,22		210	
Propagation delay data input to output	t_{PLH1}	See figure 3		9, 10, 11	01,03,04		20	ns
					05,07,08		30	
					09,11,12		15	
					13,15,16		12	
					17,19,20		10	
					21,22		7	
Propagation delay data input to output	t_{PHL1}				01,03,04		20	
					05,07,08		30	
					09,11,12		15	
					13,15,16		12	
					17,19,20		10	
					21,22		7	
Propagation delay clock/up to output	t_{PHL2}				02 - 04		15	
					06 - 08		20	
					10 - 12, 14,16		12	
					18, 20		10	
					21, 22		7	

See footnotes at end of table.

TABLE I. Electrical performance characteristics.

Test	Symbol	Conditions $4.5\ V \le V_{CC} \le 5.5\ V$, $-55^{o}C \le T_C \le +125^{o}C$ unless otherwise specified	Group A Subgroups	Device type	Limits		Unit
					Min	Max	
Propagation delay clock/up to output	t_{PLH2}	See figure 3	9, 10, 11	02 - 04		15	ns
				06 - 08		20	
				10 - 12, 14,16		12	
				18 - 20		10	
				21, 22		7	
Propagation delay output high impedance to output high	t_{PZH1}			01,03,04		25	
				05,07,08		30	
				09,11,12		17	
				13,15,16		14	
				17,19,20		12	
				21,22		9	
Propagation delay output high impedance to output low	t_{PZL1}			01,03,04		25	
				05,07,08		30	
				09,11,12		17	
				13,15,16		14	
				17,19,20		12	
				21,22		9	
Propagation delay output high to output high impedance 2/	t_{PHZ1}			01,03,04		20	
				05,07,08		30	
				09,11,12		15	
				13,15,16		12	
				17,19, 20,21, 22		10	

See footnotes at end of table.

TABLE I. Electrical performance characteristics.

Test	Symbol	Conditions $4.5\ V \le V_{CC} \le 5.5\ V$ $-55^{o}C \le T_C \le +125^{o}C$ unless otherwise specified	Group A Subgroups	Device type	Limits		Unit
					Min	Max	
Propagation delay output low to output high impedance 2/	t_{PLZ1}	See figure 4	9, 10, 11	01,03,04		20	ns
				05,07,08		30	
				09,11,12		15	
				13,15,16		12	
				17,19, 20,21,22		10	
Propagation delay high impedance to output high ($\overline{OE}$ to output enable) 3/	t_{PZH2}			01,03,04		20	
				05,07,08		30	
				09,11,12		15	
				13,15,16		12	
				17,19,20		10	
				21,22		8	
Propagation delay hgih impedance to output low ($\overline{OE}$ to output enable 3/	t_{PZL2}			02,03,04		20	
				06,07,08		25	
				10,11,12, 14 - 16		12	
				18 - 20		10	
				21,22		8	
Propagation delay output high to high impedance ($\overline{OE}$ to output disable 2/ 3/	t_{PHZ2}			02,03,04		20	
				06,07,08		25	
				10,11,12, 14 - 16		12	
				18 - 20, 21,22		10	

See footnotes at end of table.

TABLE I. Electrical performance characteristics.

Test	Symbol	Conditions $4.5\ V \le V_{CC} \le 5.5\ V$ $-55^{o}C \le T_C \le +125^{o}C$ unless otherwise specified	Group A Subgroups	Device type	Limits		Unit
					Min	Max	
Hold time	t_H	See figure 4	9, 10, 11	02,03,04, 06,07,08, 10,11,12, 14,15,16, 18,20,21, 22	0		ns
Setup time	t_{SU}			02,03,04	20		
				06,07,08	30		
				10,11,12	15		
				14 - 16, 18 - 20	11		
				21,22	7		
Maximum clock frequency data path register	f_{MAX}			02,03,04	41.6		MHz
				06,07,08	25.0		
				10,11,12	50.0		
				14 - 16	56.0		
				18 - 20	62.5		
				21,22	100		

1/ The output conditions may be chosen to produce a current that closely approximates one-half of the true short-circuit output current, I_{OS}.

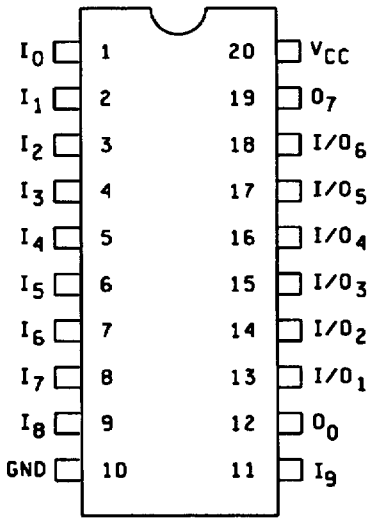
2/ Testing shall be performed using C_L = 5 pF.

3/ Test applies only to register outputs.

4/ The total clock period of CLK high and CLK low must not exceed clock frequency, f_{clock}. Minimum pulse durations specified are only for CLK high or CLK low, but not for both simultaneously.

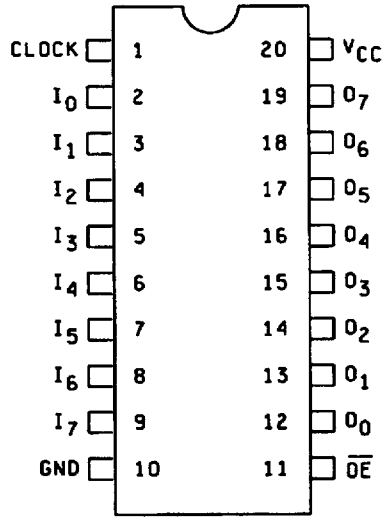
DEVICE TYPES 01,05,09,13, AND 17

CASE R AND S



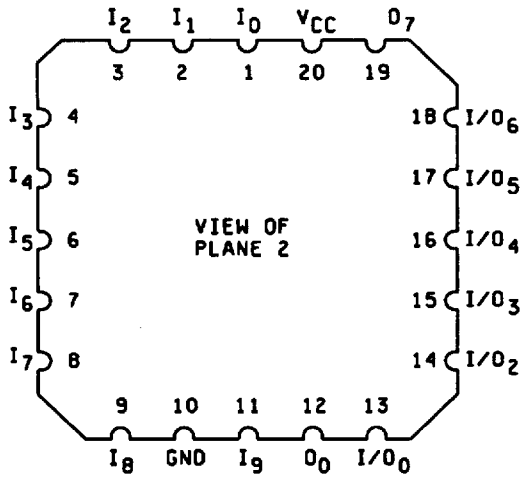
DEVICE TYPES 02,06,10,14,18, AND 21

CASE R AND S



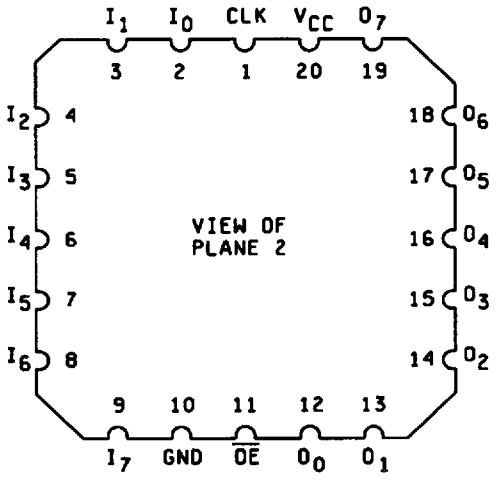
DEVICE TYPES 01,05,09,13, AND 17

CASE 2



DEVICE TYPES 02,06,10,14,18, AND 21

CASE 2



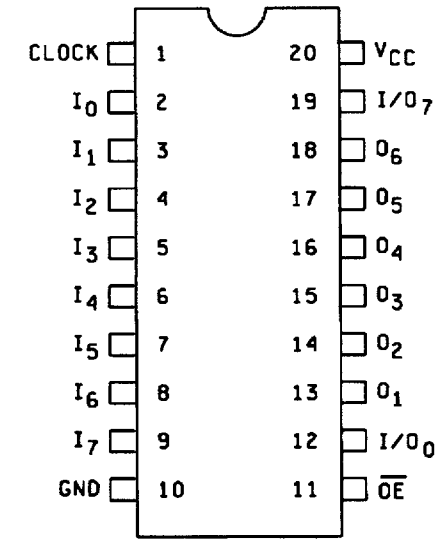
Option A with active terminals on plane 1.

Option A with active terminals on plane 1.

FIGURE 1. Terminal connections.

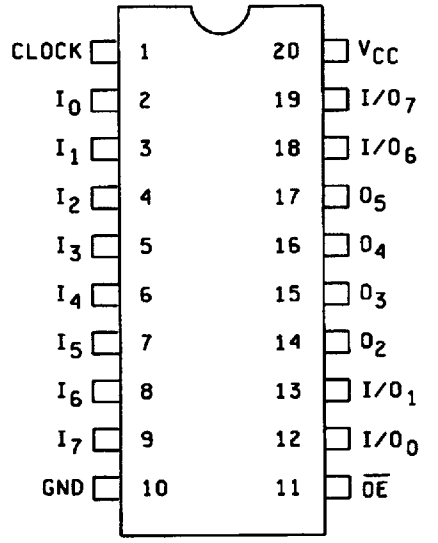
DEVICE TYPES 03,07,11,15, AND 19

CASE R AND S



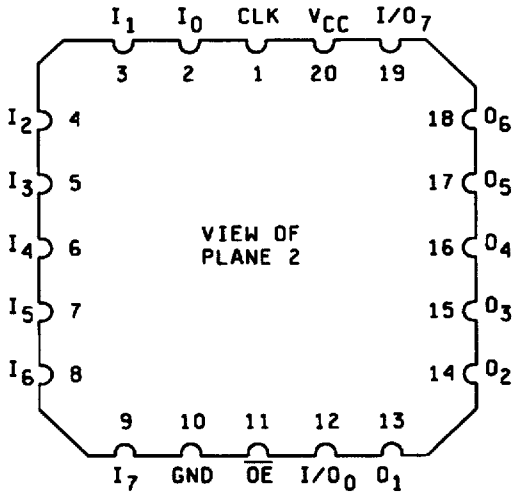
DEVICE TYPES 04,08,12,16,20, AND 22

CASE R AND S



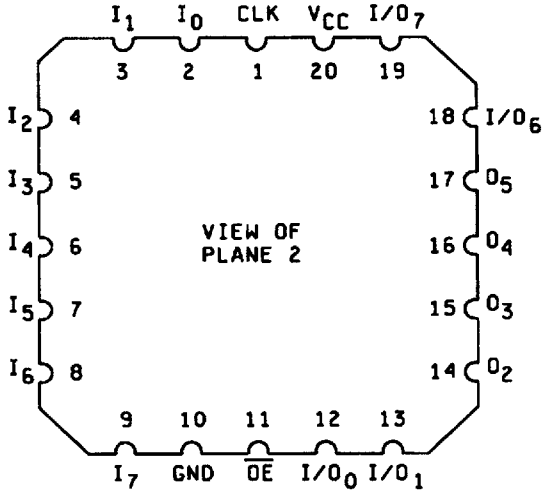
DEVICE TYPES 03,07,11,15, AND 19

CASE 2



DEVICE TYPES 04,08,12,16,20, AND 22

CASE 2



Option A with active terminals on plane 1.

Option A with active terminals on plane 1.

FIGURE 1. Terminal connections - Continued.

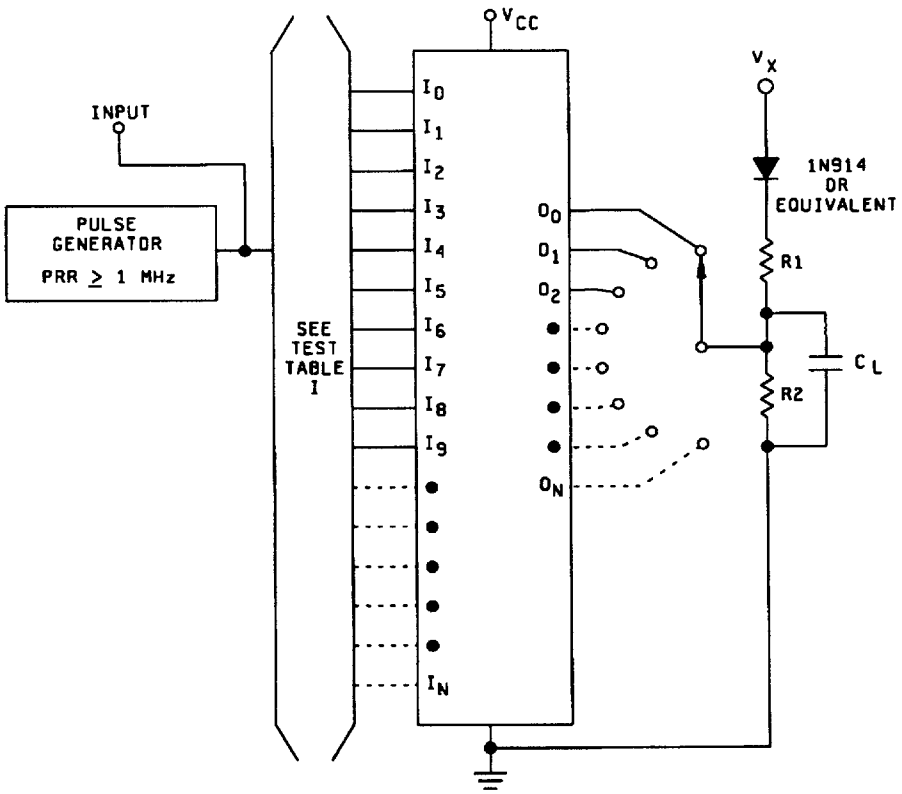
Device types 01 through 22

Truth table

Address												Output level								
CK	$\overline{OE}$	I_9	I_8	I_7	I_6	I_5	I_4	I_3	I_2	I_1	I_0	O_7	O_6	O_5	O_4	O_3	O_2	O_1	O_0	Device
		X	X	X	X	X	X	X	X	X	X	Z	Z	Z	Z	Z	Z	Z	Z	01,05, 09,13, 17
CK	L			X	X	X	X	X	X	X	X	H	H	H	H	H	H	H	H	02,06, 10,14, 18,21
CK	L			X	X	X	X	X	X	X	X	Z	H	H	H	H	H	H	Z	03,07, 11,15, 19
CK	L			X	X	X	X	X	X	X	X	Z	Z	H	H	H	H	Z	Z	04,08, 12,16, 20,22

NOTES:
1. Z = three-state.
2. Clock (pin 1): Low to high transition required to obtain valid data after last address transition.
3. Enable (pin 11): Must be low to enable output.

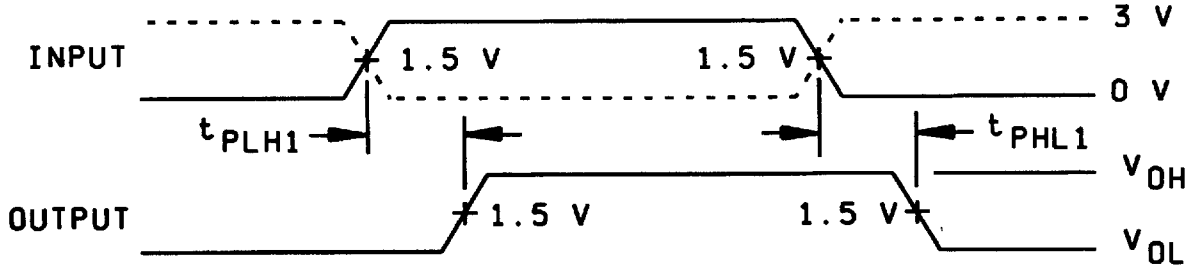
FIGURE 2. Truth table (unprogrammed).



TEST CIRCUIT

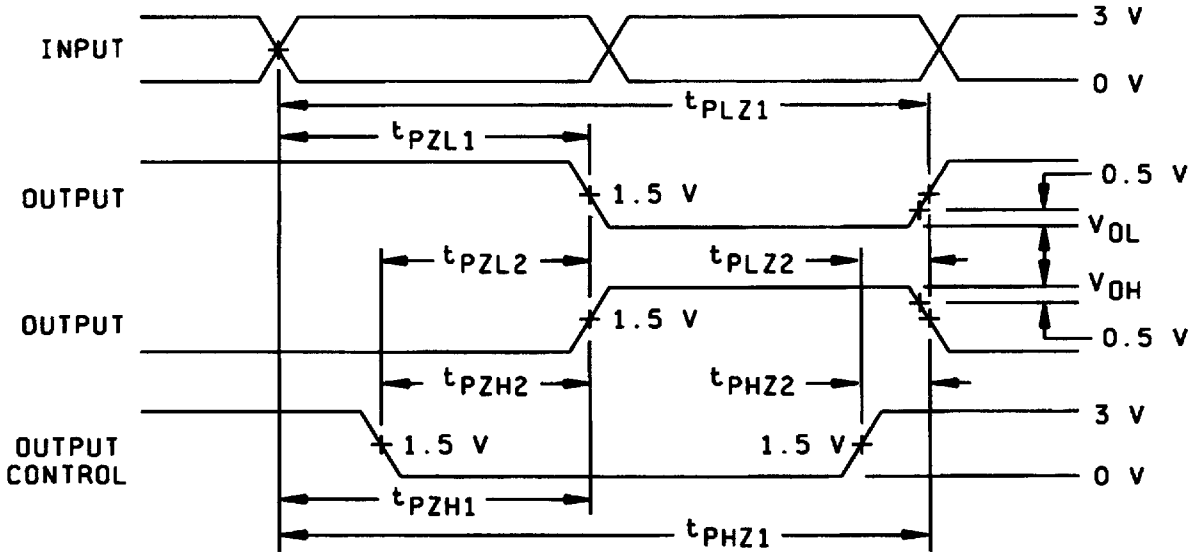
NOTES:
1. CL = 50 pF minimum, including jig and probe capacitance; R1 = 365Ω ±2%; R2 = 715Ω ±2%.
2. The tests shall check all inputs, gates, and outputs that have been programmed. The test shall be performed VCC = 4.5 V and 5.5 V.
3. V_X = 5.7 V for t_{PLH}, t_{PHL}, t_{PZL}, and t_{PLZ} tests and 0 V for t_{PHZ}, t_{PZH} and f_{max} tests.

Test circuit

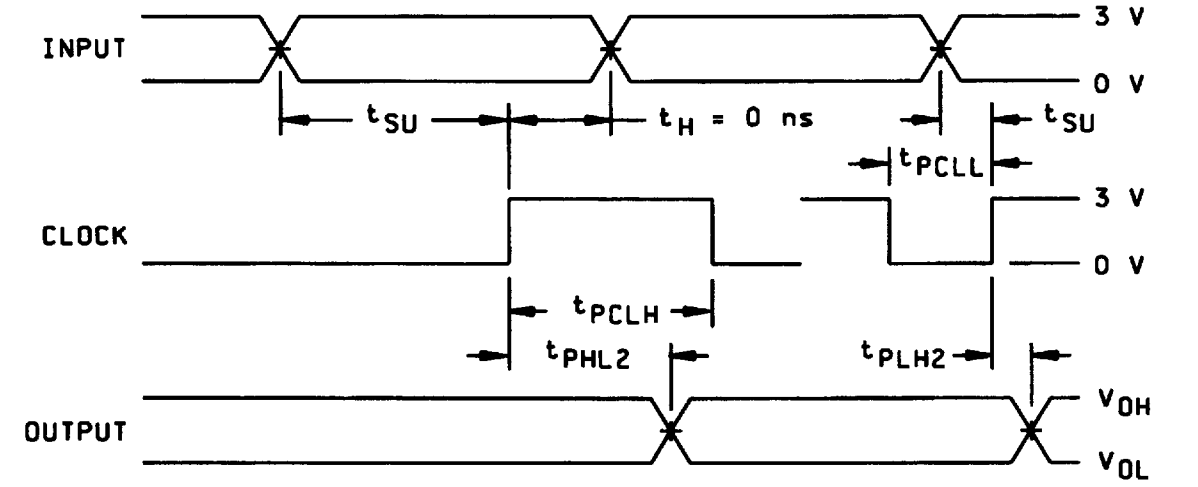


NON-REGISTERED SWITCHING WAVEFORMS

FIGURE 3. Test circuit and switching waveforms.



INPUT AND OUTPUT CONTROL SWITCHING WAVEFORM



REGISTERED SWITCHING WAVEFORM

FIGURE 3. Test circuit and switching waveforms - Continued.

4.3 Quality conformance inspection. Quality conformance inspection shall be in accordance with method 5005 of MIL-STD-883 including groups A, B, C, and D inspections. The following additional criteria shall apply.

4.3.1 Group A inspection.

a. Tests shall be as specified in table II herein.

b. Subgroups 4, 5, and 6 in table I, method 5005 of MIL-STD-883 shall be omitted.

c. Unprogrammed devices shall be tested for programmability and ac performance compliance to the requirements of group A, subgroups 9, 10, and 11. Either of the two following techniques is acceptable:

(1) Testing the entire lot using additional built-in test circuitry which allows the manufacturer to verify programmability and ac performance without programming the user array. If this is done, the resulting test patterns shall be verified on all devices during subgroups 9, 10, and 11, group A testing in accordance with the sampling plan specified in method 5005 of MIL-STD-883.

(2) If such compliance cannot be tested on an unprogrammed device, a sample shall be selected to satisfy programmability requirements prior to performing subgroups 9, 10, and 11. Twelve devices shall be submitted to programming (see 3.2.3.1). If more than two devices fail to program, the lot shall be rejected. At the manufacturer's option, the sample may be increased to 24 total devices with no more than 4 total device failures allowable. Ten devices from the programmability sample shall be submitted to the requirements of group A, subgroups 9, 10, and 11. If more than two total devices fail, the lot shall be rejected. At the manufacturers option, the sample may be increased to 20 total devices with no more than 4 total device failures allowable.

4.3.2 Groups C and D inspections.

a. End-point electrical parameters shall be as specified in table II herein.

b. Steady-state life test conditions, method 1005 of MIL-STD-883.

(1) Test condition A, B, C, or D using the circuit submitted with the certificate of compliance (see 3.7 herein).

(2) T_A = +125°C, minimum.

(3) Test duration: 1,000 hours, except as permitted by method 1005 of MIL-STD-883.

4.4 Programming procedures. The programming procedures shall be as specified by the device manufacturer.

5. PACKAGING

5.1 Packaging requirements. The requirements for packaging shall be in accordance with MIL-PRF-38535, appendix A.

6. NOTES

6.1 Intended use. Microcircuits conforming to this drawing are intended for use for Government microcircuit applications (original equipment), design applications, and logistics purposes.

6.2 Replaceability. Microcircuits covered by this drawing will replace the same generic device covered by a contractor-prepared specification or drawing.

TABLE II. Electrical test requirements. *

MIL-STD-883 test requirements	Subgroups (per method 5005, table I)
Interim electrical parameters (method 5004)	1
Final electrical test parameters (method 5004) for unprogrammed devices	1**, 2, 3, 7**, 8
Final electrical test parameters (method 5004) for programmed devices	1**, 2, 3, 7**, 8, 9
Group A test requirements (method 5005)	1, 2, 3, 7, 8, 9, 10***, 11***
Groups C and D end-point electrical parameters (method 5005)	1, 2, 3, 7, 8

* Indicates any or all subgroups may be combined when using high-speed testers. Subgroups 7 and 8 functional tests shall verify the truth table of figure 2, for unprogrammed devices or that the altered item drawing pattern exists for programmed devices.

** Indicates PDA applies to subgroups 1 and 7.

*** Subgroups 10 and 11, if not tested, shall be guaranteed to the specified limits in table I.

6.3 Configuration control of SMD's. All proposed changes to existing SMD's will be coordinated with the users of record for the individual documents. This coordination will be accomplished in accordance with MIL-STD-973 using DD Form 1692, Engineering Change Proposal.

6.4 Record of users. Military and industrial users shall inform Defense Electronics Supply Center when a system application requires configuration control and the applicable SMD. DESC will maintain a record of users and this list will be used for coordination and distribution of changes to the drawings. Users of drawings covering microelectronics devices (FSC 5962) should contact DESC-EC, telephone (513) 296-6047.

6.5 Comments. Comments on this drawing should be directed to DESC-EC, Dayton, Ohio 45444-5270, or telephone (513) 296-5377.

6.6 Approved sources of supply. Approved sources of supply are listed in MIL-HDBK-103. The vendors listed in MIL-HDBK-103 have agreed to this drawing and a certificate of compliance (see 3.6 herein) has been submitted to and accepted by DESC-EC.