REVISIONS			
LTR	DESCRIPTION	DATE	APPROVED
A	Add a LCC package. In table I, change I_{IN} from -8 mA to -18 mA.	8 June 1987	

REV																															
PAGE																															
REV STATUS	REV	A	A		A			A										A													
OF PAGES	PAGES	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16														

Defense Electronics Supply Center
Dayton, Ohio

Original date of drawing:

2 May 1986

AMSC N/A

PREPARED BY
Sandra Rooney

CHECKED BY
D. DiEnzo

APPROVED BY
M. A. Hauck

SIZE
A

CODE IDENT. NO.
14933

REV A

MILITARY DRAWING

This drawing is available for use by all Departments and Agencies of the Department of Defense

TITLE: MICROCIRCUITS, DIGITAL, 256 X 8-BIT BIPOLAR RAM, MONOLITHIC SILICON

DWG NO. 5962-86052

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5962-E379

DISTRIBUTION STATEMENT A. Approved for public release; distribution is unlimited.

DESC FORM 193

1. SCOPE

1.1 Scope. This drawing describes device requirements for class B microcircuits in accordance with 1.2.1 of MIL-STD-883, "Provisions for the use of MIL-STD-883 in conjunction with compliant non-JAN devices".

1.2 Part number. The complete part number shall be as shown in the following example:

5962-86052	01	W	X
Drawing number	Device type (1.2.1)	Case outline (1.2.2)	Lead finish per MIL-M-38510

1.2.1 Device type. The device type shall identify the circuit function as follows:

Device type	Generic number	Circuit function
01	8X350	2048-bit bipolar RAM

1.2.2 Case outline. The case outline shall be as designated in appendix C of MIL-M-38510, and as follows:

Outline letter	Case outline
W	D-7 (22-lead, 3/8" x 1 1/8"), dual-in-line package
3	C-4 (28-terminal, .450" x .450"), square chip carrier package

1.3 Absolute maximum ratings.

Supply voltage	+7 V dc maximum
Input voltage	+5.5 V dc maximum
Storage temperature range	-65°C to +150°C
Maximum power dissipation (P_D)	1.05 W 1/
Lead temperature (soldering, 10 seconds)	+300°C
Thermal resistance, junction-to-case (θ_{JC})	See MIL-M-38510, appendix C
Junction temperature (T_J)	+200°C

1.4 Recommended operating conditions.

Supply voltage range (V_{CC})	+4.75 V dc to +5.25 V dc
Case operating temperature range (T_C)	-55°C to +125°C
Minimum high level input voltage	2.0 V dc
Maximum high level input voltage	0.8 V dc

1/ Must withstand the added P_D due to short circuit test (e.g., I_{OS}).

2. APPLICABLE DOCUMENTS

2.1 Government specification and standard. Unless otherwise specified, the following specification and standard, of the issue listed in that issue of the Department of Defense Index of Specifications and Standards specified in the solicitation, form a part of this drawing to the extent specified herein.

SPECIFICATION

MILITARY

MIL-M-38510 - Microcircuits, General Specification for.

STANDARD

MILITARY

MIL-STD-883 - Test Methods and Procedures for Microelectronics.

(Copies of the specification and standard required by manufacturers in connection with specific acquisition functions should be obtained from the contracting activity or as directed by the contracting activity.)

2.2 Order of precedence. In the event of a conflict between the text of this drawing and the references cited herein, the text of this drawing shall take precedence.

3. REQUIREMENTS

3.1 Item requirements. The individual item requirements shall be in accordance with 1.2.1 of MIL-STD-883, "Provisions for the use of MIL-STD-883 in conjunction with compliant non-JAN devices" and as specified herein.

3.2 Design, construction, and physical dimensions. The design, construction, and physical dimensions shall be as specified in MIL-M-38510 and herein.

3.2.1 Terminal connections. The terminal connections shall be as specified on figure 1.

3.2.2 Truth table. The truth table shall be as specified on figure 2.

3.2.3 Logic diagram. The logic diagram shall be as specified on figure 3.

3.2.4 Case outline. The case outline shall be in accordance with 1.2.2 herein.

3.3 Electrical performance characteristics. Unless otherwise specified, the electrical performance characteristics are as specified in table I and apply over the full recommended case operating temperature range.

3.4 Marking. Marking shall be in accordance with MIL-STD-883 (see 3.1 herein). The part shall be marked with the part number listed in 1.2 herein. In addition, the manufacturer's part number may also be marked as listed in 6.4 herein.

TABLE I. Electrical performance characteristics.

Test	Symbol	Conditions 1/ 2/ $-55°C < T_C < +125°C$ $4.75\ V < V_{CC} < 5.25\ V$ See figures 4 and 5	Group A subgroups	Limits Min	Limits Max	Unit
Input voltage low	V_{IL}		1,2,3		0.8	V
Input voltage high	V_{IH}		1,2,3	2.0		V
Input voltage clamp 3/	V_{IC}	V_{CC} = Min, I_{IN} = -18 mA	1,2,3		-1.2	V
Output voltage low 4/	V_{OL}	V_{CC} = Min, I_{OL} = 9.6 mA	1,2,3		0.5	V
Output voltage high 5/	V_{OH}	V_{CC} = Min, I_{OH} = -2 mA	1,2,3	2.4		V
Input current low	I_{IL}	V_{CC} = Max, V_{IN} = 0.45 V	1,2,3		-150	µA
Input current high	I_{IH}	V_{CC} = Max, V_{IN} = 5.5 V	1,2,3		50	µA
Output current high Z state	I_{OZ}	V_{CC} = Max, $\overline{ME}$ = High, V_{OUT} = 5.5 V $\overline{ME}$ = High, V_{OUT} = 0.5 V	1,2,3		80 -100	µA
Output current short circuit 3/ 6/	I_{OS}	SC = WC, $\overline{ME}$ = Low, V_{OUT} = 0V, stored high, V_{CC} = Max	1,2,3	-15	-85	mA
V_{CC} supply current 7/	I_{CC}	$\overline{ME}$ = High, V_{CC} = Max	1,2,3		200	mA
Output enable time from SC- to data out	T_{E1}	See figures 6 and 7	9,10,11		40	ns
Output enable time from $\overline{ME}$- to data out	T_{E2}		9,10,11		40	ns
Output disable time from SC+ to data out	T_{D1}		9,10,11		40	ns
Output disable time from $\overline{ME}$+ to data out	T_{D2}		9,10,11		40	ns
Pulse width master clock 8/	T_W		9,10,11	50		ns

See footnotes at end of table.

TABLE I. Electrical performance characteristics.

Test	Symbol	Conditions 1/ 2/ $-55°C \le T_C \le +125°C$, $4.75\ V \le V_{CC} \le 5.25\ V$, See figures 4 and 5	Group A subgroups	Limits Min	Limits Max	Unit
Setup time from address to to MCLK-	T_{SA}	See figures 6 and 7	9,10,11	40		ns
Hold time from MCLK- to address	T_{HA}		9,10,11	10		ns
Setup time from data in to MCLK-	T_{SD}		9,10,11	45		ns
Hold time from MCLK- to data in	T_{HD}		9,10,11	10		ns
Setup time from $\overline{ME}$- to MCLK-	T_{S3}		9,10,11	50		ns
Hold time from MCLK- to $\overline{ME}$+	T_{H3}		9,10,11	5		ns
Setup time from $\overline{ME}$- to MCLK-	T_{S1}		9,10,11	40		ns
Hold time from MCLK- to ME-	T_{H2}		9,10,11	5		ns
Setup time from SC-, WC- to $\overline{ME}$	T_{S2}		9,10,11	5		ns
Hold time from MCLK- to SC-	T_{H1}		9,10,11	5		ns
Hold time from MCLK- to WC-	T_{H4}		9,10,11	5		ns

1/ All voltage values are with respect to network ground terminal.

2/ The operating case temperature ranges are guaranteed with transverse air flow exceeding 400 linear feet per minute and a 2 minute warmup. Typical thermal resistance values of the package at maximum temperature are:
θ_{JC} junction-to-case at 400 fpm air flow: 50°C/W
θ_{JC} junction-to-case still air: 90°C/W
θ_{JC} junction-to-case: 20°C/W

3/ Test each pin one at a time.

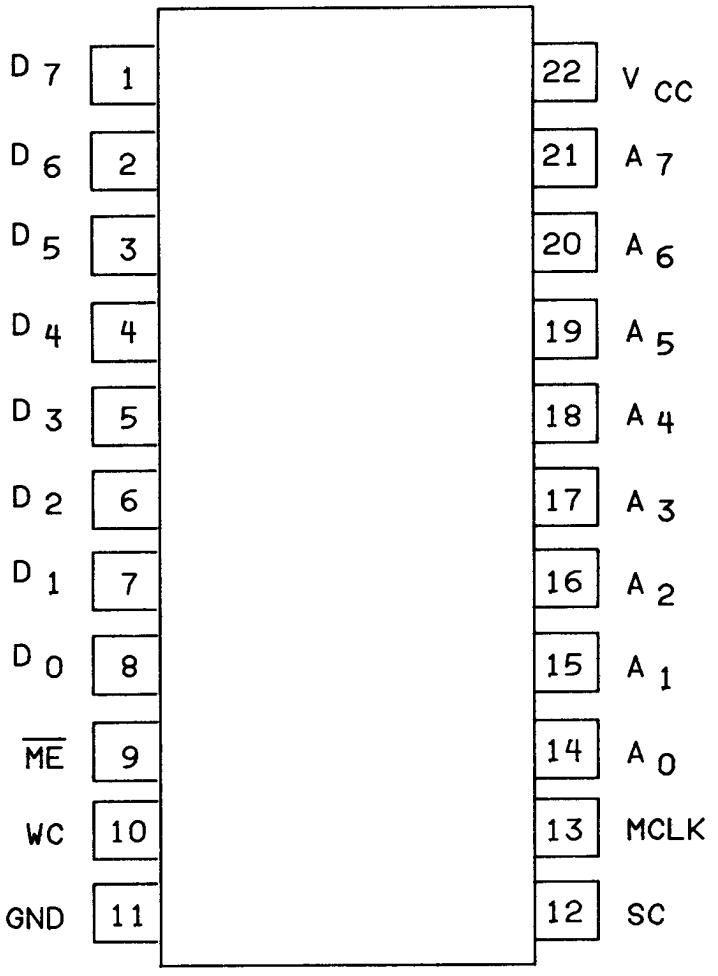
4/ Measured with a logic low stored. Output sink current is supplied through a resistor to V_{CC}.

5/ Measured with a logic high.

6/ Duration of the short circuit should not exceed 1 second.

7/ I_{CC} is measured with the write enable and memory enable inputs grounded, all other inputs at 4.5 V and the output open.

8/ Minimum required to guarantee a write into the slowest bit.



TOP VIEW

FIGURE 1. Terminal connections.

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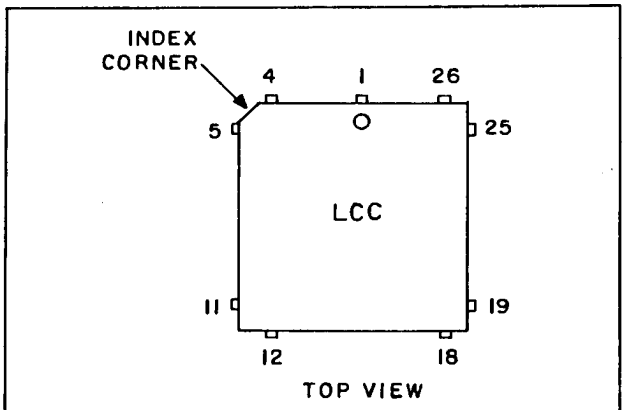

PIN	FUNCTION	PIN	FUNCTION
1	NC	15	NC
2	D_7	16	SC
3	D_6	17	MCLK
4	D_5	18	NC
5	D_4	19	A_0
6	D_3	20	A_1
7	D_2	21	A_2
8	NC	22	NC
9	D_1	23	A_3
10	D_0	24	A_4
11	$\overline{ME}$	25	A_5
12	NC	26	A_6
13	WC	27	A_7
14	GND	28	V_{CC}

FIGURE 1. Terminal connections - Continued.

Mode	$\overline{ME}$	SC	WC	MCLK	Address Data Bus Lines
Hold address Disable data out	1	X	X	X	High Z data out
Input new address	0	1	0	1	Address High Z
Hold address Disable data out	0	1	0	0	High Z data out
Hold address Write data	0	0	1	1	Data in
Hold address Disable data out	0	0	1	0	High Z data out
Hold address Read data	0	0	0	X	Data out
Undefined state	0	1	1	1	-
Hold address Disable data out	0	1	1	0	High Z data out

NOTES: X = Don't care.
The SC and WC outputs from the 8X300 are never at 1 simultaneously.

FIGURE 2. Truth table.

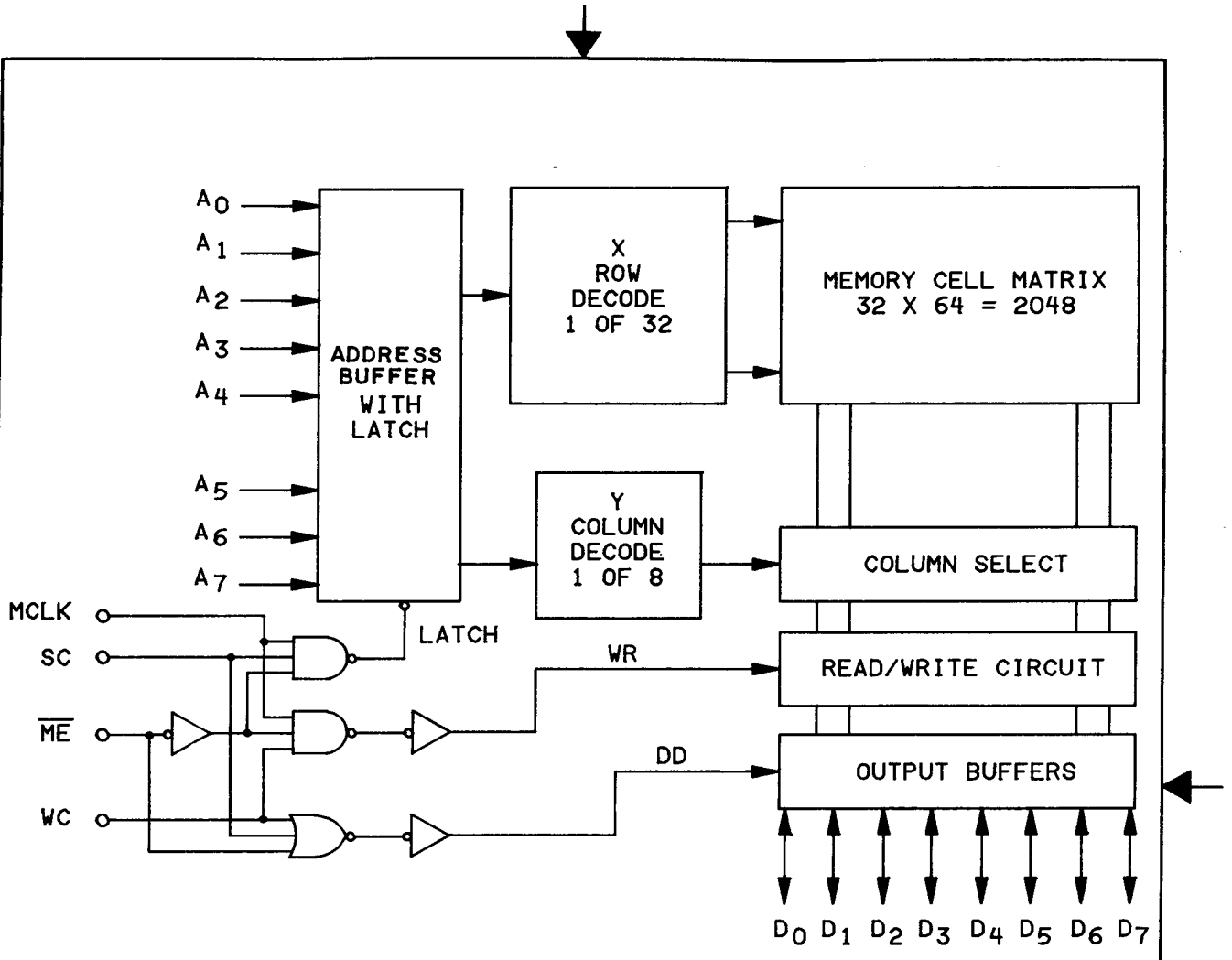

FIGURE 3. Logic diagram.

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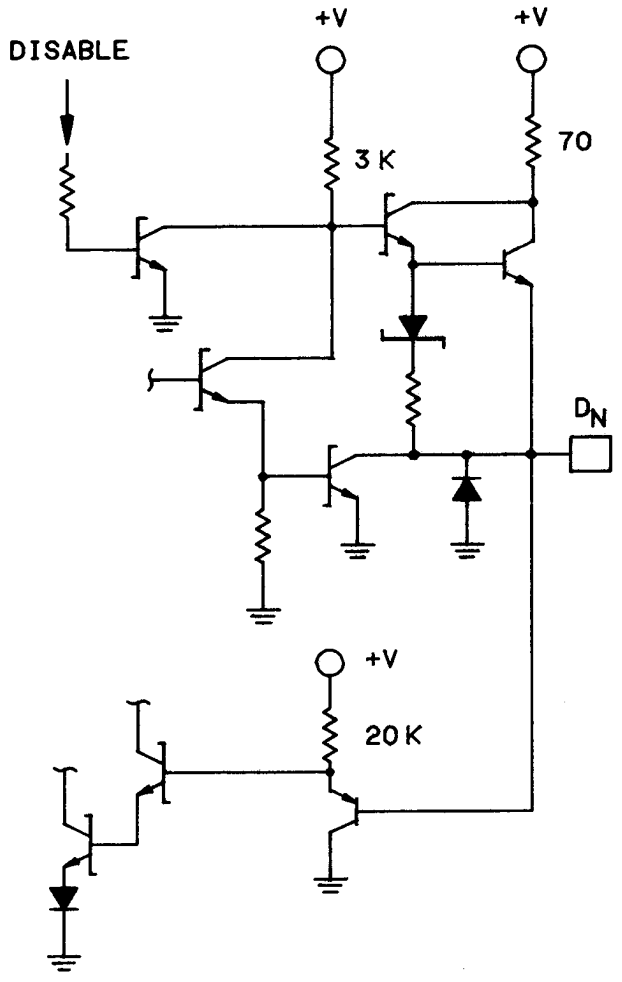
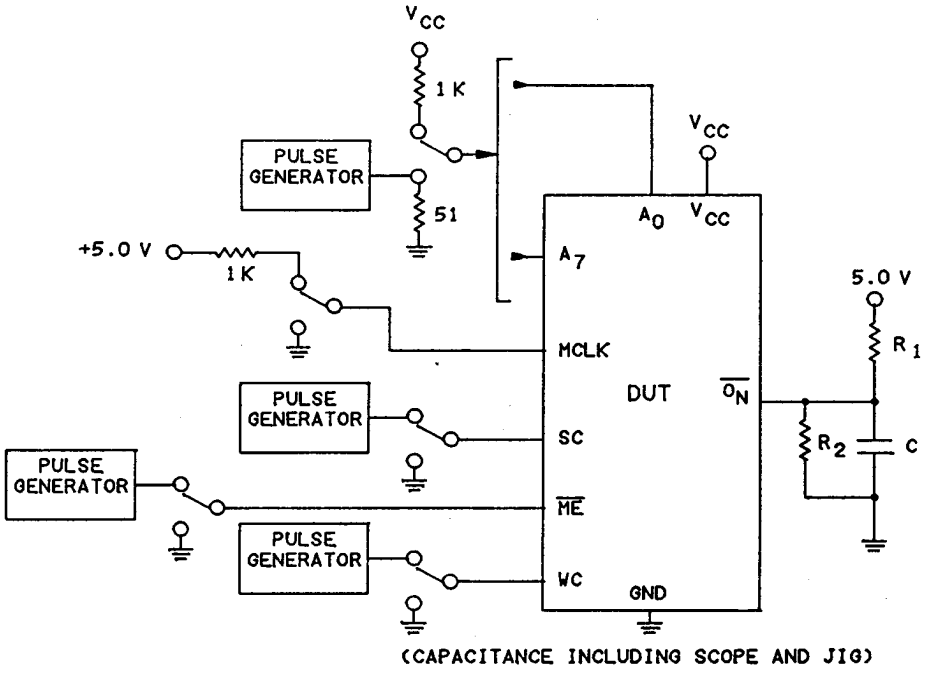


FIGURE 4. Typical I/O structure.

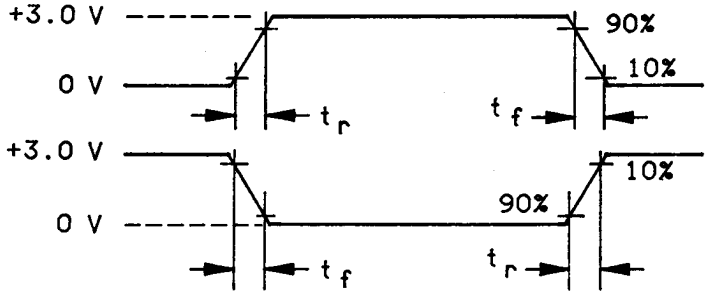


(CAPACITANCE INCLUDING SCOPE AND JIG)

ALL RESISTOR VALUES ARE TYPICAL AND IN OHMS

FIGURE 5. Test load circuit.

ALL INPUT PULSES



MEASUREMENTS: ALL CIRCUIT DELAYS ARE MEASURED AT THE +1.5 V LEVEL OF INPUTS AND OUTPUT.

NOTE: t_r, $t_f \leq 5$ ns

FIGURE 6. Voltage waveform.

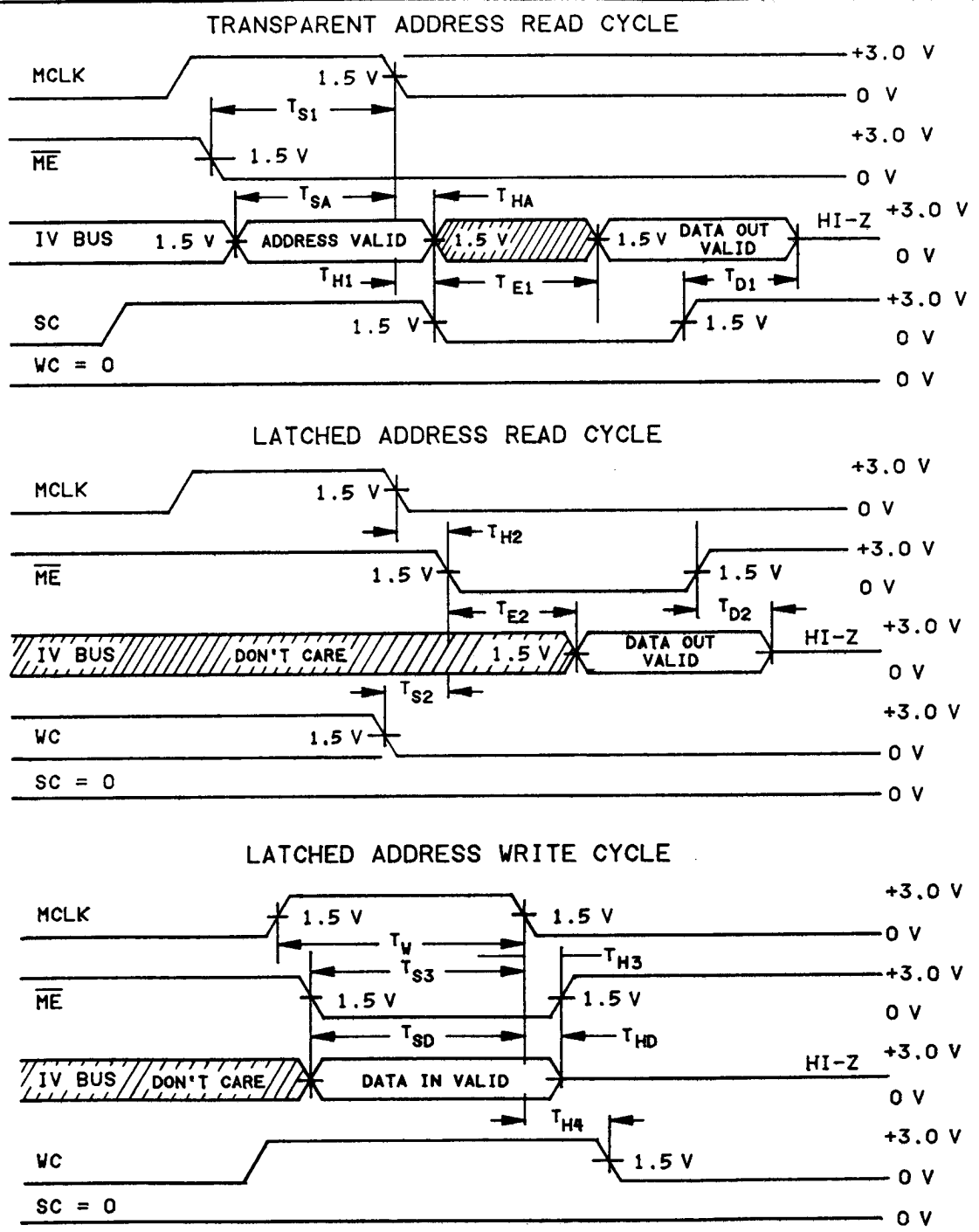


FIGURE 7. Timing diagrams.

TIMING DEFINITIONS

T_{S1}	Required delay between beginning of Master Enable low and falling edge of Master Clock.
T_{SA}	Required delay between beginning of valid address and falling edge of Master Clock.
T_{HA}	Required delay between falling edge of Master Clock and end of valid Address.
T_{H1}	Required delay between falling edge of Master Clock and when Select Command becomes low.
T_{E1}	Delay between beginning of Select Command low and beginning of valid data output on the IV Bus.
T_{D1}	Delay between when select Command becomes high and end of valid data output on the IV Bus.
T_{H2}	Required delay between falling edge of Master Clock and when Master Enable becomes low.
T_{E2}	Delay between when Master Enable becomes low and beginning of valid data output on the IV Bus.
T_{D2}	Delay between when Master Enable becomes high and end of valid data output on the IV Bus.
T_{S2}	Required delay between when Select Command or Write Command becomes low and when Master Enable becomes low.
T_{W}	Minimum width of the Master Clock pulse.
T_{S3}	Required delay between when Master Enable becomes low and falling edge of Master Clock.
T_{H3}	Required delay between falling edge of Master Clock and when Master Enable becomes high.
T_{SD}	Required delay between beginning of valid data input on the IV Bus and falling edge of Master Clock.
T_{HD}	Required delay between falling edge of Master Clock and end of valid data input on the IV Bus.
T_{H4}	Required delay between falling edge of Master Clock and when Write Command becomes low.

NOTES:
SC + ME = 1 to avoid bus conflict
WC + ME = 1 to avoid bus conflict
The SC and WC outputs from the 8X300 are never at 1 simultaneously.

FIGURE 7. Timing diagrams - Continued.

3.5 Certificate of compliance. A certificate of compliance shall be required from a manufacturer in order to be listed as an approved source of supply in 6.4. The certificate of compliance submitted to DESC-ECS prior to listing as an approved source of supply shall state that the manufacturer's product meets the requirements of MIL-STD-883 (see 3.1 herein) and the requirements herein.

3.6 Certificate of conformance. A certificate of conformance as required in MIL-STD-883 (see 3.1 herein) shall be provided with each lot of microcircuits delivered to this drawing.

3.7 Notification of change. Notification of change to DESC-ECS shall be required in accordance with MIL-STD-883 (see 3.1 herein).

3.8 Verification and review. DESC, DESC's agent, and the acquiring activity retain the option to review the manufacturer's facility and applicable required documentation. Offshore documentation shall be made available onshore at the option of the reviewer.

4. QUALITY ASSURANCE PROVISIONS

4.1 Sampling and inspection. Sampling and inspection procedures shall be in accordance with section 4 of MIL-M-38510 to the extent specified in MIL-STD-883 (see 3.1 herein).

4.2 Screening. Screening shall be in accordance with method 5004 of MIL-STD-883, and shall be conducted on all devices prior to quality conformance inspection. The following additional criteria shall apply:

a. Burn-in test (method 1015 of MIL-STD-883).

(1) Test condition A, B, C, or D using the circuit submitted with the certificate of compliance (see 3.5 herein).

(2) T_A = +125°C, minimum.

b. Interim and final electrical test parameters shall be as specified in table II herein, except interim electrical parameter tests prior to burn-in are optional at the discretion of the manufacturer.

4.3 Quality conformance inspection. Quality conformance inspection shall be in accordance with method 5005 of MIL-STD-883 including groups A, B, C, and D inspections. The following additional criteria shall apply.

4.3.1 Group A inspection.

a. Tests shall be as specified in table II herein.

b. Subgroups 4, 5, and 6 in table I, method 5005 of MIL-STD-883 shall be omitted.

c. Subgroup 7 functional testing shall include verification of instruction set.

4.3.2 Groups C and D inspections.

a. End-point electrical parameters shall be as specified in table II herein.

b. Steady-state life test (method 1005 of MIL-STD-883) conditions:

(1) Test condition A, B, C, or D using the circuit submitted with the certificate of compliance (see 3.5 herein).

(2) T_A = +125°C, minimum.

(3) Test duration: 1,000 hours, except as permitted by appendix B of MIL-M-38510 and method 1005 of MIL-STD-883.

TABLE II. Electrical test requirements.

MIL-STD-883 test requirements	Subgroups (per method 5005, table I)
Interim electrical parameters (method 5004)	---
Final electrical test parameters (method 5004)	1*,2,3,7,8,9
Group A test requirements (method 5005)	1,2,3,7,8,9, 10,11
Groups C and D end-point electrical parameters (method 5005)	1,2,3
Additional electrical subgroups for group C periodic inspections	---

*PDA applies to subgroup 1.

5. PACKAGING

5.1 Packaging requirements. The requirements for packaging shall be in accordance with MIL-M-38510.

6. NOTES

6.1 Intended use. Microcircuits conforming to this drawing are intended for use when military specifications do not exist and qualified military devices that will perform the required function are not available for OEM application. When a military specification exists and the product covered by this drawing has been qualified for listing on QPL-38510, the device specified herein will be inactivated and will not be used for new design. The QPL-38510 product shall be the preferred item for all applications.

6.2 Replaceability. Microcircuits covered by this drawing will replace the same generic device covered by a contractor-prepared specification or drawing.

6.3 Comments. Comments on this drawing should be directed to DESC-ECS, Dayton, Ohio 45444, or telephone 513-296-5375.

6.4 Approved source of supply. An approved source of supply is listed herein. Additional sources will be added as they become available. The vendor listed herein has agreed to this drawing and a certificate of compliance (see 3.5 herein) has been submitted to DESC-ECS.

Military drawing part number	Vendor CAGE number	Vendor similar part number 1/	Replacement military specification part number
5962-8605201WX	18324	8X350/BWA	---
5962-86052013X	18324	8X350/B3X	---

1/ Caution. Do not use this number for item acquisition. Items acquired to this number may not satisfy the performance requirements of this drawing.

Vendor CAGE number	Vendor name and address
18324	Signetics, Incorporated 4130 S. Market Court Sacramento, CA 95834