REVISIONS			
LTR	DESCRIPTION	DATE (YR-MO-DA)	APPROVED
A	Table I, pages 4 and 5, change: V_{OH} from 2.5 V to 2.4 V. f_{MAX} (Min), subgroup 9, from 100 MHz to 90 MHz and subgroups 10 and 11 from 90 MHz to 75 MHz. t_{PLH4}, subgroups 10 and 11 from 15.5 ns to 16.5 ns. Add "5962" to the military drawing number in 6.4. Editorial changes on pages 2 and 8. Change code ident. to 67268.	1987 JULY 24	
B	Technical changes in 1.4, recommended operating conditions. Increased setup and hold time. Delete footnote 2/ from table I. Table I f_{MAX} test from 75 MHz to 60 MHz. Table I t_{PHL2} through t_{PHL4} increase maximum limits. Made editorial changes throughout document. Change in table II. Add CAGE 27014 to all packages. Add figure 5.	1989 JAN 3	

CURRENT CAGE CODE 67268

REV																									
SHEET																									
REV																									
SHEET																									
REV STATUS OF SHEETS	REV	B	B	B	B	B	B	B	B	B	B	B	B	B											
	SHEET	1	2	3	4	5	6	7	8	9	10	11	12	13											

PMIC N/A

STANDARDIZED MILITARY DRAWING

THIS DRAWING IS AVAILABLE FOR USE BY ALL DEPARTMENTS AND AGENCIES OF THE DEPARTMENT OF DEFENSE

AMSC N/A

PREPARED BY: Larry T. Gauder

CHECKED BY: D. Johnson

APPROVED BY: M. Cook

DRAWING APPROVAL DATE: 28 JANUARY 1987

REVISION LEVEL: B

DEFENSE ELECTRONICS SUPPLY CENTER
DAYTON, OHIO 45444

MICROCIRCUIT, DIGITAL ADVANCED SCHOTTKY TTL, BINARY COUNTER, MONOLITHIC SILICON

SIZE	CAGE CODE	5962-86072
A	14933	

SHEET 1 OF 13

DESC FORM 193-1
SEP 87

* U.S. GOVERNMENT PRINTING OFFICE: 1987 — 748-129/60912

5962-E1130

1. SCOPE

1.1 Scope. This drawing describes device requirements for class B microcircuits in accordance with 1.2.1 of MIL-STD-883, "Provisions for the use of MIL-STD-883 in conjunction with compliant non-JAN devices".

1.2 Part number. The complete part number shall be as shown in the following example:

5962-86072	01	E	X
Drawing number	Device type (1.2.1)	Case outline (1.2.2)	Lead finish per MIL-M-38510

1.2.1 Device type. The device type shall identify the circuit function as follows:

Device type	Generic number	Circuit function
01	54F169	Synchronous 4-bit up/down binary counter

1.2.2 Case outlines. The case outlines shall be as designated in appendix C of MIL-M-38510, and as follows:

Outline letter	Case outline
E	D-2 (16-lead, .840" x 310" x .200"), dual-in line package
F	F-5 (16-lead, .440" x .285" x .085"), flat package
2	C-2 (20 terminal, .358" x .358" x .100"), square chip carrier package

1.3 Absolute maximum ratings.

Supply voltage range	-0.5 V dc minimum to +7.0 V dc maximum
Input voltage range	-1.2 V dc at -18 mA to +7.0 V dc
Storage temperature	-65°C to +150°C
Maximum power dissipation (P_D)	413 mW
Lead temperature (soldering, 10 seconds)	+300°C
Thermal resistance, junction-to-case (θ_{JC}):	See MIL-M-38510, appendix C
Junction temperature (T_J)	+175°C

1.4 Recommended operating conditions.

Supply voltage (V_{CC})	4.5 V dc minimum to 5.5 V dc maximum
Minimum high level input voltage (V_{IH})	2.0 V dc
Maximum low level input voltage (V_{IL})	0.8 V dc
Case operating temperature range (T_C)	-55°C to +125°C
Minimum setup time, Dn to CP:	
T_C = +25°C	4.0 ns
T_C = -55°C, +125°C	4.5 ns
Minimum hold time, Dn to CP:	
T_C = +25°C	3.0 ns
T_C = -55°C, +125°C	3.5 ns

1/ Maximum power dissipation is defined as V_{CC} x I_{CC}, and must withstand the added P_D due to short circuit test; e. g., I_{OS}

Minimum setup time, $\overline{CEP}$ or $\overline{CET}$ to CP:	
T_C = +25°C	7.0 ns
T_C = -55°C, +125°C	8.0 ns
Minimum hold time, $\overline{CEP}$ or $\overline{CET}$ to CP	1.0 ns
Minimum setup time, $\overline{PE}$ to CP:	
T_C = +25°C	8.0 ns
T_C = -55°C, +125°C	10.0 ns
Minimum hold time, $\overline{PE}$ to CP	1.0 ns
Minimum setup time, U/$\overline{D}$ to CP:	
T_C = +25°C	11.0 ns
T_C = -55°C, +125°C	14.0 ns
Minimum hold time U/$\overline{D}$ to CP	0.0 ns
Minimum width of clock pulse	9.0 ns

2. APPLICABLE DOCUMENTS

2.1 Government specification and standard. Unless otherwise specified, the following specification and standard, of the issue listed in that issue of the Department of Defense Index of Specifications and Standards specified in the solicitation, form a part of this drawing to the extent specified herein.

SPECIFICATION

MILITARY

MIL-M-38510 - Microcircuits, General Specification for.

STANDARD

MILITARY

MIL-STD-883 - Test Methods and Procedures for Microelectronics.

(Copies of the specification and standard required by manufacturers in connection with specific acquisition functions should be obtained from the contracting activity or as directed by the contracting activity.)

2.2 Order of precedence. In the event of a conflict between the text of this drawing and the references cited herein, the text of this drawing shall take precedence.

3. REQUIREMENTS

3.1 Item requirements. The individual item requirements shall be in accordance with 1.2.1 of MIL-STD-883, "Provisions for the use of MIL-STD-883 in conjunction with compliant non-JAN devices" and as specified herein.

3.2 Design, construction, and physical dimensions. The design, construction, and physical dimensions shall be as specified in MIL-M-38510 and herein.

3.2.1 Terminal connections. The terminal connections shall be as specified on figure 1.

3.2.2 Truth tables. The truth tables shall be as specified on figure 2.

3.2.3 Logic diagram. The logic diagram shall be as specified on figure 3.

3.2.4 Counting sequence. The counting sequence diagram shall be as specified on figure 4.

3.2.5 Test circuit and switching waveforms. The test circuit and switching waveforms shall be as specified on figure 5.

TABLE I. Electrical performance characteristics.

Test	Symbol	Conditions $-55°C < T_C < +125°C$ unless otherwise specified		Group A subgroups	Limits		Unit
					Min	Max	
High level output voltage	V_{OH}	V_{CC} = 4.5 V; I_{OH} = -1.0 mA V_{IL} = 0.8 V; V_{IH} = 2.0 V		1, 2, 3	2.4		V
Low level output voltage	V_{OL}	V_{CC} = 4.5 V; I_{OL} = 20 mA V_{IL} = 0.8 V; V_{IH} = 2.0 V		1, 2, 3		0.5	V
Input clamp voltage	V_{IC}	V_{CC} = 4.5 V I_{IN} = -18 mA		1, 2, 3		-1.2	V
High level input current	I_{IH1}	V_{CC} = 5.5 V V_{IN} = 2.7 V		1, 2, 3		20	µA
	I_{IH2}	V_{CC} = 5.5 V V_{IN} = 7.0 V		1, 2, 3		100	µA
Low level input current	I_{IL}	V_{CC} = 5.5 V V_{IN} = 0.5 V	$\overline{CET}$ input	1, 2, 3		-1.2	mA
			other inputs	1, 2, 3		-0.6	mA
Short circuit output current	I_{OS}	V_{CC} = 5.5 V V_{OUT} = 0.0 V	1/	1, 2, 3	-60	-150	mA
Supply current	I_{CC}	V_{CC} = 5.5 V		1, 2, 3		75	mA
Functional tests		See 4.3.1c		7, 8			
Maximum clock frequency	f_{MAX}	V_{CC} = 5.0 V R_L = 500Ω C_L = 50 pF See figures 4 and 5		9	90		MHz
				10, 11	60		MHz

See footnotes at end of table.

TABLE I. Electrical performance characteristics - Continued.

Test	Symbol	Conditions $-55°C < T_C < +125°C$ unless otherwise specified	Group A subgroups	Limits		Unit
				Min	Max	
Propagation delay time, CP to Q_n ($\overline{PE}$ high or low)	t_{PLH1}	V_{CC} = 5.0 V R_L = 500Ω C_L = 50 pF See figures 4 and 5	9		9	ns
			10, 11		12	ns
	t_{PHL1}		9		12	ns
			10, 11		16	ns
Propagation delay time, CP to $\overline{TC}$	t_{PLH2}		9		16	ns
			10, 11		21	ns
	t_{PHL2}		9		12	ns
			10, 11		15	ns
Propagation delay time, $\overline{CET}$ to $\overline{TC}$	t_{PLH3}		9		6	ns
			10, 11		9	ns
	t_{PHL3}		9		11	ns
			10, 11		12	ns
Propagation delay time, U/$\overline{D}$ to $\overline{TC}$	t_{PLH4}		9		15	ns
			10, 11		16.5	ns
	t_{PHL4}		9		12	ns
			10, 11		14	ns

1/ Not more than one output should be shorted at a time, and the duration of the short circuit condition should not exceed 1 second.

Case outlines	E and F	2
Terminal number	Terminal symbol	
1	$U/\overline{D}$	NC
2	CP	$U/\overline{D}$
3	D_0	CP
4	D_1	D_0
5	D_2	D_1
6	D_3	NC
7	$\overline{CEP}$	D_2
8	GND	D_3
9	$\overline{PE}$	$\overline{CEP}$
10	$\overline{CET}$	GND
11	Q_3	NC
12	Q_2	$\overline{PE}$
13	Q_1	$\overline{CET}$
14	Q_0	Q_3
15	$\overline{TC}$	Q_2
16	V_{CC}	NC
17	---	Q_1
18	---	Q_0
19	---	$\overline{TC}$
20	---	V_{CC}

NC = No connection

FIGURE 1. Terminal connections.

$\overline{PE}$	$\overline{CEP}$	$\overline{CET}$	U/$\overline{D}$	Action on rising clock edge
L	X	X	X	Load (D_n-Q_n)
H	L	L	H	Count up (Increment)
H	L	L	L	Count down (Decrement)
H	H	X	X	No change (hold)
H	X	H	X	No change (hold)

H = High voltage level
L = Low voltage level
X = Irrelevant

Operating mode	Inputs						Outputs	
	CP	U/$\overline{D}$	$\overline{CEP}$	$\overline{CET}$	$\overline{PE}$	D_n	Q_n	$\overline{TC}$
Parallel load	↑	X	X	X	l	l	L	See note
	↑	X	X	X	l	h	H	See note
Count up	↑	h	l	l	h	X	Count up	See note
Count down	↑	l	l	l	h	X	Count down	See note
Hold (do nothing)	↑	X	h	X	h	X	q_n	See note
	↑	X	X	h	h	X	q_n	H

H = High voltage level steady state
h = High voltage level one setup time prior to the Low-to-High clock transition
L = Low voltage level steady state
l = Low voltage level one setup time prior the Low-to-High clock transition
X = Irrelevant
q = Lower case letters indicate the state of the referenced output prior to the Low-to-high clock transition
↑ = Low-to-high clock transition

NOTE: $\overline{TC}$ is LOW when $\overline{CET}$ is LOW and the counter is at terminal count. Terminal count when counting up is HHHH, and terminal count when counting down is LLLL.

FIGURE 2. Truth tables.

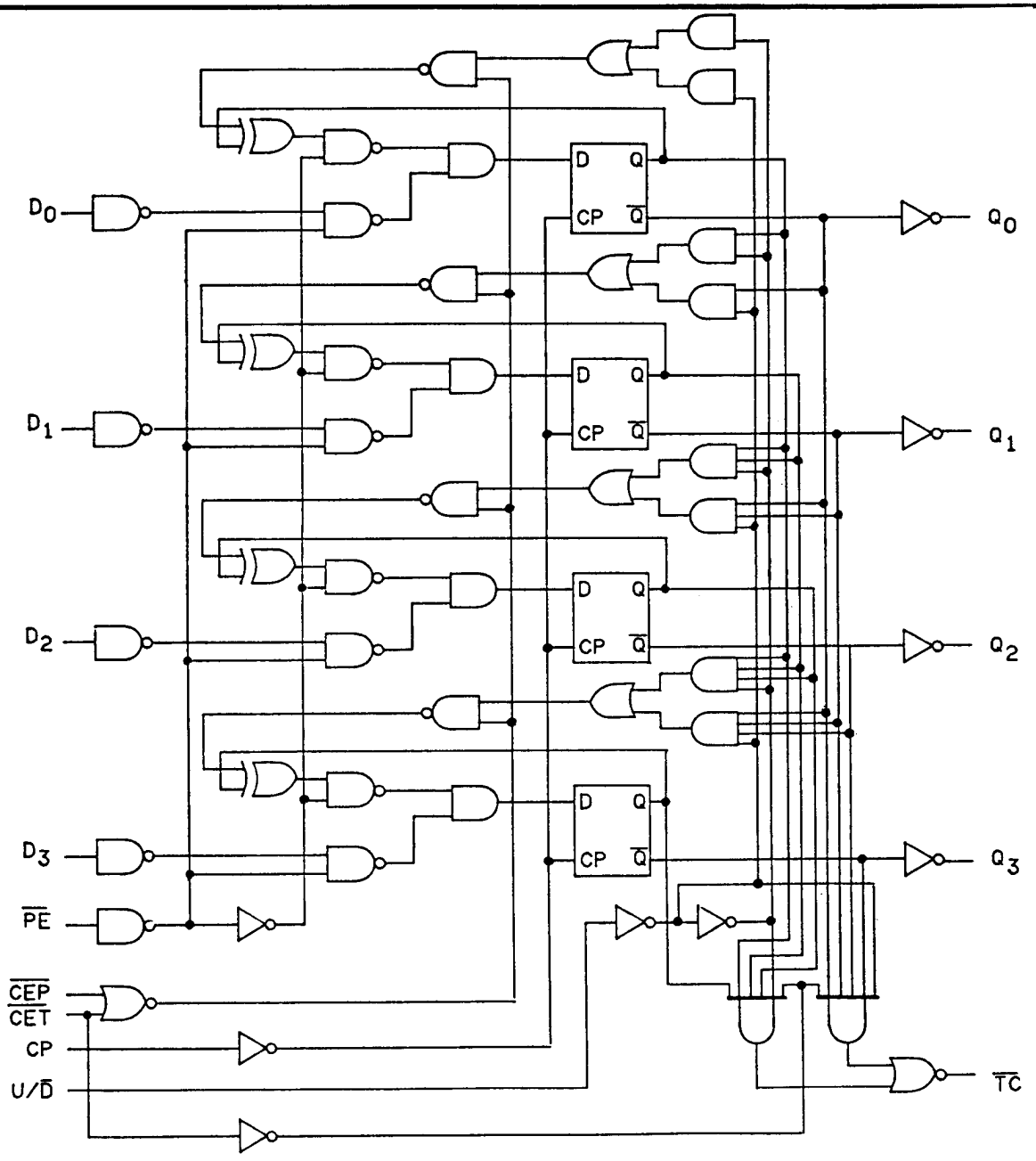
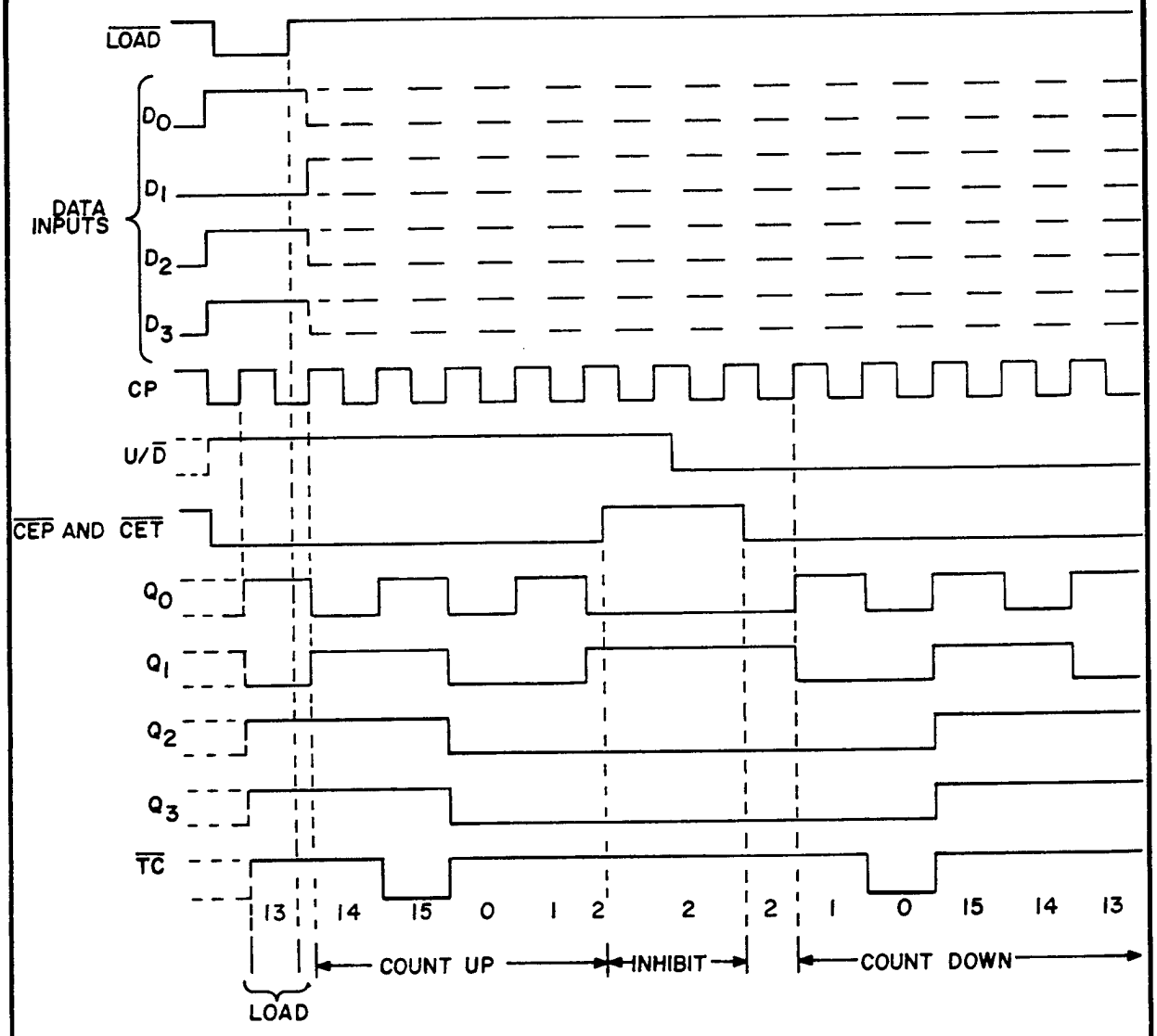
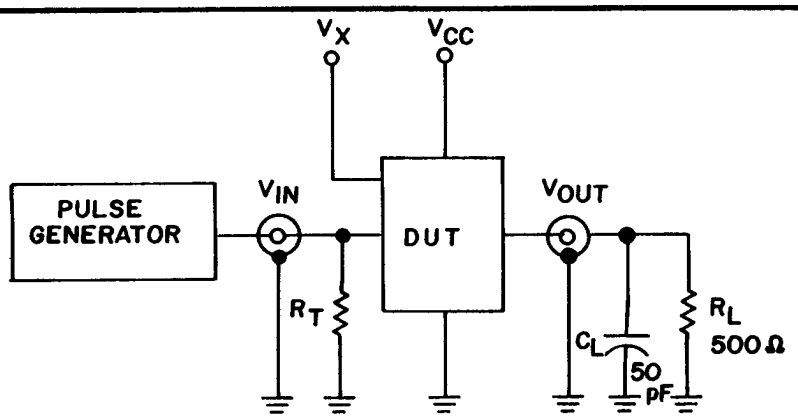


FIGURE 3. Logic diagram.

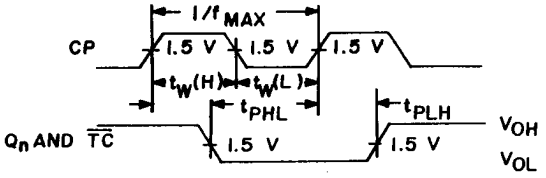


NOTES:
1. Load (preset) to binary thirteen.
2. Count up to fourteen, fifteen (maximum), zero, one, and two.
3. Inhibit.
4. Count down to one, zero (minimum), fifteen, fourteen, and thirteen.

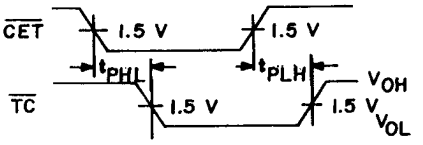
FIGURE 4. Counting sequence.



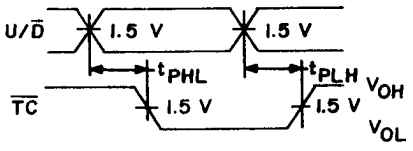
Test circuit or equivalent
Test circuit



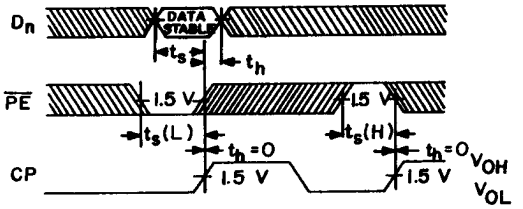
CLOCK TO OUTPUT DELAYS AND CLOCK PULSE WIDTH



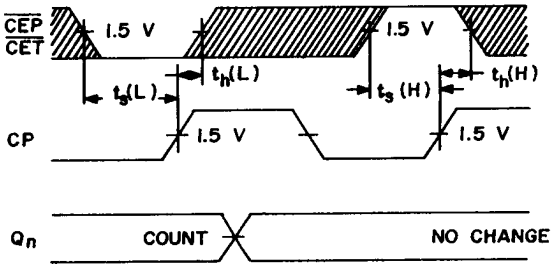
PROPAGATION DELAYS $\overline{CET}$ INPUT TO TERMINAL COUNT OUTPUT



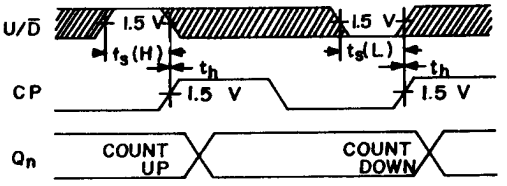
PROPAGATION DELAYS U/$\overline{D}$ CONTROL TO TERMINAL COUNT OUTPUT



PARALLEL DATA AND PARALLEL ENABLE SETUP AND HOLD TIMES



COUNT ENABLE SETUP AND HOLD TIMES



UP/DOWN CONTROL SETUP AND HOLD TIMES

SEE NOTES ON NEXT PAGE

FIGURE 5. Test circuit and switching waveforms.

Notes:

1. C_L = Load capacitance includes jig and probe capacitance.

2. R_T = Termination resistance should be equivalent to Z_{OUT} of pulse generators.

3. V_X = Unlocked pins must be held at $\leq$ 0.8 V, $\geq$ 2.7 V or open per function table.

4. All input pulses have the following characteristics: PRR $\leq$ 1 MHz, duty cycle = 50%, tr = tf = 2.5 ns ±1 ns.

3.2.6 Case outlines. The case outlines shall be in accordance with 1.2.2 herein.

3.3 Electrical performance characteristics. Unless otherwise specified, the electrical performance characteristics are as specified in table I and apply over the full case operating temperature range.

3.4 Marking. Marking shall be in accordance with MIL-STD-883 (see 3.1 herein). The part shall be marked with the part number listed in 1.2 herein. In addition, the manufacturer's part number may also be marked as listed in 6.4 herein.

3.5 Certificate of compliance. A certificate of compliance shall be required from a manufacturer in order to be listed as an approved source of supply in 6.4. The certificate of compliance submitted to DESC-ECS prior to listing as an approved source of supply shall state that the manufacturer's product meets the requirements of MIL-STD-883 (see 3.1 herein) and the requirements herein.

3.6 Certificate of conformance. A certificate of conformance as required in MIL-STD-883 (see 3.1 herein) shall be provided with each lot of microcircuits delivered to this drawing.

3.7 Notification of change. Notification of change to DESC-ECS shall be required in accordance with MIL-STD-883 (see 3.1 herein).

3.8 Verification and review. DESC, DESC's agent, and the acquiring activity retain the option to review the manufacturer's facility and applicable required documentation. Offshore documentation shall be made available onshore at the option of the reviewer.

4. QUALITY ASSURANCE PROVISIONS

4.1 Sampling and inspection. Sampling and inspection procedures shall be in accordance with section 4 of MIL-M-38510 to the extent specified in MIL-STD-883 (see 3.1 herein).

4.2 Screening. Screening shall be in accordance with method 5004 of MIL-STD-883, and shall be conducted on all devices prior to quality conformance inspection. The following additional criteria shall apply:

a. Burn-in test, method 1015 of MIL-STD-883.

(1) Test condition A, B, C, or D using the circuit submitted with the certificate of compliance (see 3.5 herein).

(2) T_A = +125°C, minimum.

b. Interim and final electrical test parameters shall be as specified in table II herein, except interim electrical parameter tests prior to burn-in are optional at the discretion of the manufacturer.

4.3 Quality conformance inspection. Quality conformance inspection shall be in accordance with method 5005 of MIL-STD-883 including groups A, B, C, and D inspections. The following additional criteria shall apply:

4.3.1 Group A inspection.

a. Tests shall be as specified in table II herein.

b. Subgroups 4, 5, and 6 in table I, method 5005 of MIL-STD-883 shall be omitted.

c. Subgroup 7 and 8 tests shall verify the truth table as specified on figure 2.

4.3.2 Groups C and D inspections.

a. End-point electrical parameters shall be as specified in table II herein.

b. Steady-state life test conditions method 1005 of MIL-STD-883:

(1) Test condition A, B, C, or D using the circuit submitted with the certificate of compliance (see 3.5 herein).

(2) T_A = +125°C, minimum.

(3) Test duration: 1,000 hours, except as permitted by method 1005 of MIL-STD-883.

TABLE II. Electrical test requirements.

MIL-STD-883 test requirements	Subgroups (per method 5005, table I)
Interim electrical parameters (method 5004)	---
Final electrical test parameters (method 5004)	1*,2,3,7,8,9
Group A test requirements (method 5005)	1,2,3,7,8,9, 10, 11
Groups C and D end-point electrical parameters (method 5005)	1, 2, 3

* PDA applies to subgroup 1.

5. PACKAGING

5.1 Packaging requirements. The requirements for packaging shall be in accordance with MIL-M-38510.

6. NOTES

6.1 Intended use. Microcircuits conforming to this drawing are intended for use when military specifications do not exist and qualified military devices that will perform the required function are not available for OEM application. When a military specification exists and the product covered by this drawing has been qualified for listing on QPL-38510, the device specified herein will be inactivated and will not be used for new design. The QPL-38510 product shall be the preferred item for all applications.

6.2 Replaceability. Microcircuits covered by this drawing will replace the same generic device covered by a contractor-prepared specification or drawing.

6.3 Comments. Comments on this drawing should be directed to DESC-ECS, Dayton, Ohio 45444, or telephone 513-296-5375.

6.4 Approved sources of supply. Approved sources of supply are listed herein. Additional sources will be added as they become available. The vendors listed herein have agreed to this drawing and a certificate of compliance (see 3.5 herein) has been submitted to DESC-ECS.

Military drawing part number	Vendor CAGE number	Vendor similar part number 1/
5962-8607201EX	18324 27014	54F169/BEA 54F169DMQB
5962-8607201FX	18324 27014	54F169/BFA 54F169FMQB
5962-86072012X	18324 27014	54F169/B2A 54F169LMQB

1/ Caution. Do not use this number for item acquisition. Items acquired to this number may not satisfy the performance requirements of this drawing.

Vendor CAGE number	Vendor name and address
18324	Signetics Corporation 4130 S. Market Court Sacramento, CA 95834
27014	National Semiconductor Corporation 333 Western Avenue South Portland, ME 04106