REVISIONS			
LTR	DESCRIPTION	DATE (YR-MO-DA)	APPROVED
A	Correct typing errors in truth table and table I. Reword paragraph 4.3.1c. Update vendors part numbers.	1987 July 13	M. A. Frye
B	Add one vendor, CAGE 18324 and their part numbers. Add programming procedure and waveforms for circuit B.	1988 May 17	M. A. Frye
C	Change vendor similar part numbers from 82523B/BEA and 82523B/BFA to 82S123B/BEA and 82S123B/BFA respectively. Table I changed V_{OL} max limit from .45 volt to 0.5 volt and I_{OS} max limit from -90 mA to -100 mA. Editorial changes throughout.	1989 JAN 12	M. A. Frye

REV																								
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REV STATUS OF SHEETS	REV	C	C	C	C	C			A		C	C	C	C	C	C	C	C	C					
	SHEET	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18					

PMIC N/A

STANDARDIZED MILITARY DRAWING

THIS DRAWING IS AVAILABLE FOR USE BY ALL DEPARTMENTS AND AGENCIES OF THE DEPARTMENT OF DEFENSE

AMSC N/A

PREPARED BY: Steve Duncan

CHECKED BY: Ray Monnin

APPROVED BY: M. A. Frye

DRAWING APPROVAL DATE: 1986 July 17

REVISION LEVEL: C

DEFENSE ELECTRONICS SUPPLY CENTER
DAYTON, OHIO 45444

MICROCIRCUITS, MEMORY, DIGITAL,
32 X 8-BIT PROM, MONOLITHIC SILICON

SIZE	CAGE CODE	
A	67268	5962-86703

SHEET 1 OF 18

DESC FORM 193
SEP 87

* U.S. GOVERNMENT PRINTING OFFICE: 1987 — 748-129/60911

5962-E1129

DISTRIBUTION STATEMENT A. Approved for public release; distribution is unlimited.

1. SCOPE

1.1 Scope. This drawing describes device requirements for class B microcircuits in accordance with 1.2.1 of MIL-STD-883, "Provisions for the use of MIL-STD-883 in conjunction with compliant non-JAN devices".

1.2 Part number. The complete part number shall be as shown in the following example:

5962-86703	01	E	X
Drawing number	Device type (1.2.1)	Case outline (1.2.2)	Lead finish per MIL-M-38510

1.2.1 Device types. The device types shall identify the circuit function as follows:

Device type	Generic number	Circuit function	Access time
01	See 6.4	32 X 8-bit PROM, T. S.	50 ns
02	See 6.4	32 X 8-bit PROM, T. S.	35 ns

1.2.2 Case outlines. The case outlines shall be as designated in appendix C of MIL-M-38510, and as follows:

Outline letter	Case outline
E	D-2 (16 lead, .840" x .310" x .200"), dual-in-line package
F	F-5 (16 lead, .440" x .285" x .085"), flat package
2	C-2 (20 terminal, .358" x .358" x .100"), square chip carrier package

1.3 Absolute maximum ratings.

Supply voltage range	-0.5 V dc to +7.0 V dc
Input voltage range	-0.5 V dc to +5.5 V dc
Storage temperature range	-65°C to +150°C
Maximum power dissipation (P_D) 1/	633 mW
Lead temperature (soldering, 10 seconds)	+300°C
Thermal resistance, junction-to-case (θ_{JC}): Cases E, F, and 2	See MIL-M-38510, appendix C
DC voltage applied to outputs (except during programming)	-0.5 V dc to +V_{CC} maximum
DC voltage applied to outputs during programming	21 V dc
Output current into outputs during programming (maximum duration of 1 second)	250 mA
DC input current	-30 mA to +5 mA

1.4 Recommended operating conditions.

Supply voltage range (V_{CC})	4.5 V dc minimum to 5.5 V dc maximum
Minimum high level input voltage (V_{IH})	2.0 V dc
Maximum low level input voltage (V_{IL})	0.8 V dc
Case operating temperature range (T_C)	-55°C to +125°C

1/ Must withstand the added P_D due to short circuit test; e.g., I_{OS}.

2. APPLICABLE DOCUMENTS

2.1 Government specification and standard. Unless otherwise specified, the following specification and standard, of the issue listed in that issue of the Department of Defense Index of Specifications and Standards specified in the solicitation, form a part of this drawing to the extent specified herein.

SPECIFICATION

MILITARY

MIL-M-38510 - Microcircuits, General Specification for.

STANDARD

MILITARY

MIL-STD-883 - Test Methods and Procedures for Microelectronics.

(Copies of the specification and standard required by manufacturers in connection with specific acquisition functions should be obtained from the contracting activity or as directed by the contracting activity.)

2.2 Order of precedence. In the event of a conflict between the text of this drawing and the references cited herein, the text of this drawing shall take precedence.

3. REQUIREMENTS

3.1 Item requirements. The individual item requirements shall be in accordance with 1.2.1 of MIL-STD-883, "Provisions for the use of MIL-STD-883 in conjunction with compliant non-JAN devices" and as specified herein.

3.2 Design, construction, and physical dimensions. The design, construction, and physical dimensions shall be as specified in MIL-M-38510 and herein.

3.2.1 Logic diagram. The logic diagram shall be as specified on figure 1.

3.2.2 Terminal connections. The terminal connections shall be as specified on figure 2.

3.2.3 Truth table. The truth table shall be as specified on figure 3.

3.2.4 Case outlines. The case outlines shall be in accordance with 1.2.2 herein.

3.2.4.1 Unprogrammed devices. The truth table for unprogrammed devices for contracts involving no altered item drawing shall be as specified on figure 3. When required in groups A, B, or C inspection (see 4.4 and 4.5), the devices shall be programmed by the manufacturer prior to test in a checkerboard pattern (a minimum of 50 percent of the total number of bits programmed) or to any altered item drawing pattern which includes at least 25 percent of the total number of bits programmed.

3.2.4.2 Programmed devices. The truth table for programmed devices shall be as specified by an altered item drawing.

3.3 Electrical performance characteristics. Unless otherwise specified, the electrical performance characteristics are as specified in table I and apply over the full case operating temperature range.

3.4 Marking. Marking shall be in accordance with MIL-STD-883 (see 3.1 herein). The part shall be marked with the part number listed in 1.2 herein. In addition, the manufacturer's part number may also be marked as listed in 6.4 herein.

TABLE I. Electrical performance characteristics.

Test	Symbol	Conditions $-55°C \le T_C \le +125°C$, $4.5\ V \le V_{CC} \le 5.5\ V$ unless otherwise specified	Group A subgroups	Device types	Limits Min	Limits Max	Unit
Output high voltage 1/	V_{OH}	V_{CC} = min, I_{OH} = -2.0 mA, V_{IN} = V_{IH} or V_{IL}	1,2,3	All	2.4		V
Output low voltage 1/	V_{OL}	V_{CC} = min, I_{OL} = 16 mA, V_{IN} = V_{IH} or V_{IL}	1,2,3	All		0.5	V
Input high level 1/	V_{IH}	Guaranteed input logical high voltage for all inputs	1,2,3	All	2.0		V
Input low level 1/	V_{IL}	Guaranteed input logical low voltage for all inputs	1,2,3	All		0.8	V
Input low current	I_{IL}	V_{CC} = max, V_{IN} = 0.45 V	1,2,3	All		-250	µA
Input high current	I_{IH}	V_{CC} = max, V_{IN} = 2.7 V	1,2,3	All		25	µA
Output short circuit current	I_{OS}	V_{CC} = max, V_{OUT} = 0.0 V 2/	1,2,3	All	-20	-100	mA
Power supply current	I_{CC}	All inputs = GND, V_{CC} = max	1,2,3	All		115	mA
Input clamp voltage 1/	V_I	V_{CC} = min, I_{IN} = -18 mA	1,2,3	All		-1.2	V
Output leakage current	I_{CEX}	V_{CC} = max, V_{CS} = 2.4 V; V_O = 4.5 V	1,2,3	All		40	µA
		V_O = 2.4 V				40	
		V_O = 0.4 V				-40	
Address access time	t_{AA}	See figures 4 and 5 3/	9,10,11	01		50	ns
				02		35	
Enable access time	t_{EA}	See figures 4 and 5 4/	9,10,11	01		30	ns
				02		25	

See footnotes at end of table.

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TABLE I. Electrical performance characteristics - Continued.

Test	Symbol	Conditions $-55°C \le T_C \le +125°C$, $4.5\ V \le V_{CC} \le 5.5\ V$ unless otherwise specified	Group A subgroups	Device types	Limits		Unit
					Min	Max	
Enable recovery time	t_{ER}	See figures 4 and 5 4/	9,10,11	01		30	ns
				02		25	

1/ These are absolute voltages with respect to device ground pin and include all overshoots due to system or tester noise or both. Do not attempt to test these values without suitable equipment.

2/ Not more than one output should be shorted at a time. Duration of the short circuit should not be more than 1 second.

3/ Parameter t_{AA} is tested with switch S1 closed and C_L = 30 pF.

4/ Parameter t_{EA} is tested with C_L = 30 pF to the 1.5 V; S1 is open for high impedance to high tests and closed for high impedance to low tests. Parameter t_{ER} is tested with C_L = 5 pF. High to high impedance tests are made with S1 open to an output voltage of V_{OH} -0.5 V. Low to high impedance tests are made with S1 closed to the V_{OL} +0.5 V level.

3.5 Processing options. Since the PROM is an unprogrammed memory capable of being programmed by either the manufacturer or the user to result in a wide variety of PROM configurations, two processing options are provided for selection in the contract, using an altered item drawing.

3.5.1 Unprogrammed PROM delivered to the user. All testing shall be verified through group A testing as defined in 3.2.4.1, tables II and III. It is recommended that users perform subgroups 7 and 9 after programming to verify the specific program configuration.

3.5.2 Manufacturer-programmed PROM delivered to the user. All testing requirements and quality assurance provisions herein, including the requirements of the altered item drawing shall be satisfied by the manufacturer prior to delivery.

3.6 Certificate of compliance. A certificate of compliance shall be required from a manufacturer in order to be listed as an approved source of supply in 6.4. The certificate of compliance submitted to DESC-ECS prior to listing as an approved source of supply shall state that the manufacturer's product meets the requirements of MIL-STD-883 (see 3.1 herein) and the requirements herein.

3.7 Certificate of conformance. A certificate of conformance as required in MIL-STD-883 (see 3.1 herein) shall be provided with each lot of microcircuits delivered to this drawing.

3.8 Notification of change. Notification of change to DESC-ECS shall be required in accordance with MIL-STD-883 (see 3.1 herein).

3.9 Verification and review. DESC, DESC's agent, and the acquiring activity retain the option to review the manufacturer's facility and applicable required documentation. Offshore documentation shall be made available onshore at the option of the reviewer.

4. QUALITY ASSURANCE PROVISIONS

4.1 Sampling and inspection. Sampling and inspection procedures shall be in accordance with section 4 of MIL-M-38510 to the extent specified in MIL-STD-883 (see 3.1 herein).

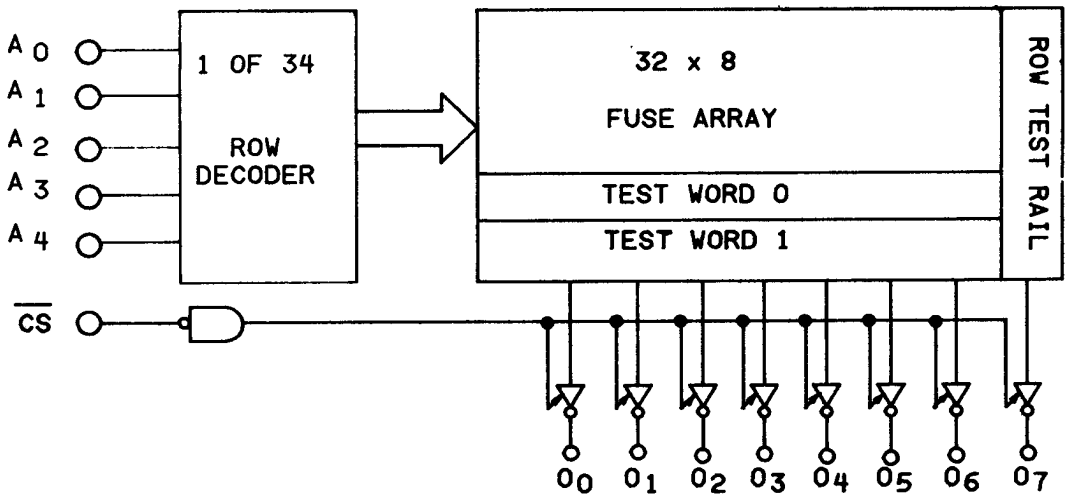
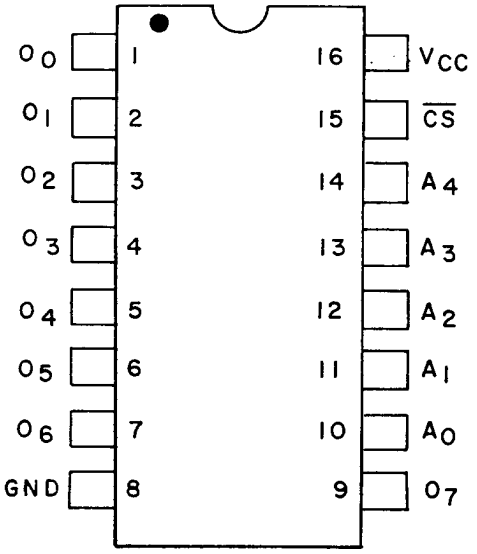
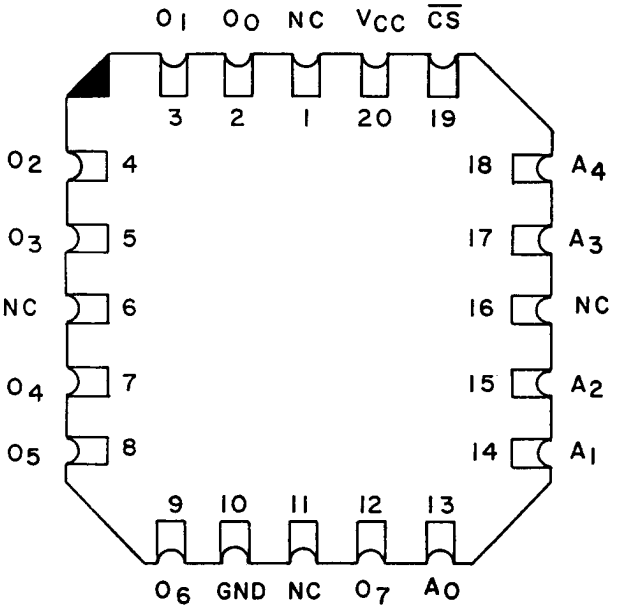


FIGURE 1. Logic diagram.

Cases E and F



Case 2



Note: Pin 1 is marked for orientation

FIGURE 2. Terminal connections.

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		REVISION LEVEL	SHEET 7

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Word No.	$\overline{CS}$	ADDRESS					DATA							
		A_4	A_3	A_2	A_1	A_0	O_7	O_6	O_5	O_4	O_3	O_2	O_1	O_0
NA	L	X	X	X	X	X	5/ OC	5/ OC	5/ OC	5/ OC	5/ OC	5/ OC	5/ OC	5/ OC
	H	X	X	X	X	X								

NOTES:

1. NA = Not applicable.
2. X = Input may be high level, low level or open circuit.
3. OC = Open circuit (high resistance output).
4. Program readout can only be accomplished with enable input at low level.
5. The outputs for an unprogrammed device shall be low.

FIGURE 3. Truth table.

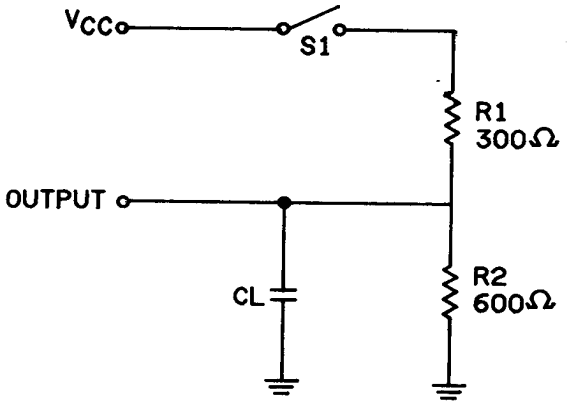

FIGURE 4. Switching test circuit.

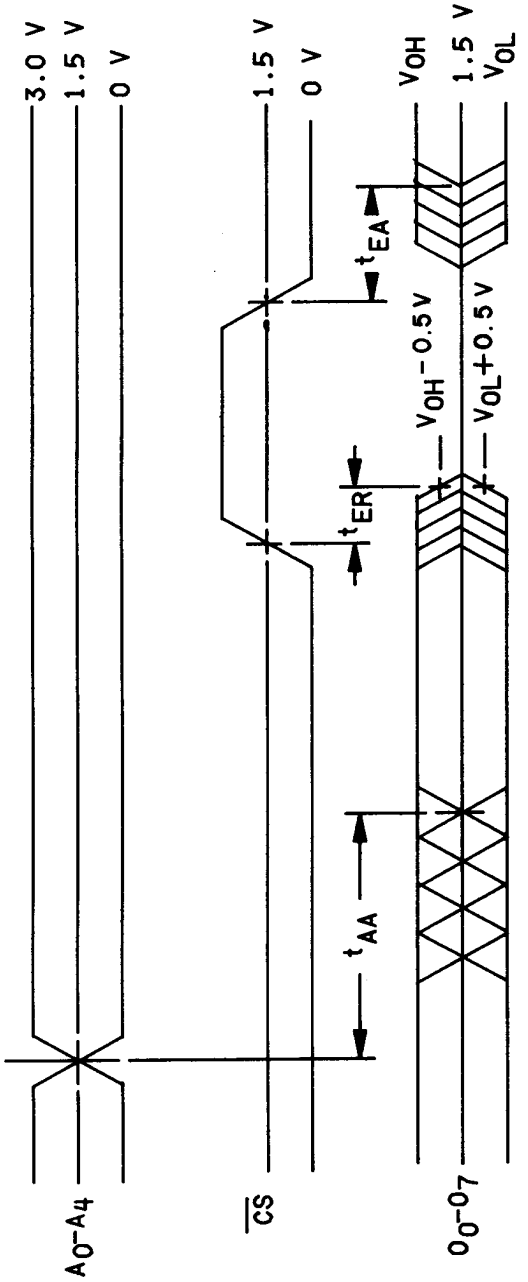

FIGURE 5. Switching waveforms.

4.2 Screening. Screening shall be in accordance with method 5004 of MIL-STD-883, and shall be conducted on all devices prior to quality conformance inspection. The following additional criteria shall apply:

a. Burn-in test, method 1015 of MIL-STD-883.

(1) Test condition C or D using the circuit submitted with the certificate of compliance (see 3.6 herein).

(2) T_A = +125°C, minimum.

b. Interim and final electrical test parameters shall be as specified in table II herein, except interim electrical parameter tests prior to burn-in are optional at the discretion of the manufacturer.

c. All devices processed to altered item drawing may be programmed either before or after burn-in at the manufacturer's discretion. The required electrical testing shall include, as a minimum, the final electrical tests for programmed devices as specified in table II.

4.3 Quality conformance inspection. Quality conformance inspection shall be in accordance with method 5005 of MIL-STD-883 including groups A, B, C, and D inspections. The following additional criteria shall apply.

TABLE II. Electrical test requirements.

MIL-STD-883 test requirements	Subgroups (per method 5005, table I)
Interim electrical parameters (method 5004)	---
Final electrical test parameters (method 5004)	1*, 2, 3, 7*, 8, 9, 10**, 11**
Group A test requirements (method 5005)	1, 2, 3, 7, 8, 9, 10**, 11**
Groups C and D end-point electrical parameters (method 5005)	1, 2, 3

* PDA applies to subgroups 1 and 7.
**Subgroups 10 and 11, if not tested, shall be guaranteed to the specified limits in table I.

4.3.1 Group A inspection.

a. Tests shall be as specified in table II herein.

b. Subgroups 4, 5, and 6 in table I, method 5005 of MIL-STD-883 shall be omitted.

c. Unprogrammed devices shall be tested for programmability and ac performance compliance to the requirements of group A, subgroups 9, 10, and 11. Either of two techniques is acceptable:

1. Testing the entire lot using additional built-in test circuitry which allows the manufacturer to verify programmability and ac performance without programming the user array. If this is done, the resulting test patterns shall be verified on all devices during subgroups 9, 10, and 11, group A testing in accordance with the sampling plan specified in MIL-STD-883, method 5005.

2. If such compliance cannot be tested on an unprogrammed device, a sample shall be selected to satisfy programmability requirements prior to performing subgroups 9, 10, and 11. Twelve devices shall be submitted to programming (see 3.2.4.1). If more than two devices fail to program, the lot shall be rejected. At the manufacturer's option, the sample may be increased to 24 total devices with no more than 4 total device failures allowable. Ten devices from the programmability sample shall be submitted to the requirements of group A, subgroups 9, 10, and 11. If more than two total devices fail, the lot shall be rejected. At the manufacturer's option, the sample may be increased to 20 total devices with no more than 4 total device failures allowable.

4.3.2 Groups C and D inspections.

a. End-point electrical parameters shall be as specified in table II herein.

b. Steady-state life test conditions, method 1005 of MIL-STD-883.

(1) Test condition C or D using the circuit submitted with the certificate of compliance (see 3.6 herein).

(2) T_A = +125°C, minimum.

(3) Test duration: 1,000 hours, except as permitted by method 1005 of MIL-STD-883.

c. The group C, subgroup 1 sample shall include devices tested in accordance with 4.3.1c.

4.4 Programming procedure for circuit A. The programming characteristics in table IIIA and the following procedures shall be used for programming the device.

a. Connect the device in the electrical configuration for programming. The waveforms of figure 6 and the programming characteristics in table IIIA shall apply to these procedures.

b. Terminate all outputs with a 300Ω resistor to V_{ONP}. Apply V_{IHP} to the $\overline{CS}$ input.

c. Address the PROM with the binary address of the selected word to be programmed. V_{CC} is to be at V_{CCP}.

d. After a delay of t_1, apply one V_{OP} pulse noting $d(V_{OP})/dt$. After a delay of t_2, raise $\overline{CS}$ to V_{CSP} at $d(V_{CS})/dt$. Wait t_p and then remove the V_{OP} supply. Wait t_3 before lowering $\overline{CS}$ to V_{ILP}.

e. To verify programming after $\overline{CS}$ has established V_{ILP}, lower V_{CC} to V_{CCL} for a period of t_4. The output programmed should remain a logic 1.

f. The outputs should be programmed one at a time, since the internal decoding circuitry is capable of sinking only one unit of programming current at a time. Note that the PROM is supplied with fuses generating a low level logic output prior to programming. Programming a fuse will cause the output to go to a high level logic in the verify mode.

g. Repeat steps 4.4b through 4.4f for all other bits to be programmed.

4.5 Programming procedures for circuit B. The programming characteristics in table IIIB and the following procedures shall be used for programming the devices.

a. Connect the device in the electrical configuration for programming. The waveforms on figure 6 and the programming characteristics in table IIIB shall apply to these procedures.

b. Terminate all output pins with a 10 kΩ resistor to V_{CC}.

c. Bypass V_{CC} to ground with a 0.01 μF capacitor.

d. Apply initial voltage of V_{IH} to the programming control pin ($\overline{CS}$), and appropriate voltage to chip select pins (as applicable) in accordance with table I.

e. Apply 0 volts to all other pins.

f. Select the word to be programmed by applying V_{IL} or V_{IH} to the appropriate address pins.

g. Wait the delay shown in table IIIB for t_{D1}, and then raise the V_{CC} pin to V_{CCP}.

h. Wait the delay shown in table IIIB for t_{D2}, and then raise the corresponding output pin to V_{OPF}.

i. Wait the delay shown in table IIIB for t_{D3}, and then lower the programming control pin ($\overline{CS}$) to V_{IL} for the duration of t_p.

j. Return the programming control pin to V_{IH}.

k. Wait for the delay shown in table IIIB for t_{D4}, and then lower the output to 0 volts.

l. Wait for the delay shown in table IIIB for t_{D5}, and repeat steps f through k, for each output bit desired to be a logic one.

m. Wait for the delay shown in table IIIB for t_{D6}, and apply V_{CCV} to V_{CC} pin.

n. Wait for the delay shown in table IIIB for t_{D7}, and lower $\overline{CS}$ input to V_{IL} for a duration of t_v.

o. A properly blown fuse will read V_{OH}, and unblown fuse will read V_{OL}.

p. Wait for the delay shown in table IIIB for t_{D8}, and select a new address.

q. Wait for the delay shown in table IIIB for t_{D1}, and return V_{CC} to V_{CCP}.

r. Repeat steps f through q, until all required addresses are programmed.

s. Complete address verification.

(1) Wait for the delay shown in table IIIB for t_{D7}, keeping V_{CC} at V_{CCV}.

(2) Lower $\overline{CS}$ input to V_{IL}.

(3) Sequentially select all addresses in the memory.

(4) A properly blown fuse will read V_{OH}, and unblown fuse will read V_{OL}.

5. PACKAGING

5.1 Packaging requirements. The requirements for packaging shall be in accordance with MIL-M-38510.

6. NOTES

6.1 Intended use. Microcircuits conforming to this drawing are intended for use when military specifications do not exist and qualified military devices that will perform the required function are not available for OEM application. When a military specification exists and the product covered by this drawing has been qualified for listing on QPL-38510, the device specified herein will be inactivated and will not be used for new design. The QPL-38510 product shall be the preferred item for all applications.

TABLE IIIA. Programming characteristics for circuit A.

Test	Symbol	Conditions T_C = +25°C	Limits			Unit
			Min	Recommended	Max	
V_{CC} during programming	V_{CCP}		5.0		5.5	V
High level input voltage during programming	V_{IHP}		2.4		5.5	V
Low level input voltage during programming	V_{ILP}		0.0		0.45	V
Chip select voltage during programming	V_{CSP}	$\overline{CS}$ pin	14.5		15.5	V
Output voltage during programming	V_{OP}		19.5		20.5	V
Voltage on outputs not to be programmed	V_{ONP}		0		V_{CCP} +0.3	V
Current on outputs not to be programmed	I_{ONP}				20	mA
Rate of output voltage change	$\frac{d(V_{OP})}{dt}$		20		250	V/µs
Rate of chip select voltage change	$\frac{d(V_{CS})}{dt}$	$\overline{CS}$ pin	100		1000	V/µs
Programming period	t_p		50		100	µs
V_{CC} during programming verification	V_{CCL}		4.5		5.0	µs

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TABLE IIIB. Programming characteristics for circuit B.

Test	Symbol	Conditions	Limits			Unit
			Min	Recommended	Max	
Power supply voltage to program 1/	V_{CCP}	I_{CCP} = 425	8.5	8.75	9.0	V
Verify voltage	V_{CCV}		4.75	5.0	5.25	V
High input voltage	V_{IH}	I_{IH} = 50 µA	2.4	3.0	5.5	V
Low input voltage	V_{IL}	I_{IL} = -500 µA	0	0	0.5	V
Forced output voltage (program) 2/ 3/	V_{OPF}	I_{OPF} = 300	17.0	17.5	18.0	V
Output high voltage	V_{OH}		2.4		5.25	V
Output low voltage	V_{OL}		0		0.45	V
Delay time	t_{D1}	50% add to 10% V_{CCP}	10	10	25	µs
Delay time	t_{D2}	90% V_{CCP} to 10% V_{OPF}	1	1	5	µs
Pulse sequence delays	t_{D3}-t_{D8}	See figure 6	1	1	10	µs
Rise time	t_{R1}	10% to 90%	2	7	20	µs
Rise time	t_{R2}	10% to 90%	17	20	35	µs
Fall time	t_{F1}	90% to 10%	1	4	10	µs
Fall time	t_{F2}	90% to 10%	2	7	20	µs

See footnotes at end of table.

TABLE IIIB. Programming characteristics for circuit B - Continued.

Test	Symbol	Conditions	Limits			Unit
			Min	Recommended	Max	
Programming pulse width 4/ 5/	t_p	10% to 10%	10	10	25	µs
Verify pulse width 4/ 5/	t_v	10% to 10%	5	5	10	µs

NOTES:

1/ If the overall program/verify cycle exceeds the recommended times, a 25% duty cycle must be used for V_{CCP}.

2/ V_{OPF} supply should regulate to ±0.25 V at I_{OPF}.

3/ Maximum slew rate for V_{OPF} should be 1.0 V/µs.

4/ $\overline{CS}$ rise time slew rate should be 1.0 V/ns maximum.

5/ $\overline{CS}$ fall time slew rate should be 10.0 V/ns maximum.

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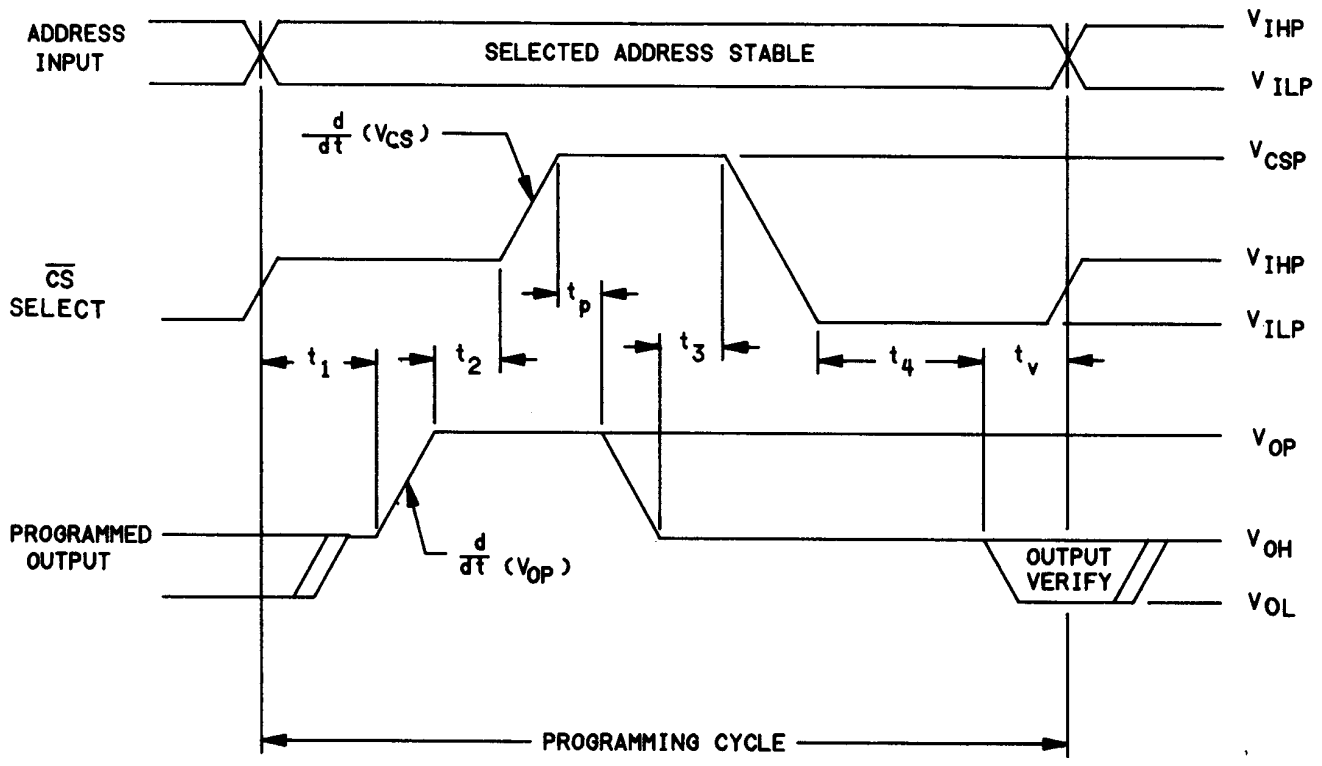
CIRCUIT A



NOTES:
1. All delays between edges are specified from completion of the first edge, not midpoints.
2. Delays t_1, t_2, t_3, and t_4 must be greater than 100 ns; maximum delays of 1 µs are recommended to minimize heating during programming.
3. During t_V the output being programmed is switched to the load R and verified.
4. Outputs not being programmed are connected to V_{ONP} through resistor which provides output current limiting.

FIGURE 6. Programming voltage waveforms during programming.

CIRCUIT B

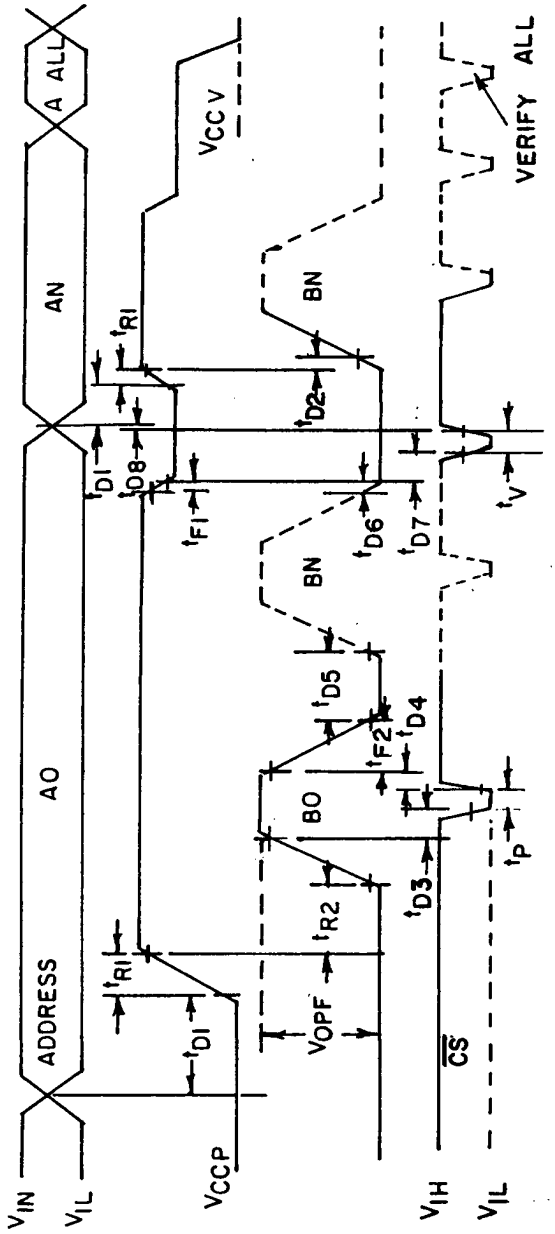


FIGURE 6. Programming voltage waveforms during programming - Continued.

6.2 Replaceability. Microcircuits covered by this drawing will replace the same generic device covered by a contractor-prepared specification or drawing.

6.3 Comments. Comments on this drawing should be directed to DESC-ECS, Dayton, Ohio 45444, or telephone 513-296-5375.

6.4 Approved sources of supply. Approved sources of supply are listed herein. Additional sources will be added as they become available. The vendors listed herein have agreed to this drawing and a certificate of compliance (see 3.6 herein) has been submitted to DESC-ECS.

Military drawing part number	Vendor CAGE number	Vendor similar part number 1/
5962-8670301EX	18324 34335	82S123A/BEA AM27S19/BEA
5962-8670301FX	18324 34335	82S123A/BFA AM27S19/BFA
5962-86703012X	34335	AM27S19/B2A
5962-8670302EX	18324 34335	82S123B/BEA AM27S19A/BEA
5962-8670302FX	18324 34335	82S123B/BFA AM27S19A/BFA
5962-86703022X	34335	AM27S19A/B2A

1/ Caution. Do not use this number for item acquisition. Items acquired to this number may not satisfy the performance requirements of this drawing.

Vendor CAGE number	Vendor name and address	Programming procedure	Fusable link
18324	Signetics, Incorporated 4130 S. Market Court Sacramento, CA 95834	B	Nichrome fuse
34335	Advanced Micro Devices, Incorporated 901 Thompson Place P.O. Box 3453 Sunnyvale, CA 94088	A	Platinum silicide fuse