040152

REVISIONS

LTR	DESCRIPTION	DATE (YR-MO-DA)	APPROVED
A	Change CAGE to 67268. Added case outline Z. Added vendor CAGE 60911 and five new device types to drawing. Dropped vendor CAGE number 34335 as source of supply. Deleted V_{CC} for data retention from recommended operating conditions, and added it to table I as I_{CC4}. Moved standard power devices for vendor CAGE number 61772 and 34649 to devices 11-15. Editorial changes throughout. Changes to table I, and correction in vendor similar part number for vendor 04713. Deleted subgroups 1, 2, 3 from table II.	1988 MAR 04	

CURRENT CAGE CODE 67268

REV																								
SHEET																								
REV																								
SHEET																								
REV STATUS OF SHEETS	REV	A	A	A	A	A	A	A		A	A	A	A				A	A	A	A	A			
	SHEET	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20			

PMIC N/A

STANDARDIZED MILITARY DRAWING

THIS DRAWING IS AVAILABLE FOR USE BY ALL DEPARTMENTS AND AGENCIES OF THE DEPARTMENT OF DEFENSE

AMSC N/A

PREPARED BY James E. Jamison

CHECKED BY Charles Reising

APPROVED BY

DRAWING APPROVAL DATE 5 February 1987

REVISION LEVEL A

DEFENSE ELECTRONICS SUPPLY CENTER
DAYTON, OHIO 45444

MICROCIRCUITS, DIGITAL, CMOS, 4K X 4 STATIC RAM, MONOLITHIC SILICON

SIZE	CAGE CODE	
A	14933	5962-86705

SHEET 1 OF 20

DESC FORM 193-1
SEP 87

* U.S. GOVERNMENT PRINTING OFFICE: 1987 — 748-129/60912

5962-E611

1. SCOPE

1.1 Scope. This drawing describes device requirements for class B microcircuits in accordance with 1.2.1 of MIL-STD-883, "Provisions for the use of MIL-STD-883 in conjunction with compliant non-JAN devices".

1.2 Part number. The complete part number shall be as shown in the following example:

5962-86705	01	R	X
Drawing number	Device type (1.2.1)	Case outline (1.2.2)	Lead finish per MIL-M-38510

1.2.1 Device types. The device types shall identify the circuit function as follows:

Device type	Generic number	Circuit function	Access time
01,11	(See 6.4)	4096 X 4 CMOS static RAM	25 ns
02	(See 6.4)	4096 X 4 CMOS static RAM	25 ns
03,12	(See 6.4)	4096 X 4 CMOS static RAM	35 ns
04	(See 6.4)	4096 X 4 CMOS static RAM	35 ns
05,13	(See 6.4)	4096 X 4 CMOS static RAM	45 ns
06	(See 6.4)	4096 X 4 CMOS static RAM	45 ns
07,14	(See 6.4)	4096 X 4 CMOS static RAM	55 ns
08	(See 6.4)	4096 X 4 CMOS static RAM	55 ns
09,15	(See 6.4)	4096 X 4 CMOS static RAM	70 ns
10	(See 6.4)	4096 X 4 CMOS static RAM	70 ns

1.2.2 Case outline. The case outline shall be as designated in appendix C of MIL-M-38510, and as follows:

Outline letter	Case outline
R	D-8 (20-lead, 1/4" X 1-1/16"), dual-in-line package
X	C-13 (20 terminal, 0.29" X 0.425") chip carrier package
Y	See figure 1 (20 lead, 0.39" X 0.49") flat package
Z	F-9A (20 lead, .300" X .540") flat package

1.3 Absolute maximum ratings.

Supply voltage range	-0.5 V dc to +7.0 V dc
Input voltage range	-0.3 V dc to V_{CC} + .5 V dc
Storage temperature range	-65°C to +150°C
Maximum power dissipation (P_D)	1.0 W
Lead temperature (soldering, 10 seconds)	+300°C
Thermal resistance, junction-to-case (θ_{JC}):	
Cases R, X, and Z	See MIL-M-38510, appendix C
Case Y	+3.8°C/W
Junction temperature (T_J)	+175°C
DC output current	25 mA

1.4 Recommended operating conditions.

Supply voltage (V_{CC})	4.5 V dc minimum to 5.5 V dc maximum
Minimum high-level input voltage (V_{IH})	2.4 V dc
Maximum low-level input voltage (V_{IL})	0.8 V dc
Case operating temperature range (T_C)	-55°C to +125°C
V_{CC} for data retention (V_{DR})	2.2 V dc minimum 1/

2. APPLICABLE DOCUMENTS

2.1 Government specification and standard. Unless otherwise specified, the following specification and standard, of the issue listed in that issue of the Department of Defense Index of Specifications and Standards specified in the solicitation, form a part of this drawing to the extent specified herein.

SPECIFICATION

MILITARY

MIL-M-38510 - Microcircuits, General Specification for.

STANDARD

MILITARY

MIL-STD-883 - Test Methods and Procedures for Microelectronics.

(Copies of the specification and standard required by manufacturers in connection with specific acquisition functions should be obtained from the contracting activity or as directed by the contracting activity.)

2.2 Order of precedence. In the event of a conflict between the text of this drawing and the references cited herein, the text of this drawing shall take precedence.

3. REQUIREMENTS

3.1 Item requirements. The individual item requirements shall be in accordance with 1.2.1 of MIL-STD-883, "Provisions for the use of MIL-STD-883 in conjunction with compliant non-JAN devices" and as specified herein.

3.2 Design, construction, and physical dimensions. The design, construction, and physical dimensions shall be as specified in MIL-M-38510 and herein.

3.2.1 Terminal connections. The terminal connections shall be as specified on figure 2.

3.2.2 Truth table. The truth table shall be as specified on figure 3.

3.2.3 Logic diagram. The logic diagrams shall be as specified on figure 4.

3.2.4 Case outline. The case outline shall be in accordance with 1.2.2 herein.

3.2.5 Die overcoat. Polyimide and silicon coatings are allowable as an overcoat on the die for alpha particle protection provided that each coated microcircuit inspection lot (reference MIL-M-38510, paragraph 3.1.3.8) shall be subjected to and pass the internal moisture content test (group D, subgroup 6, test method 5005 of MIL-STD-883). The frequency of the internal water vapor testing may not be decreased unless approved by the preparing activity.

3.3 Electrical performance characteristics. Unless otherwise specified, the electrical performance characteristics are as specified in table I and apply over the full recommended case operating temperature range.

1/ Applies to devices 01-10.

TABLE I. Electrical performance characteristics.

Test	Symbol	Conditions 1/ 2/ V_{SS} = 0 V, 4.5 V ≤ V_{CC} ≤ 5.5 V, -55°C ≤ T_C ≤ +125°C unless otherwise specified	Group A subgroups	Device type	Limits Min	Limits Max	Unit
Output high current	I_{OH}	V_{OH} = 2.4 V V_{CC} = 4.5 V	1,2,3	01-10 11-15	-4		mA
Output low current	I_{OL}	V_{OL} = 0.4 V	1,2,3	01-10 11-15	8		mA
Input high voltage	V_{IH}		1,2,3	01-10 11-15	2.4	6.0	V
Input low voltage 3/	V_{IL}		1,2,3	01-10 11-15	-0.5	0.8	V
Input load current	I_{IX}	GND ≤ V_I ≤ V_{CC}, V_{CC} = maximum	1,2,3	01-10 11-15	-5	5	µA
Output leakage current	I_{OZ}	GND ≤ V_O ≤ V_{CC} output disabled	1,2,3	01-10 11-15	-5 -10	5 10	µA
Input capacitance	C_I	Test frequency = 1.0 MHz V_{IN} = 0 V See 4.3.1c	4	01-10 11-15		6 4	pF
Output capacitance	C_O	T_A = 25°C, All pins at 0 V, V_{CC} = 5 V, V_{OUT} = 0 V See 4.3.1c	4	13-15 02,04 05-10 01,03,11,12		4 7 10	pF pF pF
Operating supply current	I_{CC1}	$\overline{CE}$ = V_{IL}, f = 1 MHz	1,2,3	All		120	mA
Standby power supply current (TTL)	I_{CC2}	$\overline{CE}$ = V_{IH}, V_{CC} = maximum	1,2,3	All		45	mA
Standby power supply current (CMOS)	I_{CC3}	V_{CC} +0.2 V ≥ $\overline{CE}$ ≥ V_{CC} -0.2 V outputs open V_{CC} +0.2 V ≥ V_{IN} ≥ V_{CC} -0.2 V or +0.2 ≥ V_{IN} ≥ -0.2 V	1,2,3	All		14	mA
Data retention current	I_{CC4}	V_{CC} = 2.0 V	1,2,3	01-10		1200	µA
Address valid to address do not care time (read cycle time)	t_{RC}	See figures 5, 6, and 7	9,10,11	01,02,11 03,04,12 05,06,13 07,08,14 09,10,15	25 35 45 55 70		ns
Address valid to data out valid delay (address access time)	t_{AA}		9,10,11	01,02,11 03,04,12 05,06,13 07,08,14 09,10,15		25 35 45 55 70	ns

See footnotes at end of table.

TABLE I. Electrical performance characteristics - Continued.

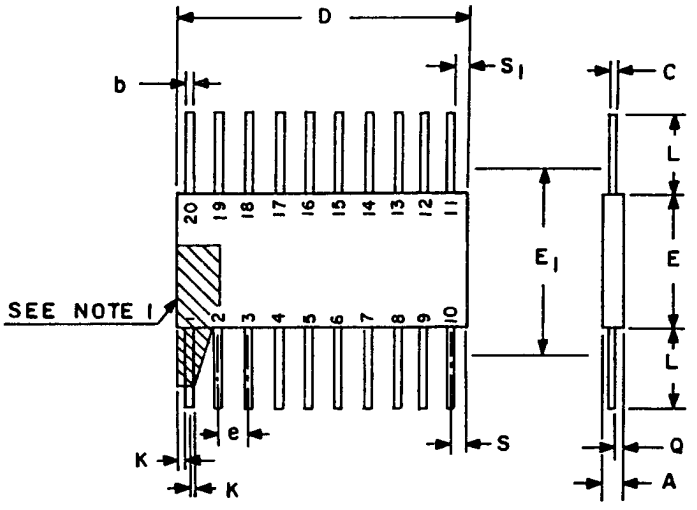
Test	Symbol	Conditions 1/ 2/ V_{SS} = 0 V, 4.5 V ≤ V_{CC} ≤ 5.5 V, -55°C ≤ T_C ≤ +125°C unless otherwise specified	Group A subgroups	Device type	Limits Min	Limits Max	Unit
Chip enable low to data out valid (chip enable access time)	t_{ACS}	See figures 5, 6, and 7	9,10,11	01,02,11		25	ns
				03,04,12		35	
				05,06,13		45	
				07,08,14		55	
				09,10,15		70	
Chip enable low to data out on 4/ 5/	t_{LZ}		9,10,11	01-10	5		ns
				11-15			
Chip enable high to data out off 4/ 5/ 6/	t_{HZ}		9,10,11	01,02,11	0	10	ns
				03,04	0	15	
				05,06, 12,13	0	20	
				07,08,14	0	25	
				09,10,15	0	30	
Address unknown to data out unknown time	t_{OH}		9,10,11	01,02,04	5		ns
				03,05-15	3		
Chip enable high to power down delay 4/	t_{PD}		9,10,11	01,02,11		25	ns
				03,04,12		35	
				05,06,13		45	
				07,08,14		55	
				09,10,15		70	
Chip enable low to power on delay 4/	t_{PU}		9,10,11	All	0		ns
Address valid to address do not care (write cycle time)	t_{WC}		9,10,11	01,02,11	25		ns
				03,04,12	35		
				05,06,13	45		
				07,08,14	55		
				09,10,15	65		
Write enable low to write enable high 7/	t_{WP}		9,10,11	01,02,11	20		ns
				03,04,12	30		
				05,06,13	30		
				07,08,14	45		
				09,10,15	65		
Write enable high to address do not care	t_{WR}		9,10,11	01-10	0		ns
				11-15	5		

See footnotes at end of table.

TABLE I. Electrical performance characteristics - Continued.

Test	Symbol	Conditions 1/ 2/ V_{SS} = 0 V, 4.5 V ≤ V_{CC} ≤ 5.5 V, -55°C ≤ T_C ≤ +125°C unless otherwise specified	Group A subgroups	Device type	Limits Min	Limits Max	Unit
Write enable low to output in high Z 4/ 5/ 6/	t_{WZ}	See figures 5, 6, and 7	9,10,11	01,02	0	7	ns
				03,11,12	0	15	
				04	0	13	
				05,06,13	0	20	
				07,08,14	0	25	
				09,10,15	0	30	
Data in valid to write enable high	t_{DW}		9,10,11	01,02,11	13		ns
				04	17		
				03,05,06, 12,13	15		
				07,08,14	25		
				09,10,15	30		
Data hold time	t_{DH}		9,10,11	All	3		ns
Address valid to write enable low	t_{AS}		9,10,11	All	0		ns
Chip enable low to write enable high 4/ 7/	t_{CW}		9,10,11	01,02,11	20		ns
				03,04,12	30		
				05,06,13	35		
				07,08,14	45		
				09,10,15	60		
Write enable high to output in low Z 4/ 5/	t_{OW}		9,10,11	All	0		ns
Address valid to end of write	t_{AW}		9,10,11	01,02,11	20		ns
				03,04,12	30		
				05,06,13	35		
				07,08,14	40		
				09,10,15	60		

1/ Test conditions assume signal transition times of 10 ns or less, timing reference levels of 1.5 V, input pulse levels of 0 to 3.0 V and output loading of the specified I_{OL}/I_{OH} and 30 pF load capacitance. Output timing reference is 1.5 V.
2/ For test and correlation purposes, ambient temperature is defined as the instant on case temperature.
3/ V_{IL} voltages of less than -0.5 V on the I/O pins will cause the output current to exceed the maximum rating. -1.0 V and -3.0 V pulses can be tolerated for up to 50 ns and 10 ns respectively.
4/ This parameter is not tested but is guaranteed by characterization.
5/ At any given temperature and voltage condition, t_{HZ} is less than t_{LZ} and t_{WZ} is less than t_{OW}. Transition is measured at 1.5 V on the input to V_{OH} at 1.9 V and V_{OL} at 0.9 V on the outputs using the load shown in figure 5. C_L = 5 pF.
6/ The minimum limit is not tested and is included for users guidelines only.
7/ The internal write time of the memory is defined by the overlap of $\overline{CE}$ low and $\overline{WE}$ low. Both signals must be low to initiate a write and either signal can terminate a write by going high. The data input setup and hold timing should be referenced to the rising edge of the signal that terminates the write.



Symbol	Inches		Notes	mm	
	Min	Max		Min	Max
A	.045	.092		1.14	2.34
b	.015	.019	5	0.38	0.48
c	.003	.006	5	0.08	0.15
D		.540	3	13.72	
E	.340	.396		8.64	10.06
E_1		.401	3	10.19	
E_2	.130			3.30	
E_3	.030			0.76	
e	.050	BSC	4, 6	1.27	
K	.008	.015	9	0.20	0.38
L	.250	.370		6.35	9.40
Q	.010	.040	2	0.25	1.02
S		.045	7		1.14
S_1	.005		7, 8	0.13	

NOTES:
1. Index area; a notch or a pin one identification mark shall be located adjacent to pin one and shall be within the shaded area shown. The manufacturer's identification shall not be used as a pin one identification mark. Alternatively, a tab (dim. k) may be used to identify pin one. This tab may be located on either side as shown.
2. Dimension Q shall be measured at the point of exit of the lead from the body. Dimension Q shall be .0085 (0.22 mm) minimum when lead finish A is applied.
3. This dimension allows for off-center lid, meniscus, and glass overrun.
4. The basic pin spacing is .050 (1.27 mm) between centerlines. Each pin centerline shall be located with ±.005 (0.13 mm) of its exact longitudinal position relative to pins 1 and 20.
5. All leads - Increase maximum limit by .003 (0.08 mm) measured at the center of the flat, when lead finish A or B is applied.
6. Eighteen spaces.
7. Applies to all four corners.
8. Dimensions S_1 may be .000 (0.00) if lead number 1,2,9,10,11,12, 19,and 20 bend toward the cavity of the package within one lead's width from the point of entry of the lead into the body.
9. Optional, see note 1. If a pin one identification mark is used in addition to this tab, the minimum limit of dimension k does not apply.

FIGURE 1. Case outline Y.

Case X

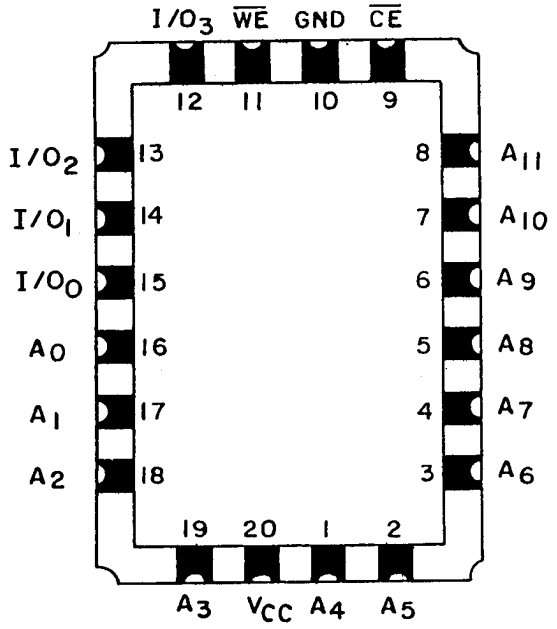
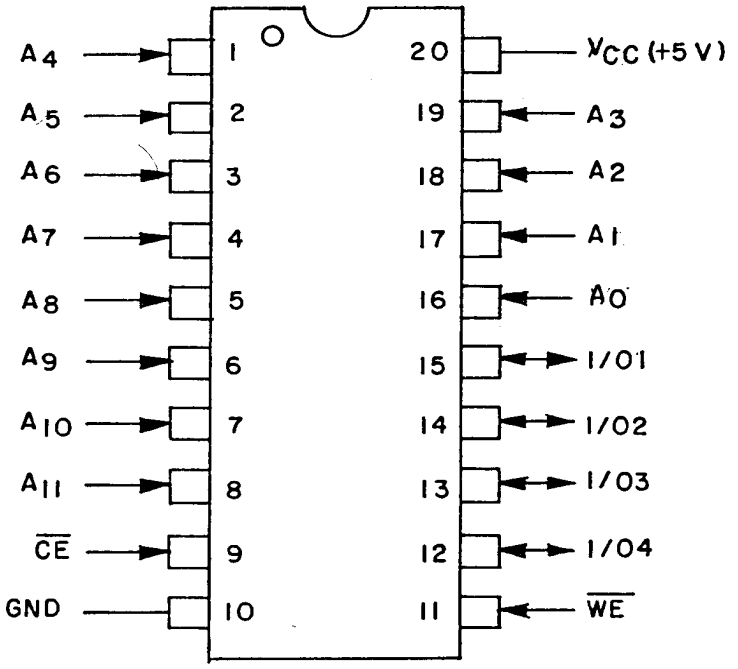


FIGURE 2. Terminal connections.

Cases R, Y and Z



Note: Pin 1 is marked for orientation.

FIGURE 2. Terminal connections - Continued.

$\overline{CE}$	$\overline{WE}$	MODE	I/O	POWER
H	X	NOT SELECTED	HIGH Z	STANDBY
L	L	WRITE	D_{IN}	ACTIVE
L	H	READ	D_{OUT}	ACTIVE

FIGURE 3. Truth table.

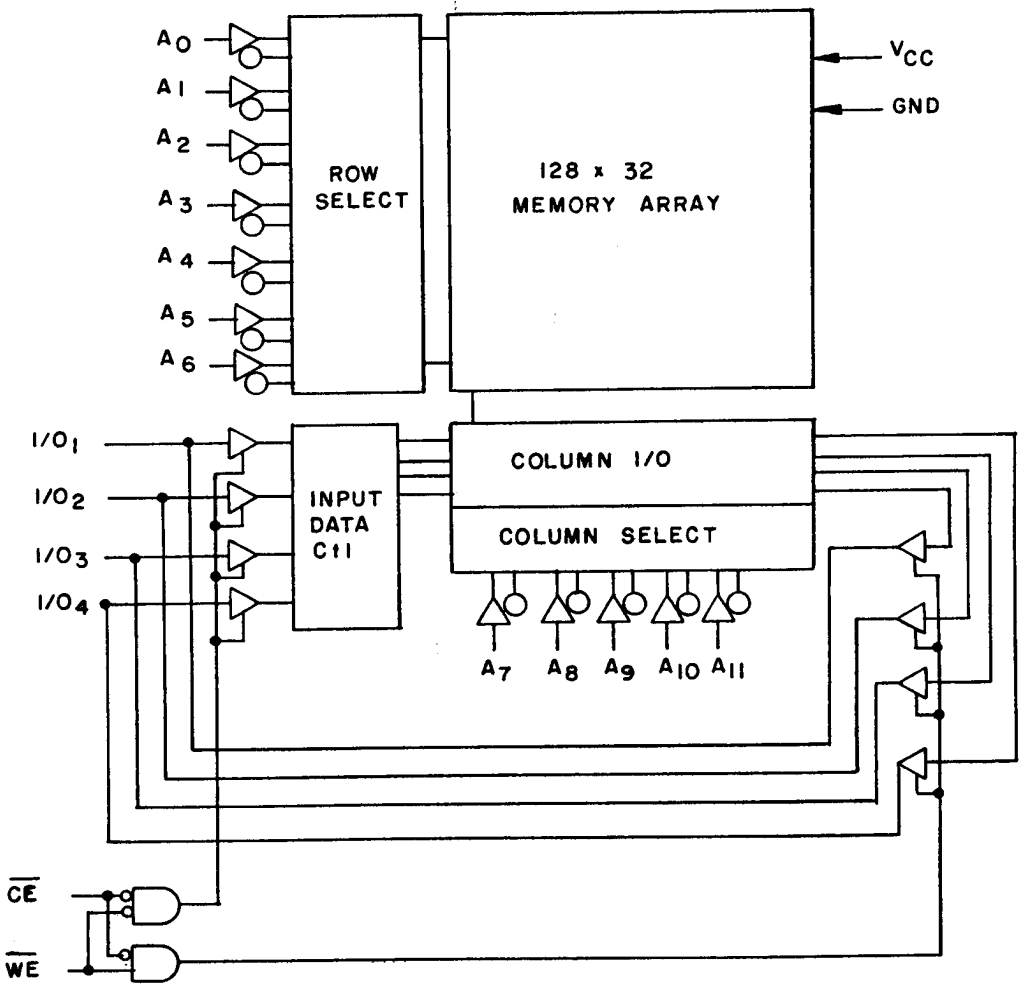
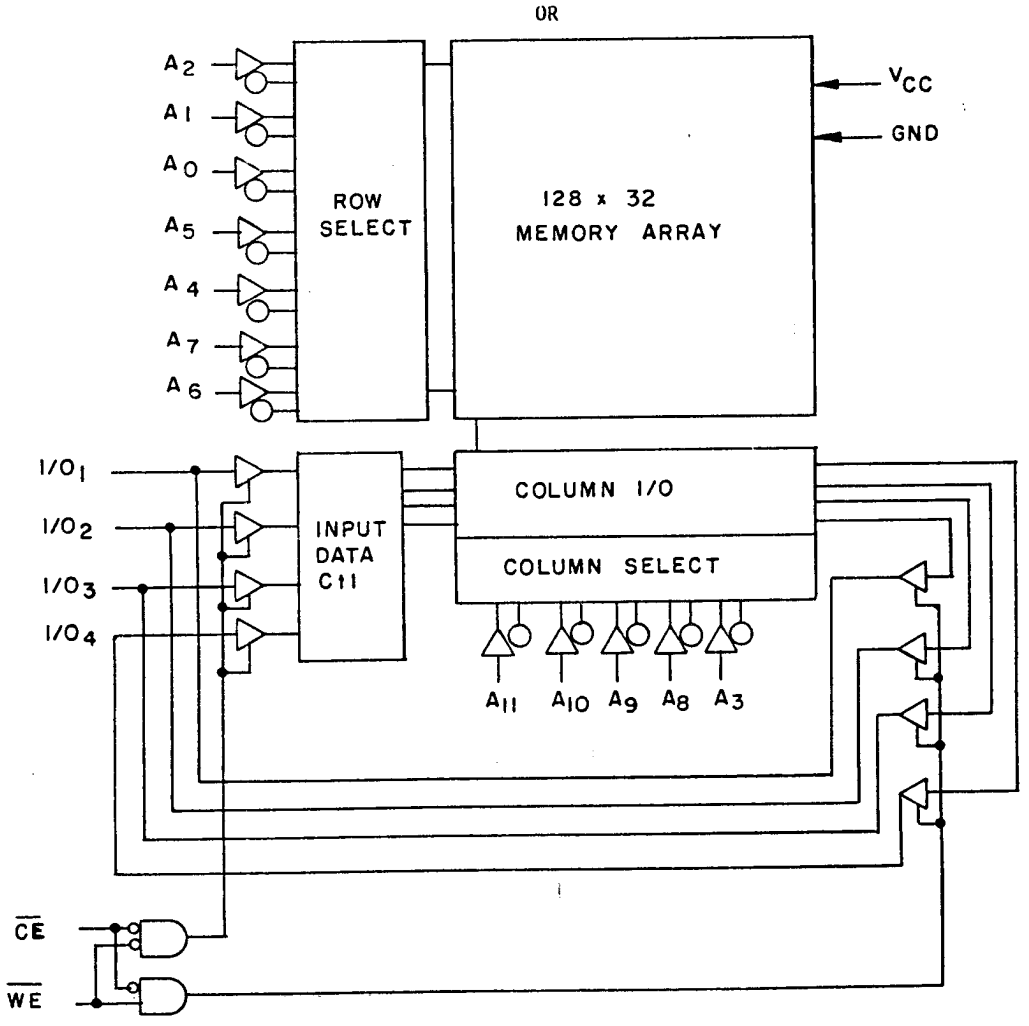


FIGURE 4. Logic diagrams.



ALTERNATE DIAGRAM

FIGURE 4. Logic diagrams - Continued.

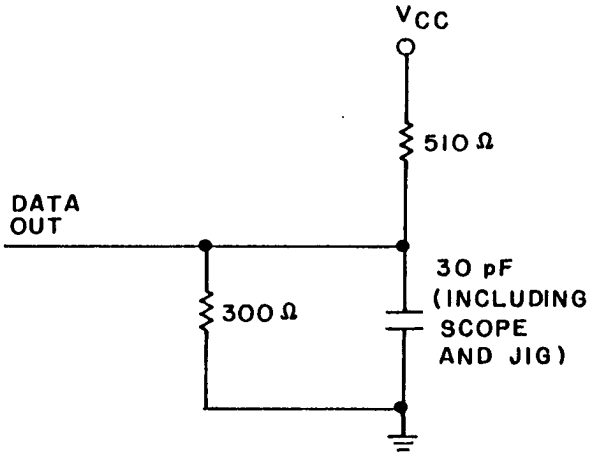


FIGURE 5. Output load.

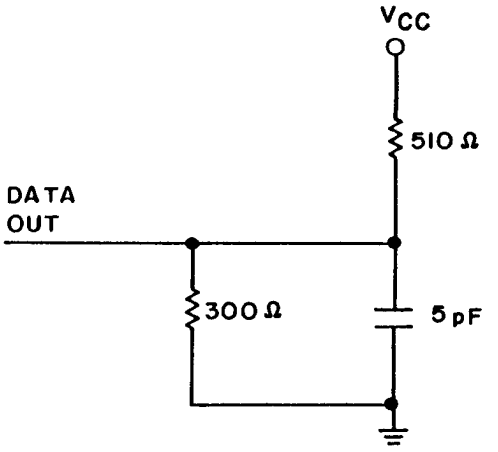
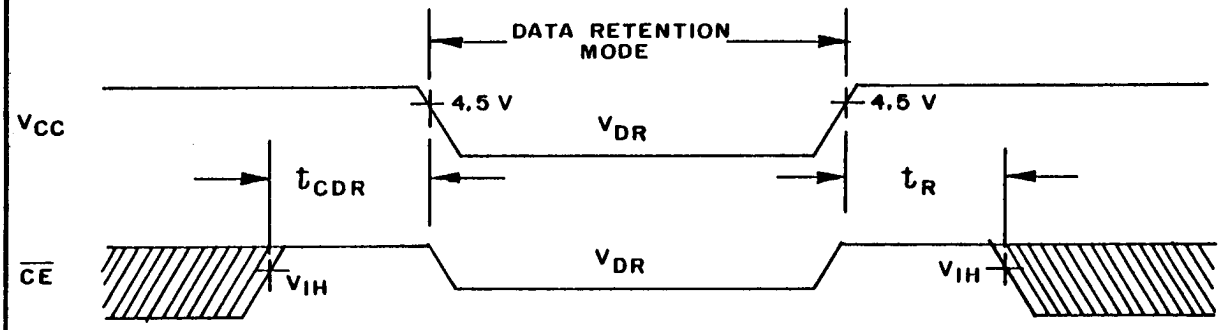


FIGURE 6. Output load for t_{HZ}, t_{LZ}, t_{OW}, t_{WZ}.

DATA RETENTION WAVEFORM



NOTES:
1. t_{CDR} = 0 ns (minimum)
   t_R = t_{RC} (minimum).
2. Waveform shown is not actual and may vary in use.

FIGURE 7. Switching waveforms.

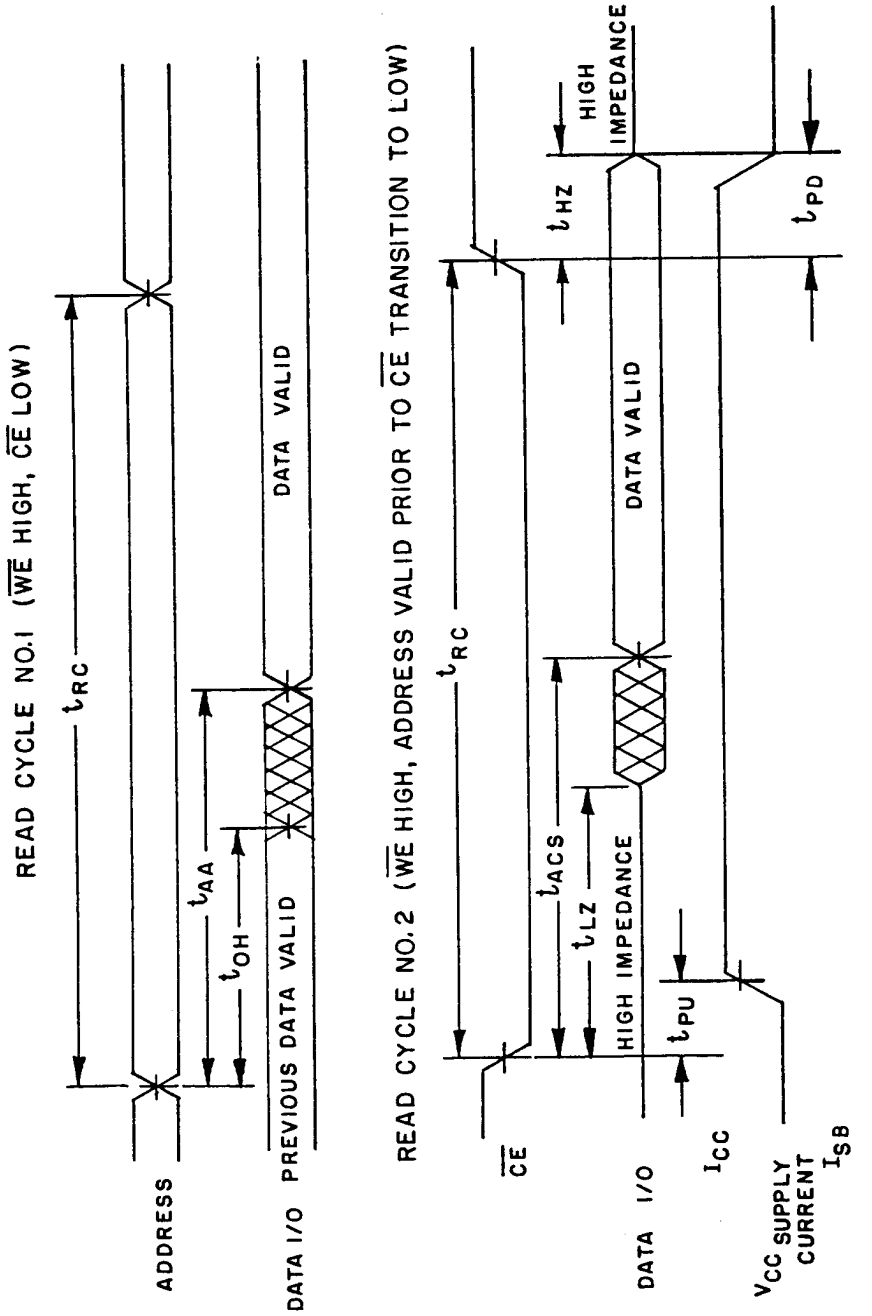


FIGURE 7. Switching waveforms - Continued.

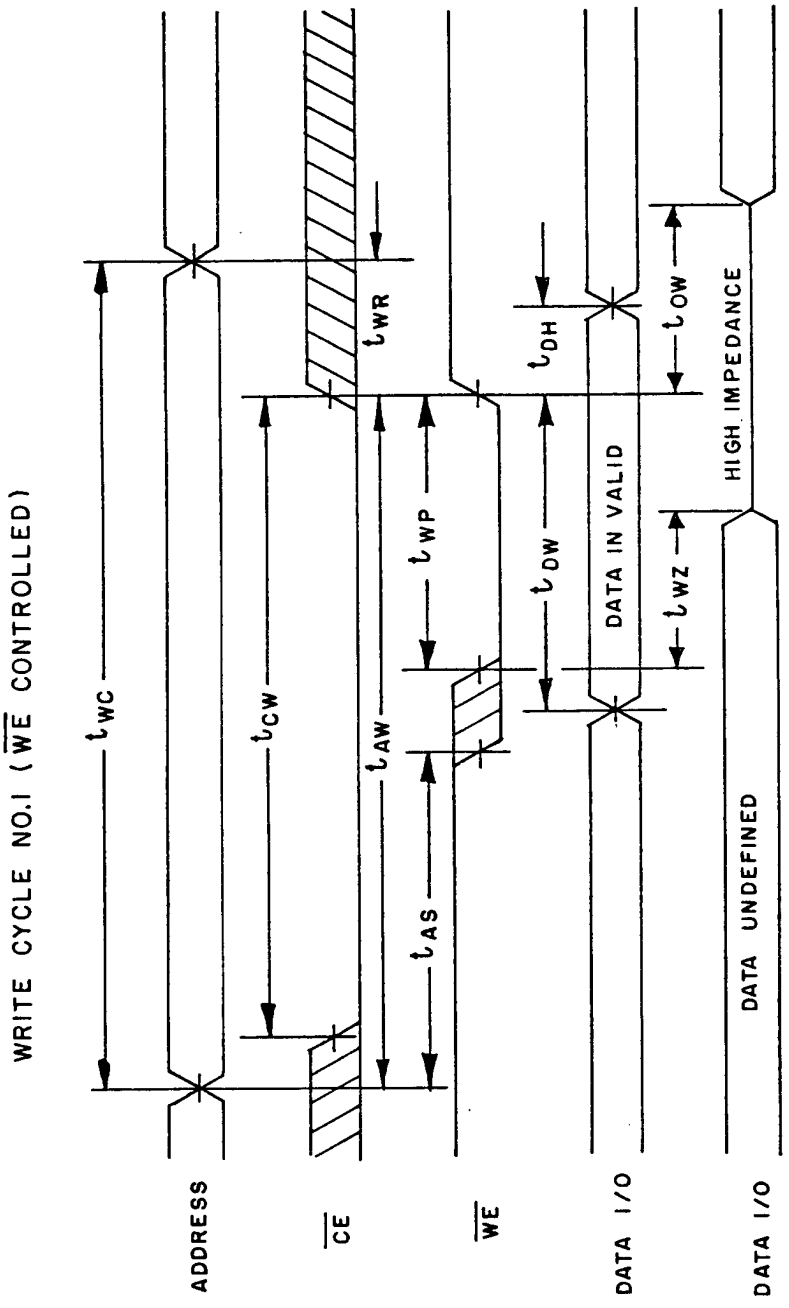
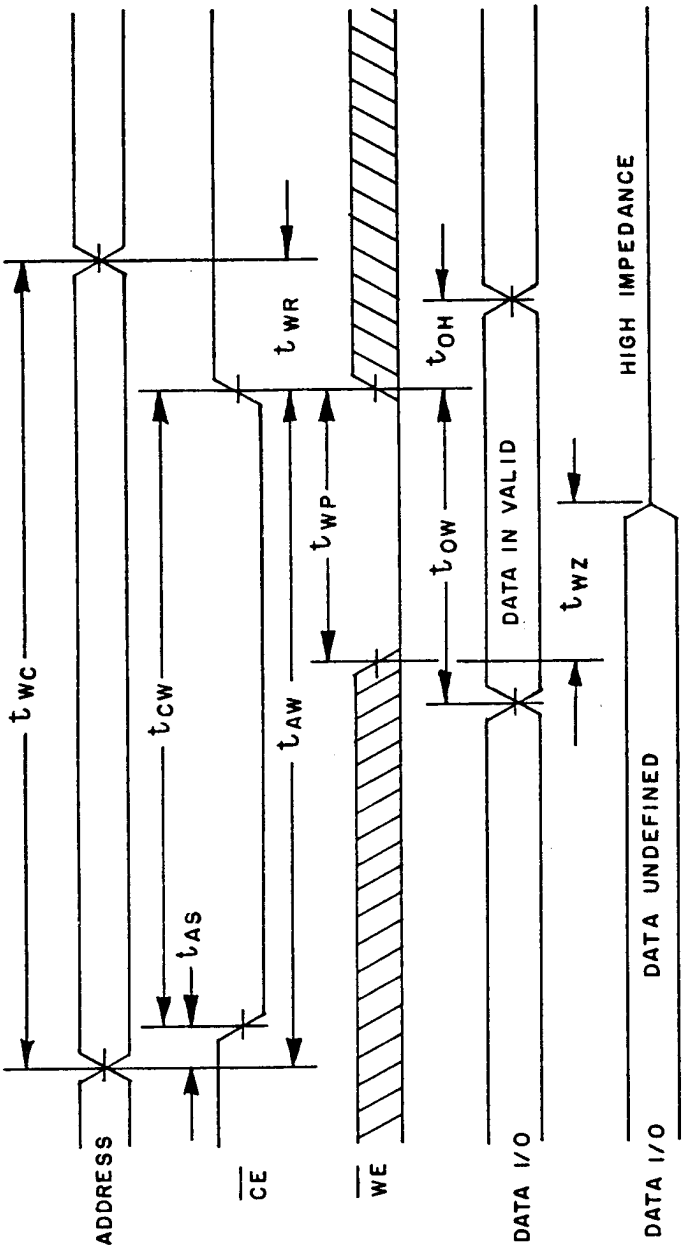


FIGURE 7. Switching waveforms - Continued.

WRITE CYCLE NO. 2 ($\overline{CE}$ CONTROLLED)



Note: If $\overline{CE}$ goes high simultaneously with $\overline{WE}$ high, the output remains in a high impedance state.

FIGURE 7. Switching waveforms - Continued.

3.4 Marking. Marking shall be in accordance with MIL-STD-883 (see 3.1 herein). The part shall be marked with the part number listed in 1.2 herein. In addition, the manufacturer's part number may also be marked as listed in 6.4 herein.

3.5 Certificate of compliance. A certificate of compliance shall be required from a manufacturer in order to be listed as an approved source of supply in 6.4. The certificate of compliance submitted to DESC-ECS prior to listing as an approved source of supply shall state that the manufacturer's product meets the requirements of MIL-STD-883 (see 3.1 herein) and the requirements herein.

3.6 Certificate of conformance. A certificate of conformance as required in MIL-STD-883 (see 3.1 herein) shall be provided with each lot of microcircuits delivered to this drawing.

3.7 Notification of change. Notification of change to DESC-ECS shall be required in accordance with MIL-STD-883 (see 3.1 herein).

3.8 Verification and review. DESC, DESC's agent, and the acquiring activity retain the option to review the manufacturer's facility and applicable required documentation. Offshore documentation shall be made available onshore at the option of the reviewer.

4. QUALITY ASSURANCE PROVISIONS

4.1 Sampling and inspection. Sampling and inspection procedures shall be in accordance with section 4 of MIL-M-38510 to the extent specified in MIL-STD-883 (see 3.1 herein).

4.2 Screening. Screening shall be in accordance with method 5004 of MIL-STD-883, and shall be conducted on all devices prior to quality conformance inspection. The following additional criteria shall apply:

a. Burn-in test, method 1015 of MIL-STD-883.

(1) Test condition A, B, C, or D using the circuit submitted with the certificate of compliance (see 3.5 herein).

(2) T_A = +125°C, minimum.

b. Interim and final electrical test parameters shall be as specified in table II herein, except interim electrical parameter tests prior to burn-in are optional at the discretion of the manufacturer.

4.3 Quality conformance inspection. Quality conformance inspection shall be in accordance with method 5005 of MIL-STD-883 including groups A, B, C, and D inspections. The following additional criteria shall apply.

4.3.1 Group A inspection.

a. Tests shall be as specified in table II herein.

b. Subgroups 5 and 6 in table I, method 5005 of MIL-STD-883 shall be omitted.

c. Subgroup 4 (C_{IN} and C_O measurements) shall be measured only for the initial test and after process or design changes which may affect capacitance.

d. Subgroups 7 and 8 shall test sufficient to verify the truth table.

4.3.2 Groups C and D inspections.

a. End-point electrical parameters shall be as specified in table II herein.

b. Steady-state life test conditions, method 1005 of MIL-STD-883:

TABLE II. Electrical test requirements.

MIL-STD-883 test requirements	Subgroups (per method 5005, table I)
Interim electrical parameters (method 5004)	---
Final electrical test parameters (method 5004)	1*,2,3,7,8, 9,10,11**
Group A test requirements (method 5005)	1,2,3,4***, 8,9,10,11**
Groups C and D end-point electrical parameters (method 5005)	2,8(+125),10

* PDA applies to subgroup 1.
** Subgroups 10 and 11, if not tested, shall be guaranteed to the specified limits in table I.
***(See 4.3.1c).

(1) Test condition A, B, C, or D using the circuit submitted with the certificate of compliance (see 3.5 herein).

(2) T_A = +125°C, minimum.

(3) Test duration: 1,000 hours, except as permitted by method 1005 of MIL-STD-883.

5. PACKAGING

5.1 Packaging requirements. The requirements for packaging shall be in accordance with MIL-M-38510.

6. NOTES

6.1 Intended use. Microcircuits conforming to this drawing are intended for use when military specifications do not exist and qualified military devices that will perform the required function are not available for OEM application. When a military specification exists and the product covered by this drawing has been qualified for listing on QPL-38510, the device specified herein will be inactivated and will not be used for new design. The QPL-38510 product shall be the preferred item for all applications.

6.2 Replaceability. Microcircuits covered by this drawing will replace the same generic device covered by a contractor-prepared specification or drawing.

6.3 Comments. Comments on this drawing should be directed to DESC-ECS, Dayton, Ohio 45444, or telephone 513-296-5375.

6.4 Approved sources of supply. Approved sources of supply are listed herein. Additional sources will be added as they become available. The vendors listed herein have agreed to this drawing and a certificate of compliance (see 3.5 herein) has been submitted to DESC-ECS.

Military drawing part number	Vendor CAGE number	Vendor similar part number 1/
5962-8670501RX	50088	MKB41H68-825
5962-8670502RX	61772	IDT6168LA25DB
5962-8670503RX	04713	6268-35/BRAJC
	50088	MKB41H68-835
5962-8670503XX	04713	6268-35M/BUAJC
5962-8670503YX	04713	6268-35/BYAJC
5962-8670504RX	61772	IDT6168LA35DB
5962-8670505RX	04713	6268-45/BRAJC
	34649	MD51C68-45/B
5962-8670505XX	04713	6268-45M/BUAJC
5962-8670505YX	04713	6268-45/BYAJC
5962-8670506RX	61772	IDT6168LA45DB
5962-8670506XX	2/	AM99CL68-45/BUA
5962-8670507RX	04713	6168-55/BRAJC
5962-8670507XX	04713	6168-55M/BUAJC
5962-8670507YX	04713	6168-55/BYAJC
5962-8670508RX	61772	IDT6168LA55DB
5962-8670508XX	2/	AM99CL68-55/BUA
5962-8670509RX	04713	6168-70/BRAJC
5962-8670509XX	04713	6168-70M/BUAJC
5962-8670509YX	04713	6168-70/BYAJC
5962-8670510RX	61772	IDT6168LA70DB
5962-8670510XX	2/	AM99CL68-70/BUA

See footnotes at end of table.

Military drawing part number	Vendor CAGE number	Vendor similar part number 1/	Replacement military specification part number
5962-8670511RX	60911	IMS1423S-25M	
	61772	IDT6168SA25DB	
5962-8670511XX	60911	IMS1423W-25M	
5962-8670511ZX	60911	IMS1423F-25M	
5962-8670512RX	60911	IMS1423S-35M	
	61772	IDT6168SA35DB	
	34649	MD51C68-35/B	
5962-8670512XX	60911	IMS1423W-35M	
5962-8670512ZX	60911	IMS1423F-35M	
5962-8670513RX	60911	IMS1423S-45M	
	61772	IDT6168SA45DB	
	34649	MD51C68-45/B	
5962-8670513XX	60911	IMS1423W-45M	
5962-8670513ZX	60911	IMS1423F-45M	
5962-8670514RX	60911	IMS1423S-55M	
	61772	IDT6168SA55DB	
	34649	MD51C68-55/B	
5962-8670514XX	60911	IMS1423W-55M	
5962-8670514ZX	60911	IMS1423F-55M	
5962-8670515RX	60911	IMS1423S-70M	
	61772	IDT6168SA70DB	
	34649	MD51C68-70/B	
5962-8670515XX	60911	IMS1423W-70M	
5962-8670515ZX	60911	IMS1423F-70M	

1/ Caution: Do not use this number for item acquisition. Items acquired to this number may not satisfy the performance requirements of this drawing.

2/ Not available from an approved source of supply.

Vendor CAGE number	Vendor name and address
04713	Motorola, Incorporated 7402 S. Price Road Tempe, AZ 85283
34649	Intel Corporation 5000 W. Chandler Boulevard Chandler, AZ 85226
50088	Thomson Components - Mostek Corporation 1310 Electronics Drive Carrollton, TX 75006
61772	Integrated Device Technology Static RAM Division 1566 Moffett Street Salinas, CA 93905
60911	INMOS Corporation 1110 Bayfield Drive Colorado Springs, CO 80935-6000