REVISIONS			
LTR	DESCRIPTION	DATE (YR-MO-DA)	APPROVED
A	Add device type 02, generic 1847. Add two packages, F-5 and C-2. Make changes to paragraphs 1.2.1, 1.2.2, 6.4, table I, and figures 1 and 2. Change drawing CAGE code to 67268.	1989 MAR 22	M.O. Lee

CURRENT CAGE CODE 67268

REV																								
SHEET																								
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REV STATUS OF SHEETS	REV	A	A	A	A	A	A	A	A	A	A	A	A											
	SHEET	1	2	3	4	5	6	7	8	9	10	11	12											

PMIC N/A

STANDARDIZED MILITARY DRAWING

THIS DRAWING IS AVAILABLE FOR USE BY ALL DEPARTMENTS AND AGENCIES OF THE DEPARTMENT OF DEFENSE

AMSC N/A

PREPARED BY: Rick Offner

CHECKED BY: Ray Monnin

APPROVED BY:

DRAWING APPROVAL DATE: 10 MARCH 1987

REVISION LEVEL: A

DEFENSE ELECTRONICS SUPPLY CENTER
DAYTON, OHIO 45444

MICROCIRCUIT, LINEAR, CURRENT MODE PULSE-WIDTH MODULATOR, MONOLITHIC SILICON

SIZE	CAGE CODE	
A	14933	5962-86806

SHEET 1 OF 12

DESC FORM 193-1
SEP 87

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5962-E1056

DISTRIBUTION STATEMENT A. Approved for public release; distribution is unlimited.

1. SCOPE

1.1 Scope. This drawing describes device requirements for class B microcircuits in accordance with 1.2.1 of MIL-STD-883, "Provisions for the use of MIL-STD-883 in conjunction with compliant non-JAN devices".

1.2 Part number. The complete part number shall be as shown in the following example:

5962-86806	01	E	X
Drawing number	Device type (1.2.1)	Case outline (1.2.2)	Lead finish per MIL-M-38510

1.2.1 Device type. The device type shall identify the circuit function as follows:

Device type	Generic number	Circuit function
01	1846	Controller, pulse-width modulator
02	1847	Controller, pulse-width modulator

1.2.2 Case outline. The case outline shall be as designated in appendix C of MIL-M-38510, and as follows:

Outline letter	Case outline
E	D-2 (16-lead, .840" x .310" x .200") dual-in-line package
F	F-5 (16-lead, .440" x .285" x .085") flat package
2	C-2 (20 terminal, .358" x .358" x .100") square leadless chip carrier package

1.3 Absolute maximum ratings.

Supply voltage (V_{IN})	+40 V dc
Collector supply voltage (V_C)	+40 V dc
Output current, source or sink	500 mA dc
Analog inputs	-0.3 V to +V_{IN}
Reference output current	-30 mA dc
Sync output current	-5 mA dc
Error amplifier output current	-5 mA dc
Soft start sink current	50 mA dc
Oscillator charging current	5 mA dc
Power dissipation at T_A = +25°C 1/	1000 mW
Power dissipation at T_C = +25°C 2/	2000 mW
Junction temperature (T_J)	+150°C
Thermal resistance:	
Junction-to-ambient (θ_{JA}):	
Case E	100°C/W
Case F	115°C/W
Case 2	88°C/W
Junction-to-case (θ_{JC})	See MIL-M-38510, appendix C
Lead temperature (soldering, 10 seconds)	+300°C
Storage temperature range	-65°C to +150°C

1/ Derate at 10 mW/°C for T_A above +50°C.
2/ Derate at 16 mW/°C for T_C above +25°C.

1.4 Recommended operating conditions.

Supply voltage range - - - - - - - - - - - - - - - - -	+8 V dc to +40 V dc
Collector supply voltage range - - - - - - - - - - - -	+4.5 V dc to +40 V dc
Ambient operating temperature range (T_A) - - - - - -	-55°C to +125°C

2. APPLICABLE DOCUMENTS

2.1 Government specification and standard. Unless otherwise specified, the following specification and standard, of the issue listed in that issue of the Department of Defense Index of Specifications and Standards specified in the solicitation, form a part of this drawing to the extent specified herein.

SPECIFICATION

MILITARY

MIL-M-38510 - Microcircuits, General Specification for.

STANDARD

MILITARY

MIL-STD-883 - Test Methods and Procedures for Microelectronics.

(Copies of the specification and standard required by manufacturers in connection with specific acquisition functions should be obtained from the contracting activity or as directed by the contracting activity.)

2.2 Order of precedence. In the event of a conflict between the text of this drawing and the references cited herein, the text of this drawing shall take precedence.

3. REQUIREMENTS

3.1 Item requirements. The individual item requirements shall be in accordance with 1.2.1 of MIL-STD-883, "Provisions for the use of MIL-STD-883 in conjunction with compliant non-JAN devices" and as specified herein.

3.2 Design, construction, and physical dimensions. The design, construction, and physical dimensions shall be as specified in MIL-M-38510 and herein.

3.2.1 Terminal connections. The terminal connections shall be as specified on figure 1.

3.2.2 Block diagram. The block diagram shall be as specified on figure 2.

3.2.3 Case outline. The case outline shall be in accordance with 1.2.2 herein.

3.3 Electrical performance characteristics. Unless otherwise specified, the electrical performance characteristics are as specified in table I and apply over the full ambient operating temperature range.

3.4 Marking. Marking shall be in accordance with MIL-STD-883 (see 3.1 herein). The part shall be marked with the part number listed in 1.2 herein. In addition, the manufacturer's part number may also be marked as listed in 6.4 herein.

3.5 Certificate of compliance. A certificate of compliance shall be required from a manufacturer in order to be listed as an approved source of supply in 6.4. The certificate of compliance submitted to DESC-ECS prior to listing as an approved source of supply shall state that the manufacturer's product meets the requirements of MIL-STD-883 (see 3.1 herein) and the requirements herein.

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Device type	01 and 02	
Case outlines	E and F	2
Terminal number	Terminal symbol	
1	CUR. LIMIT/SOFTSTART	NC
2	V_{REF}	CUR. LIMIT/SOFTSTART
3	(-) CUR. SENSE	V_{REF}
4	(+) CUR. SENSE	(-) CUR. SENSE
5	(+) ERROR AMP	(+) CUR. SENSE
6	(-) ERROR AMP	NC
7	COMPENSATION	(+) ERROR AMP
8	C_T	(-) ERROR AMP
9	R_T	COMPENSATION
10	SYNC	C_T
11	OUTPUT A	NC
12	GROUND	R_T
13	V_C	SYNC
14	OUTPUT B	OUTPUT A
15	V_{IN}	GROUND
16	SHUTDOWN	NC
17	---	V_C
18	---	OUTPUT B
19	---	V_{IN}
20	---	SHUTDOWN

NC = no connection

FIGURE 1. Terminal connections.

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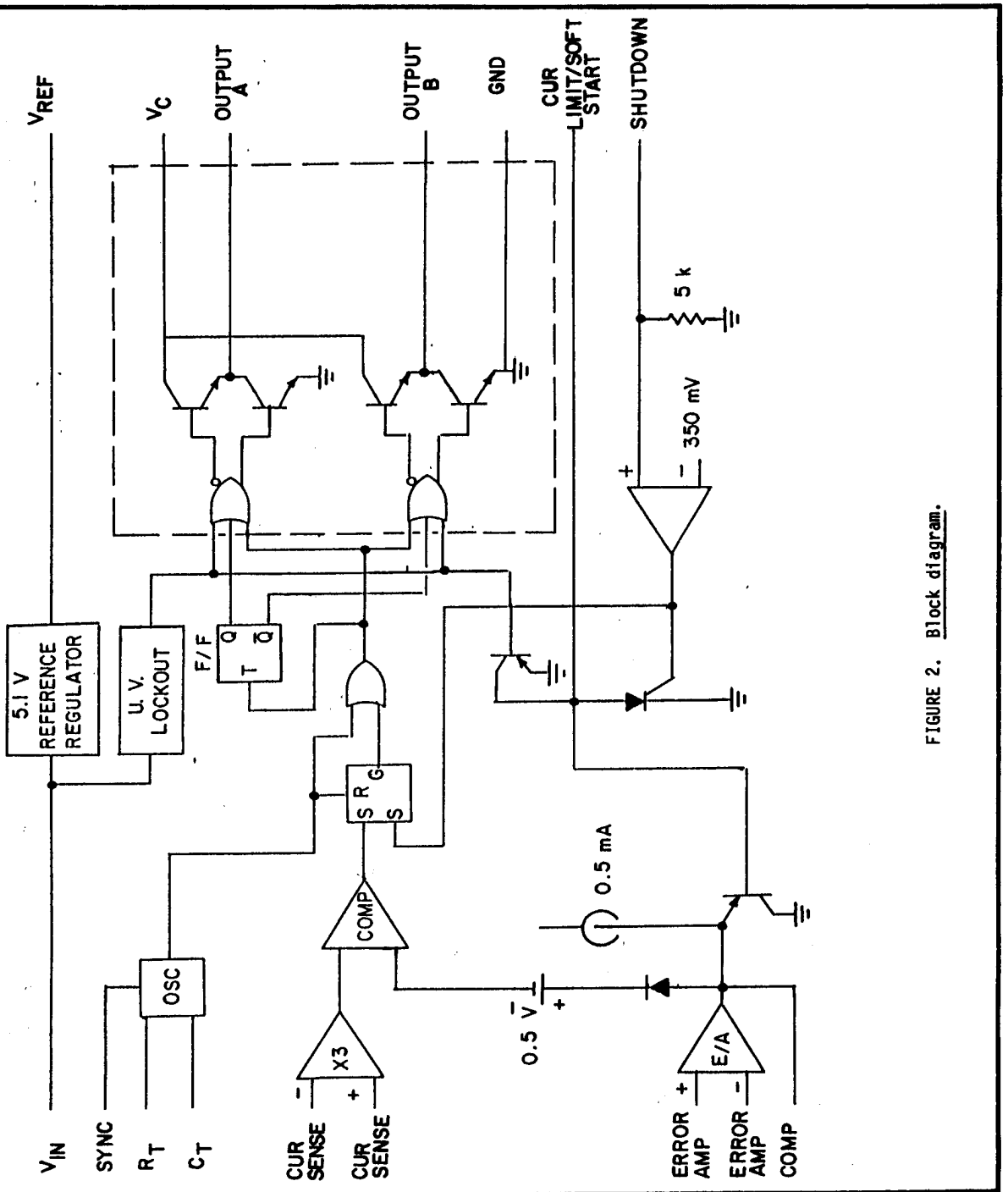

FIGURE 2. Block diagram.

STANDARDIZED MILITARY DRAWING DEFENSE ELECTRONICS SUPPLY CENTER DAYTON, OHIO 45444	SIZE A		5962-86806
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TABLE I. Electrical performance characteristics.

Test	Symbol	Conditions 1/ $-55°C \le T_A \le +125°C$	Group A subgroups	Limits		Unit
				Min	Max	
Reference section						
Output voltage	V_O	$T_A = +25°C$ $I_O = 1$ mA	1	5.05	5.15	V dc
Line regulation	R_{LINE}	8 V $\le V_{IN} \le$ 40 V	1, 2, 3	-20	20	mV dc
Load regulation	R_{LOAD}	-10 mA $\le I_L \le$ -1 mA	1, 2, 3	-15	15	mV dc
Total output variation 2/		Line, load, and temperature		5.00	5.20	V dc
Short circuit output	I_{OS}	V_{REF} = 0 V	1, 2, 3	-1	-10	mA dc
Oscillator section						
Initial accuracy		$T_A = +25°C$ R_T = 10 kΩ C_T = 4700 pF	4	39	47	kHz
Frequency change with voltage	Δf_{OSC}	8 V $\le V_I \le$ 40 V	4, 5, 6	-2.0	2.0	%
Sync output voltage High level Low level	 V_{SOH} V_{SOL}		1, 2, 3	 3.9	 2.7	V dc
Sync input voltage High level Low level	 V_{SIH} V_{SIL}	C_T = 0 V	1, 2, 3	 3.9	 2.5	V dc
Sync input current	I_{SYNC}	Sync voltage = 5.25 V C_T = 0 V	1, 2, 3		1.5	mA dc
Error amplifier section						
Input offset voltage	V_{IO}		1, 2, 3		5.0	mV dc
Input bias current	I_{IB}		1, 2, 3	-1.0		µA dc

See footnotes at end of table.

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TABLE I. Electrical performance characteristics - Continued.

Test	Symbol	Conditions 1/ $-55°C \le T_A \le +125°C$	Group A subgroups	Limits Min	Limits Max	Unit
Error amplifier section - Continued.						
Input offset current	I_{IO}		1, 2, 3	-250	250	nA dc
Open loop voltage gain	A_{VS}	ΔV_O = 1.2 V to 3 V V_{CM} = 2 V	4, 5, 6	80		dB
Unity gain bandwidth 2/	G_{BW}	T_A = +25°C	4	0.7		MHz
Common mode rejection ratio	CMRR	0 V $\le V_{CM} \le$ 38 V V_{IN} = 40 V	4, 5, 6	75		dB
Power supply rejection ratio	PSRR	8 V $\le V_{IN} \le$ 40 V	4, 5, 6	80		dB
Output sink current (COMPENSATION pin)	I_{SINK}	-15 mV $\le V_{ID} \le$ -5 V $V_{COMP\ pin}$ = 1.2 V	1, 2, 3	2.0		mA dc
Output source current (COMPENSATION pin)	I_{SOURCE}	15 mV $\le V_{ID} \le$ 5 V $V_{COMP\ pin}$ = 2.5 V	1, 2, 3		-0.4	mA dc
High level output voltage	V_{OH}	R_L = (COMP) 15 kΩ	1, 2, 3	4.3		V dc
Low level output voltage	V_{OL}	R_L = (COMP) 15 kΩ	1, 2, 3		1.0	V dc
Current sense amplifier section						
Amplifier gain	A_V	$V_{(-CUR\ SENSE\ pin)}$ = 0 V $V_{(CUR\ LIM/SS\ pin)}$ open 3/ 4/	4, 5, 6	2.5	3.15	V dc
Maximum differential input signal (pos and neg current sense pin voltages)	V_{IDIFF}	$V_{(CUR\ LIM/SS\ pin)}$ open 3/ R_L = (COMP pin) = 15 kΩ	1, 2, 3	1.1		V dc
Input offset voltage	V_{IO}	$V_{(CUR\ LIM/SS\ pin)}$ = 0.5 V COMP pin open 3/	1, 2, 3	-25	25	mV dc

See footnotes at end of table.

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TABLE I. Electrical performance characteristics - Continued.

Test	Symbol	Conditions 1/ $-55°C \le T_A \le +125°C$	Group A subgroups	Limits		Unit
				Min	Max	
Current sense amplifier section						
Common mode rejection	CMRR	$1 V \le V_{CM} \le 12 V$	4, 5, 6	60		dB
Power supply rejection	PSRR	$8 V \le V_{IN} \le 40 V$	4, 5, 6	60		dB
Input bias current	I_{IB}	$V_{(CUR LIM/SS pin)} = 0.5 V$, COMP pin open 3/	1, 2, 3	-10		µA dc
Input offset current	I_{IO}	$V_{(CUR LIM/SS pin)} = 0.5 V$, COMP pin open 3/	1, 2, 3	-1.0	1.0	µA dc
Delay to outputs 2/		$T_A = +25°C$	9		500	ns
Current limit adjust section						
Current limit offset		$V_{(-CUR SENSE pin)} = 0 V$, $V_{(+CUR SENSE pin)} = 0 V$, COMP pin open 3/	1, 2, 3	0.40	0.55	V dc
Input bias current	I_{IB}	$V_{(+ERROR AMP pin)} = V_{REF}$, $V_{(-ERROR AMP pin)} = 0 V$	1, 2, 3	-30		µA dc
Shutdown terminal section						
Threshold voltage			1, 2, 3	250	400	mV dc
Latching voltage		Current into CUR LIM/SS pin = 3.0 mA 5/			2.0	V dc
Nonlatching voltage		Current into CUR LIM/SS pin = 0.8 mA 6/		5.0		V dc
Delay to outputs 2/		$T_A = +25°C$	1		600	ns
Output section						
Collector-emitter voltage			1, 2, 3	40		V dc
Collector leakage current		$V_C = 40 V$ 7/	1, 2, 3		200	µA dc

See footnotes at end of table.

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TABLE I. Electrical performance characteristics - Continued.

Test	Symbol	Conditions 1/ $-55°C \le T_A \le +125°C$	Group A subgroups	Limits Min	Limits Max	Unit
Output low level	V_{OL}	I_{SINK} = 20 mA I_{SINK} = 100 mA	1, 2, 3		0.4 2.1	V dc
Output high level	V_{OL}	I_{SOURCE} = 20 mA I_{SOURCE} = 100 mA	1, 2, 3	13 12		V dc
Output section - Continued						
Rise time 2/	t_r	C_L = 1,000 pF T_A = +25°C	9		300	ns
Fall time 2/	t_f	C_L = 1,000 pF T_A = +25°C	9		300	ns
Under-voltage lockout section						
Start-up threshold			1, 2, 3		8.0	V dc
Total standby current						
Supply current	I_{CC}		1, 2, 3		21	mA dc
Cold start/PWM latch reset	L_{reset}	T_J = -55°C, R_T = 10 kΩ, C_T = 4700 pF, SYNC I_{OUT} = -1 mA	3	8/		kHz

1/ Standard test conditions (unless otherwise specified): $+V_{IN}$ = 15 V dc, R_T = 10 kΩ; C_T = 4,700 pF.
2/ If not tested, shall be guaranteed to specified limits.
3/ Parameter measured at trip point of latch with $V_{+ERROR\ AMP}$= V_{REF}; $V_{-ERROR\ AMP}$= 0V.
4/ Amplifier gain defined as:

$$G = \frac{\Delta V_{COMP\ pin}}{\Delta V_{+CURRENT\ SENSE\ pin}};\ \Delta V_{+CURRENT\ SENSE\ pin} = 0 \text{ to } 1.0\ V$$

5/ Current into CUR LIM/SS pin guaranteed to latch circuit in shutdown state.
6/ Current into CUR LIM/SS pin guaranteed not to latch circuit in shutdown state.
7/ This parameter only applies to device type 01.
8/ To verify that the PWM latch is resetting properly, the output stage must resume switching after the completion of a PWN latch Set command. To minimize the effects of self heating, the test must be completed within the first 50 milliseconds of applied power. The minimum limit shall be equal to 0.49 x the oscillator frequency.

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3.6 Certificate of conformance. A certificate of conformance as required in MIL-STD-883 (see 3.1 herein) shall be provided with each lot of microcircuits delivered to this drawing.

3.7 Notification of change. Notification of change to DESC-ECS shall be required in accordance with MIL-STD-883 (see 3.1 herein).

3.8 Verification and review. DESC, DESC's agent and the acquiring activity reserve the right to retain the option to review the manufacturer's facility and applicable required documentation. Off-shore documentation shall be made available on-shore at the option of the reviewer.

4. QUALITY ASSURANCE PROVISIONS

4.1 Sampling and inspection. Sampling and inspection procedures shall be in accordance with section 4 of MIL-M-38510 to the extent specified in MIL-STD-883 (see 3.1 herein).

4.2 Screening. Screening shall be in accordance with method 5004 of MIL-STD-883, and shall be conducted on all devices prior to quality conformance inspection. The following additional criteria shall apply:

a. Burn-in test, method 1015 of MIL-STD-883.

(1) Test condition A, B, C, or D using the circuit submitted with the certificate of compliance (see 3.5 herein).

(2) T_A = +125°C, minimum.

b. Interim and final electrical test parameters shall be as specified in table II herein, except interim electrical parameter tests prior to burn-in are optional at the discretion of the manufacturer.

4.3 Quality conformance inspection. Quality conformance inspection shall be in accordance with method 5005 of MIL-STD-883 including groups A, B, C, and D inspections. The following additional criteria shall apply.

4.3.1 Group A inspection.

a. Tests shall be as specified in table II herein.

b. Subgroups 7, 8, 10, and 11 in table I, method 5005 of MIL-STD-883 shall be omitted.

4.3.2 Groups C and D inspections.

a. End-point electrical parameters shall be as specified in table II herein.

b. Steady-state life test conditions, method 1005 of MIL-STD-883.

(1) Test condition A, B, C, or D using the circuit submitted with the certificate of compliance (see 3.5 herein).

(2) T_A = +125°C, minimum.

(3) Test duration: 1,000 hours, except as permitted by method 1005 of MIL-STD-883.

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TABLE II. Electrical test requirements.

MIL-STD-883 test requirements	Subgroups (per method 5005, table I)
Interim electrical parameters (method 5004)	1
Final electrical test parameters (method 5004)	1*,2,3,4,9
Group A test requirements (method 5005)	1,2,3,4,5,6,9
Groups C and D end-point electrical parameters (method 5005)	1,2,3

*PDA applies to subgroup 1.

5. PACKAGING

5.1 Packaging requirements. The requirements for packaging shall be in accordance with MIL-M-38510.

6. NOTES

6.1 Intended use. Microcircuits conforming to this drawing are intended for use when military specifications do not exist and qualified military devices that will perform the required function are not available for OEM application. When a military specification exists and the product covered by this drawing has been qualified for listing on QPL-38510, the device specified herein will be inactivated and will not be used for new design. The QPL-38510 product shall be the preferred item for all applications.

6.2 Replaceability. Microcircuits covered by this drawing will replace the same generic device covered by a contractor-prepared specification or drawing.

6.3 Comments. Comments on this drawing should be directed to DESC-ECS, Dayton, Ohio 45444, or telephone 513-296-5375.

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6.4 Approved source of supply. Approved sources of supply are listed herein. Additional sources will be added as they become available. The vendors listed herein have agreed to this drawing and a certificate of compliance (see 3.5 herein) has been submitted to DESC-ECS.

Military drawing part number	Vendor CAGE number	Vendor similar part number 1/
5962-8680601EX	12969 64155 34333	UC1846J/883B LT1846J/883B SG1846J/883B
5962-8680601FX	34333	SG1846F/883B
5962-86806012X	12969 34333	UC1846L/883B SG1846L/883B
5962-8680602EX	34333 12969 64155	SG1847J/883B UC1847J/883B LT1847J/883B
5962-8680602FX	34333	SG1847F/883B
5962-86806022X	12969 34333	UC1847L/883B SG1847L/883B

1/ Caution. Do not use this number for item acquisition. Items acquired to this number may not satisfy the performance requirements of this drawing.

Vendor CAGE number	Vendor name and address
12969	Unitrode Corporation 5 Forbes Road Lexington, MA 02173
34333	Silicon General, Incorporated 11861 Western Avenue Garden Grove, CA 92641
64155	Linear Technology Corporation 1630 McCarthy Boulevard Milpitas, CA 95035-7487