| REVISIONS | | | |
|---|---|---|---|
| LTR | DESCRIPTION | DATE (YR-MO-DA) | APPROVED |
| A | Add parameter $I_{LIR}$ to table I. Remove vendor CAGE 34335. Change drawing CAGE code. Editorial changes throughout. | 1989 MAR 01 | M. A. Frye |

**CURRENT CAGE CODE 67268**

| | | | | | | | | | | | | | | | | | | | | | | | | |
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| REV | | | | | | | | | | | | | | | | | | | | | | | | |
| SHEET | | | | | | | | | | | | | | | | | | | | | | | | |
| REV | | | | | | | | | | | | | | | | | | | | | | | | |
| SHEET | | | | | | | | | | | | | | | | | | | | | | | | |
| REV STATUS OF SHEETS | REV | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | | | | | | | | |
| | SHEET | 1 | 2 | 3 | 4 | 5 | 6 | 7 | 8 | 9 | 10 | 11 | 12 | 13 | 14 | 15 | | | | | | | | |

PMIC N/A

**STANDARDIZED MILITARY DRAWING**

THIS DRAWING IS AVAILABLE FOR USE BY ALL DEPARTMENTS AND AGENCIES OF THE DEPARTMENT OF DEFENSE

AMSC N/A

PREPARED BY: Greg A. Pitz

CHECKED BY: Ray Monnin

APPROVED BY:

DRAWING APPROVAL DATE: 10 MARCH 1987

REVISION LEVEL: A

DEFENSE ELECTRONICS SUPPLY CENTER
DAYTON, OHIO 45444

MICROCIRCUIT, DIGITAL, NMOS, PROGRAMMABLE INTERRUPT CONTROLLER, MONOLITHIC SILICON

| SIZE | CAGE CODE | |
|---|---|---|
| A | 14933 | 5962-87518 |

SHEET 1 OF 15

DESC FORM 193-1
SEP 87

* U.S. GOVERNMENT PRINTING OFFICE: 1987 — 748-129/60912

5962-E1200

1. SCOPE

1.1 Scope. This drawing describes device requirements for class B microcircuits in accordance with 1.2.1 of MIL-STD-883, "Provisions for the use of MIL-STD-883 in conjunction with compliant non-JAN devices."

1.2 Part number. The complete part number shall be as shown in the following example:

| 5962-87518 | 01 | X | X |
|---|---|---|---|
| Drawing number | Device type (1.2.1) | Case outline (1.2.2) | Lead finish per MIL-M-38510 |

1.2.1 Device type. The device type shall identify the circuit function as follows:

| Device type | Generic number | Circuit function |
|---|---|---|
| 01 | 8259A | Programmable interrupt controller |

1.2.2 Case outlines. The case outlines shall be as designated in appendix C of MIL-M-38510, and as follows:

| Outline letter | Case outline |
|---|---|
| X | D-10 (28-lead, 1.490" x .610" x .232"), dual-in-line package |
| 3 | C-4 (28-terminal, .460" x .460" x .100") square chip carrier package |

1.3 Absolute maximum ratings.

| | |
|---|---|
| Supply voltage range | +4.5 V dc to +5.5 V dc |
| Input voltage range | -0.5 V dc to +7.0 V dc |
| Storage temperature range | -65°C to +150°C |
| Maximum power dissipation ($P_D$) | 1.0 W |
| Lead temperature (soldering, 5 seconds) | +270°C |
| Thermal resistance, junction-to-case ($\theta_{JC}$): Case X and 3 | See MIL-M-38510 appendix C |
| Junction temperature ($T_J$) | +150°C |

1.4 Recommended operating conditions.

| | |
|---|---|
| Supply voltage range ($V_{CC}$) | +4.5 V dc to +5.5 V dc |
| Minimum high level input voltage ($V_{IH}$) | +2.3 V dc |
| Maximum high level input voltage ($V_{IH}$) | $V_{CC}$ +0.5 V dc |
| Minimum low level input voltage ($V_{IL}$) | -0.5 V dc |
| Maximum low level input voltage ($V_{IL}$) | +0.8 V dc |
| Case operating temperature range ($T_C$) | -55°C to +125°C |

2. APPLICABLE DOCUMENTS

2.1 Government specification and standard. Unless otherwise specified, the following specification and standard, of the issue listed in that issue of the Department of Defense Index of Specifications and Standards specified in the solicitation, form a part of this drawing to the extent specified herein.

SPECIFICATION

MILITARY

MIL-M-38510 - Microcircuits, General Specification for.

STANDARD

MILITARY

MIL-STD-883 - Test Methods and Procedures for Microelectronics.

(Copies of the specification and standard required by manufacturers in connection with specific acquisition functions should be obtained from the contracting activity or as directed by the contracting activity.)

2.2 Order of precedence. In the event of a conflict between the text of this drawing and the references cited herein, the text of this drawing shall take precedence.

3. REQUIREMENTS

3.1 Item requirements. The individual item requirements shall be in accordance with 1.2.1 of MIL-STD-883, "Provisions for the use of MIL-STD-883 in conjunction with compliant non-JAN devices" and as specified herein.

3.2 Design, construction, and physical dimensions. The design, construction, and physical dimensions shall be as specified in MIL-M-38510 and herein.

3.2.1 Terminal connections. The terminal connections shall be as specified on figure 1.

3.2.2 Logic diagram. The logic diagram shall be as specified on figure 2.

3.2.3 Case outlines. The case outlines shall be in accordance with 1.2.2 herein.

3.3 Electrical performance characteristics. Unless otherwise specified, the electrical performance characteristics are as specified in table I and apply over the full case operating temperature range.

3.4 Marking. Marking shall be in accordance with MIL-STD-883 (see 3.1 herein). The part shall be marked with the part number listed in 1.2 herein. In addition, the manufacturer's part number may also be marked as listed in 6.5 herein.

3.5 Certificate of compliance. A certificate of compliance shall be required from a manufacturer in order to be listed as an approved source of supply in 6.5. The certificate of compliance submitted to DESC-ECS prior to listing as an approved source of supply shall state that the manufacturer's product meets the requirements of MIL-STD-883 (see 3.1 herein) and the requirements herein.

TABLE I. Electrical performance characteristics.

| Test | Symbol | Conditions $-55°C < T_C < +125°C$ unless otherwise specified | | Group A subgroups | Limits | | Unit |
|---|---|---|---|---|---|---|---|
| | | | | | Min | Max | |
| Input low voltage | $V_{IL}$ | $V_{CC}$ = 5 V ±10% | | 1, 2, 3 | | .8 1/ | V |
| Input high voltage | $V_{IH}$ | $V_{CC}$ = 5 V ±10% | | 1, 2, 3 | 2.3 | | V |
| Low level output voltage | $V_{OL}$ | $V_{CC}$ = 5 V ±10%<br>$I_{OL}$ = 2.2 mA | | 1, 2, 3 | | .45 | V |
| High level output voltage | $V_{OH}$ | $V_{CC}$ = 5 V ±10%<br>$I_{OH}$ = -400 µA | | 1, 2, 3 | 2.4 | | V |
| Interrupt high level output voltage | $V_{OH}$ (INT) | $V_{CC}$ = 4.5 V | $I_{OH}$ = -100 µA | 1, 2, 3 | 3.5 | | V |
| | | | $I_{OH}$ = -400 µA | | 2.4 | | V |
| Input load current | $I_{LI}$ | $V_{CC}$ = 5.5 V<br>$V_{IN}$= 0 V to 5.5 V | | 1, 2, 3 | -10 2/ | +10 | µA |
| Input load current IR0 - IR7 | $I_{LIR}$ | $V_{CC}$ = 5.5 V<br>$V_{IN}$= 0 V to 5.5 V | | 1, 2, 3 | -300 2/ | +10 | µA |
| Output leakage current | $I_{LOL}$ | $V_{CC}$ = 5.5 V, $V_{OUT}$ = 0.45 to 4.5 V | | 1, 2, 3 | -10 2/ | +10 | µA |
| | $I_{LOH}$ | $V_{OUT}$ = $V_{CC}$, $V_{CC}$ = 5.5 V | | 1, 2, 3 | | +10 | µA |
| $V_{CC}$ supply current | $I_{CC}$ | $V_{CC}$ = 5.5 V 3/<br>Outputs loaded static | | 1, 2, 3 | | 125 | mA |
| Input capacitance | $C_{IN}$ | FC = 1 MHz, $T_C$ = +25°C<br>See 4.3.1d | | 4 | | 10 | pF |
| I/O capacitance | $C_{I/O}$ | $T_C$ = +25°C<br>See 4.3.1d | | 4 | | 20 | pF |
| Functional tests | | See 4.3.1c | | 7, 8 | | | |

See footnotes at end of table.



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TABLE I. Electrical performance characteristics - Continued.

| Test | Symbol | Conditions $-55°C \le T_C \le +125°C$ unless otherwise specified | Group A subgroups | Limits Min | Limits Max | Unit |
|---|---|---|---|---|---|---|
| AO/$\overline{CS}$ setup to $\overline{RD}$/$\overline{INTA}$ falling | $t_{AHRL}$ | See figure 3 4/ | 9,10,11 | 0 | | ns |
| AO/$\overline{CS}$ hold after $\overline{RD}$/$\overline{INTA}$ rising | $t_{RHAX}$ | | 9,10,11 | 0 | | ns |
| $\overline{RD}$ pulse width | $t_{RLRH}$ | | 9,10,11 | 235 | | ns |
| AO/$\overline{CS}$ setup to $\overline{WR}$ falling | $t_{AHWL}$ | | 9,10,11 | 0 | | ns |
| AO/$\overline{CS}$ hold after $\overline{WR}$ rising | $t_{WHAX}$ | | 9,10,11 | 0 | | ns |
| $\overline{WR}$ pulse width | $t_{WLWH}$ | | 9,10,11 | 290 | | ns |
| Data setup to $\overline{WR}$ rising | $t_{DVWH}$ | | 9,10,11 | 240 | | ns |
| Data hold after $\overline{WR}$ rising | $t_{WHDX}$ | | 9,10,11 | 0 | | ns |
| Interrupt request width (low) 5/ | $t_{JLJH}$ | | 9,10,11 | 100 | | ns |
| Cascade setup to second or third $\overline{INTA}$ falling (slave only) | $t_{CVIAL}$ | | 9,10,11 | 55 | | ns |
| End of $\overline{RD}$ to next command | $t_{RHRL}$ | | 9,10,11 | 300 | | ns |

See footnotes at end of table.

TABLE I. Electrical performance characteristics - Continued.

| Test | Symbol | Conditions $-55°C \le T_C \le +125°C$ unless otherwise specified | Group A subgroups | Limits Min | Limits Max | Unit |
|---|---|---|---|---|---|---|
| End of $\overline{WR}$ to next command | $t_{WHRL}$ | See figure 3 4/ | 9,10,11 | 370 | | ns |
| Data valid from $\overline{RD}/\overline{INTA}$ falling 6/ | $t_{RLDV}$ | | 9,10,11 | | 200 | ns |
| Data float after $\overline{RD}/\overline{INTA}$ rising 6/ | $t_{RHDZ}$ | | 9,10,11 | 10 2/ | 100 | ns |
| Interrupt output delay 6/ | $t_{JHIH}$ | | 9,10,11 | | 350 | ns |
| Cascade valid from first $\overline{INTA}$ falling (master only) 6/ | $t_{IALCV}$ | | 9,10,11 | | 565 | ns |
| Enable active 6/ from $\overline{RD}$ falling or $\overline{INTA}$ falling | $t_{RLEL}$ | | 9,10,11 | | 125 | ns |
| Enable inactive from $\overline{RD}$ rising or $\overline{INTA}$ rising 6/ | $t_{RHEH}$ | | 9,10,11 | | 150 | ns |
| Data valid from stable address 6/ | $t_{AHDV}$ | | 9,10,11 | | 200 | ns |
| Cascade valid to valid data 6/ | $t_{CVDV}$ | | 9,10,11 | | 300 | ns |

See footnotes on next page.

1/ Due to test equipment limitations, actual tested values may differ from those specified but specific limits are guaranteed.
2/ Guaranteed if not tested to the limits specified.
3/ $I_{CC}$ is measured in a static condition with outputs in a worst case state having standard $I_{OL}/I_{OH}$ loads applied.
4/ Test conditions: $V_{CC}$ = 5 V ±10% (see figure 4), $V_{IL}$ = 0.45 V, $V_{OL}$ = 0.8 V, $I_{OL}$ = 2.2 mA, $V_{IH}$ = 2.4 V, $V_{OH}$ = 2.0 V, $I_{OH}$ = -400 µA.
5/ This is the low time required to clear the input latch in the edge triggered mode.
6/ Test conditions: Capacitance of data bus: Maximum test = 100 pF, minimum test = 15 pF, $C_{INT}$ = 100 pF, $C_{ENABLE}$ = 15 pF (see figure 5).

3.6 Certificate of conformance. A certificate of conformance as required in MIL-STD-883 (see 3.1 herein) shall be provided with each lot of microcircuits delivered to this drawing.

3.7 Notification of change. Notification of change to DESC-ECS shall be required in accordance with MIL-STD-883 (see 3.1 herein).

3.8 Verification and review. DESC, DESC's agent, and the acquiring activity retain the option to review the manufacturer's facility and applicable required documentation. Offshore documentation shall be made available onshore at the option of the reviewer.

4. QUALITY ASSURANCE PROVISIONS

4.1 Sampling and inspection. Sampling and inspection procedures shall be in accordance with section 4 of MIL-M-38510 to the extent specified in MIL-STD-883 (see 3.1 herein).

4.2 Screening. Screening shall be in accordance with method 5004 of MIL-STD-883, and shall be conducted on all devices prior to quality conformance inspection. The following additional criteria shall apply:

a. Burn-in test, method 1015 of MIL-STD-883.

(1) Test condition C or D using the circuit submitted with the certificate of compliance (see 3.5 herein).

(2) $T_A$ = +125°C, minimum.

b. Interim and final electrical test parameters shall be as specified in table II herein, except interim electrical parameter tests prior to burn-in are optional at the discretion of the manufacturer.

4.3 Quality conformance inspection. Quality conformance inspection shall be in accordance with method 5005 of MIL-STD-883 including groups A, B, C, and D inspections. The following additional criteria shall apply.

4.3.1 Group A inspection.

a. Tests shall be as specified in table II herein.

b. Subgroups 5 and 6 in table I, method 5005 of MIL-STD-883 shall be omitted.

c. Subgroups 7 and 8 testing shall be sufficient to verify the functional operation of the device.

d. Subgroup 4 ($C_{IN}$ and $C_{I/O}$ measurements) shall be measured initially and after process or design changes which may affect input or output capacitance. A minimum sample size of five devices with zero rejects shall be required.

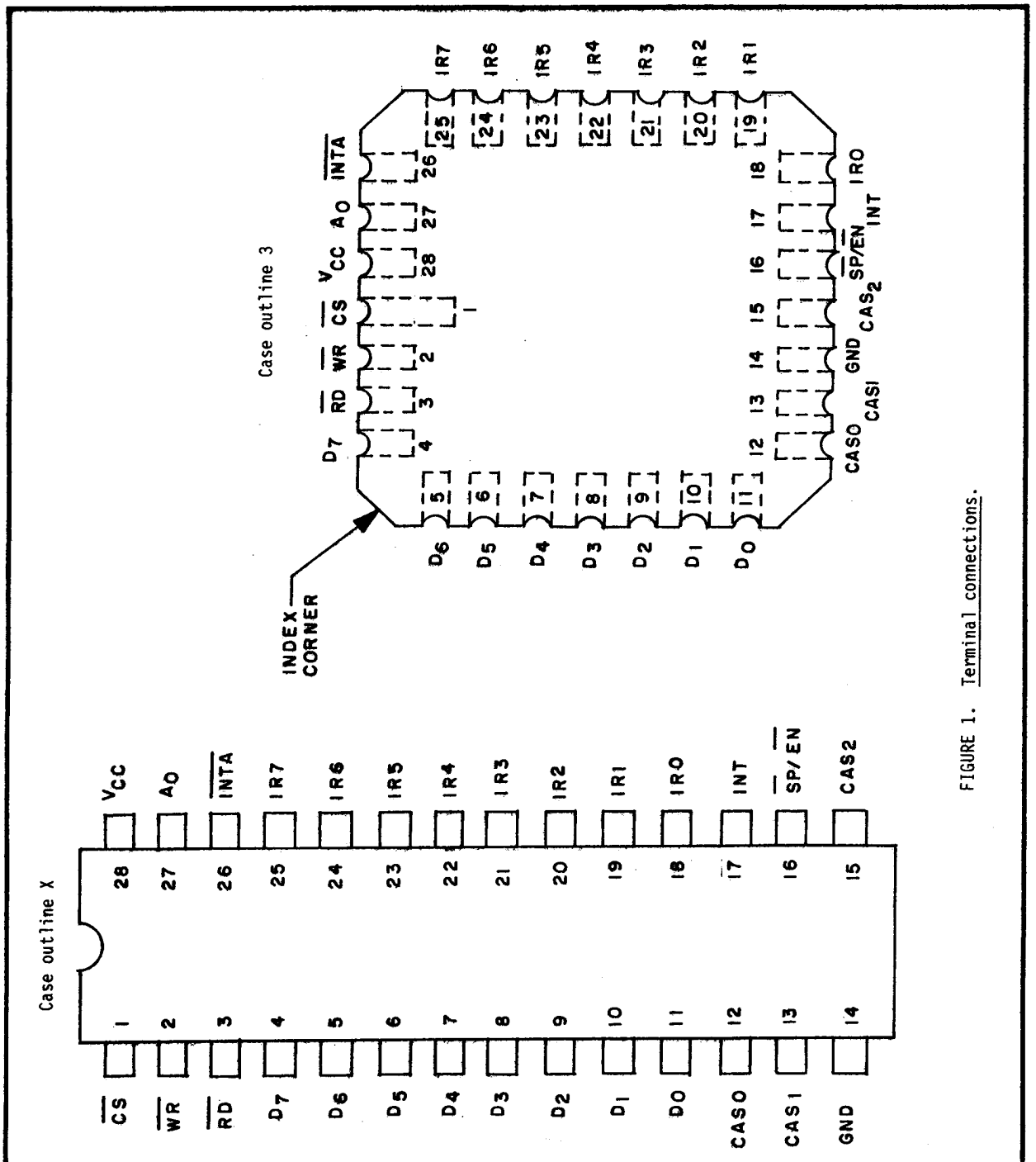



FIGURE 1. Terminal connections.

| STANDARDIZED MILITARY DRAWING<br>DEFENSE ELECTRONICS SUPPLY CENTER<br>DAYTON, OHIO 45444 | SIZE<br>A | | 5962-87518 |
|---|---|---|---|
| | | REVISION LEVEL<br>A | SHEET<br>8 |

DESC FORM 193A
SEP 87

★ U. S. GOVERNMENT PRINTING OFFICE: 1988—550-547

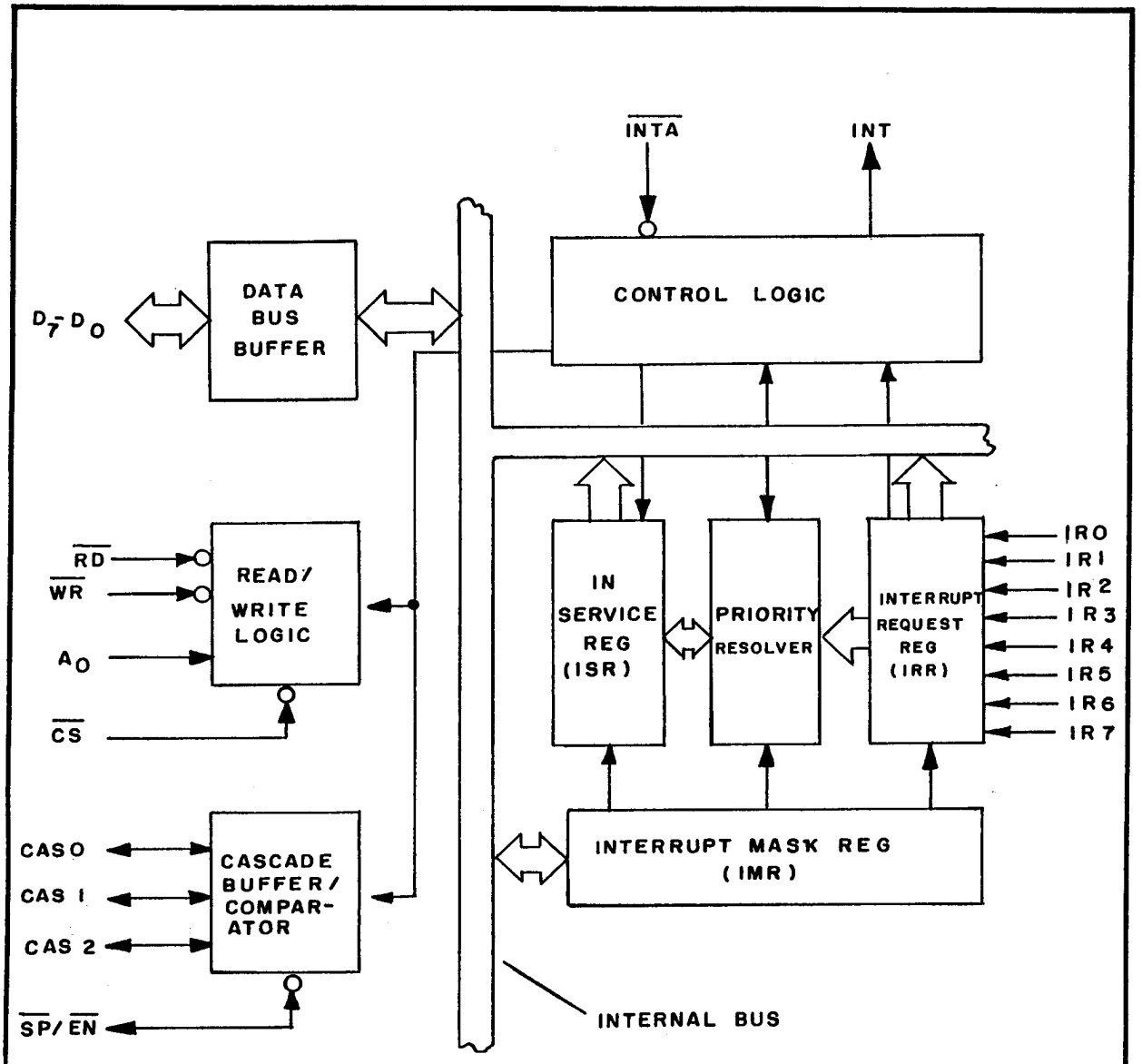



FIGURE 2. Logic diagram.

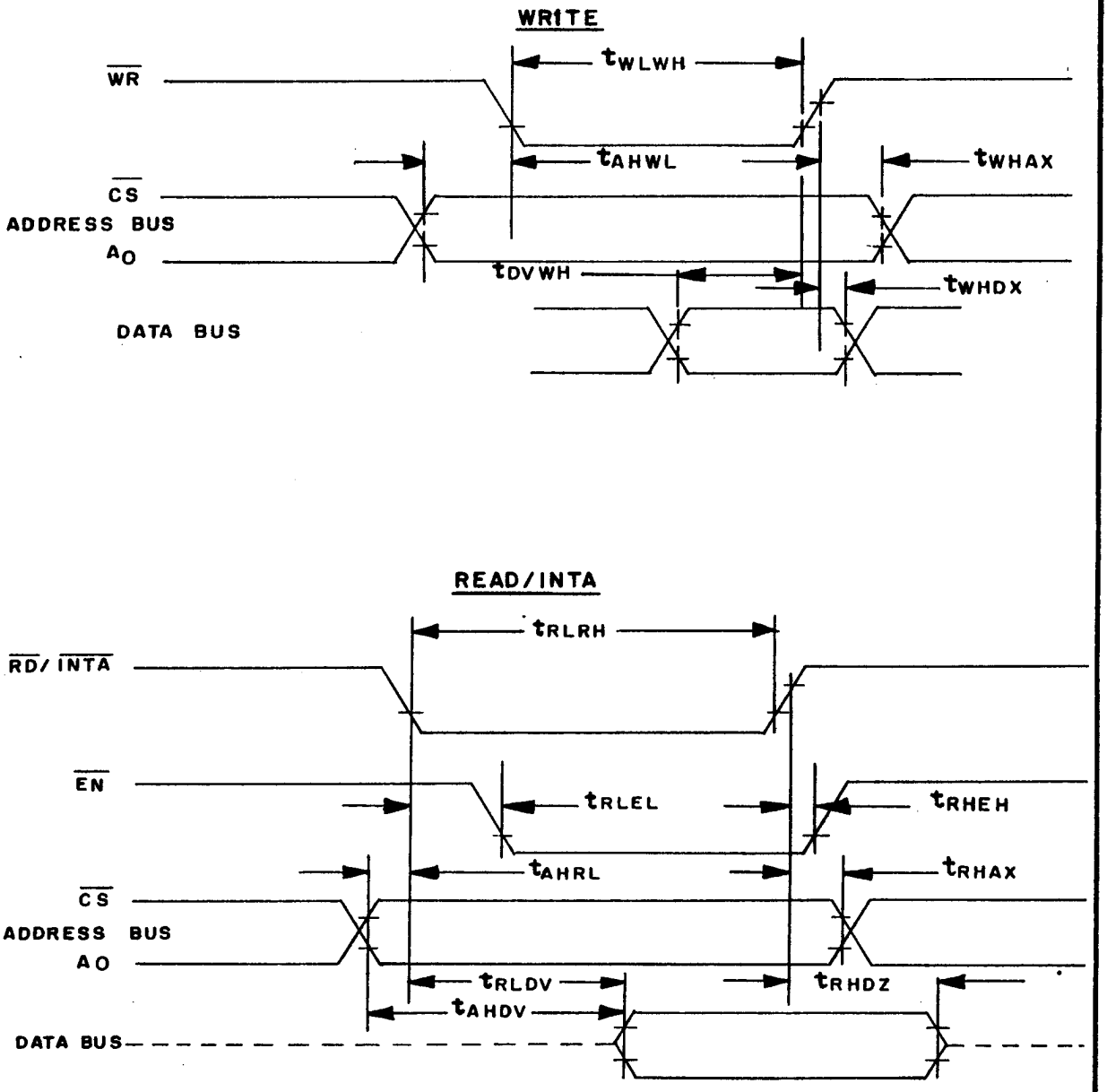
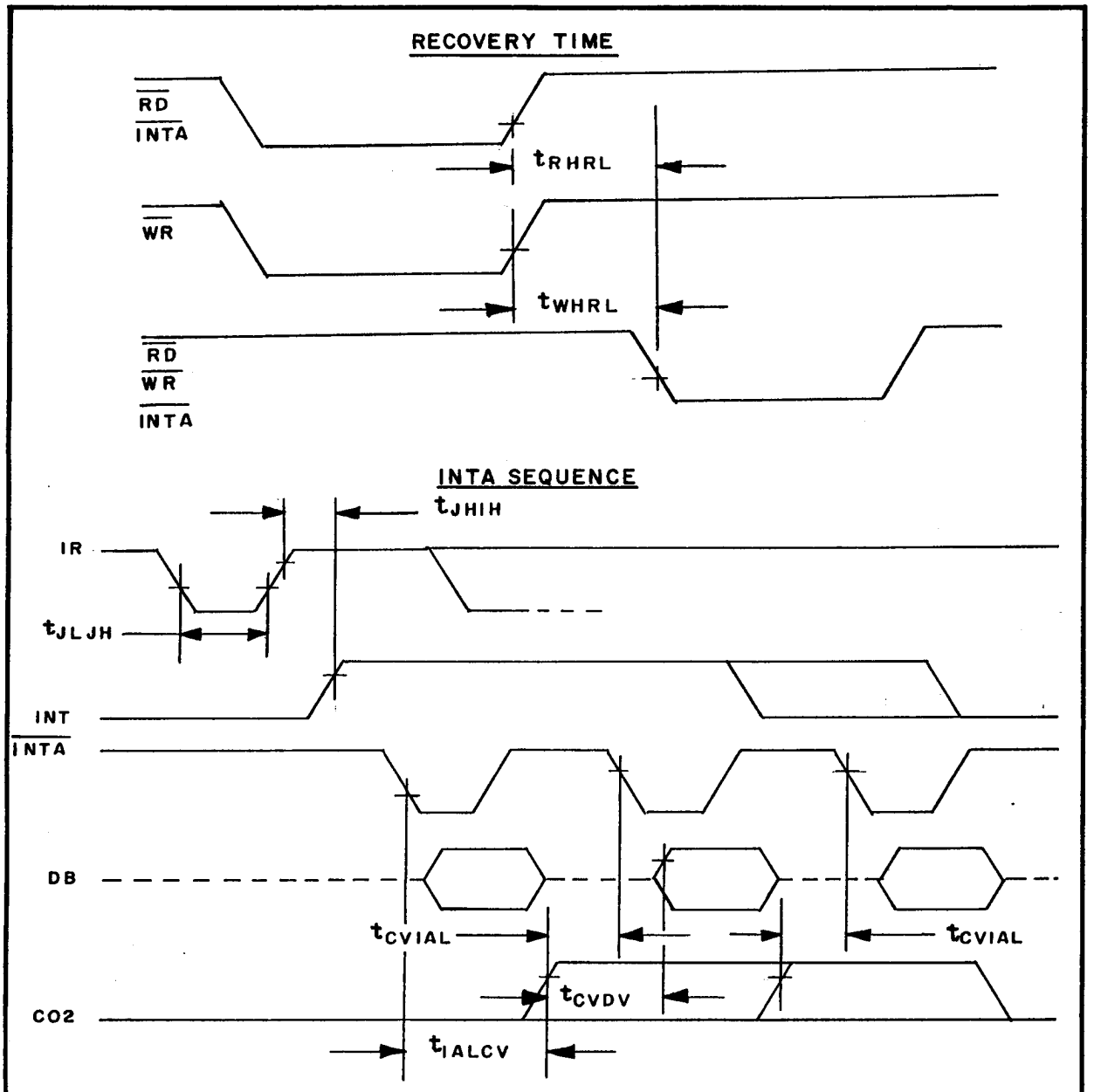
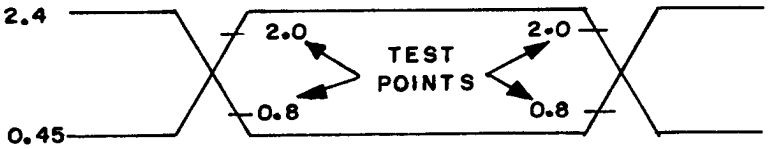



FIGURE 3. Switching waveforms.



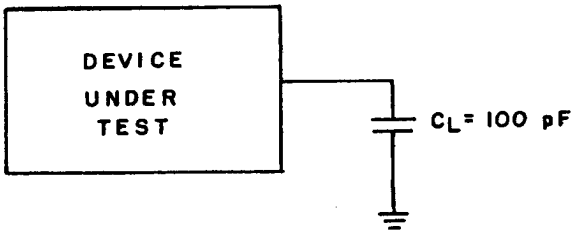

NOTES:
1. Interrupt output must remain HIGH at least until leading edge of first $\overline{\text{INTA}}$.
2. Cycle 1 in iAPX86, iAPX88 systems, the data bus is not active.

FIGURE 3. Switching waveforms - Continued.




NOTES:
1. AC testing inputs are driven at 2.4 V for a logic "1" and 0.45 V for a logic "0".
2. Timing measurements are made at 2.0 V for a logic "1" and 0.8 V for a logic "0".

FIGURE 4. Switching test input/output waveform.




NOTE: $C_L$ includes jig capacitance.

FIGURE 5. Switching test load circuit.

4.3.2 Groups C and D inspections.

a. End-point electrical parameters shall be as specified in table II herein.

b. Steady-state life test conditions, method 1005 of MIL-STD-883.

(1) Test condition C or D using the circuit submitted with the certificate of compliance (see 3.5 herein).

(2) $T_A$ = +125°C, minimum.

(3) Test duration: 1,000 hours, except as permitted by method 1005 of MIL-STD-883.

TABLE II. Electrical test requirements.

| MIL-STD-883 test requirements | Subgroups (per method 5005, table I) |
|---|---|
| Initial electrical parameters (method 5004) | --- |
| Final electrical test parameters (method 5004) | 1*, 2, 3, 7, 8, 9, 10, 11 |
| Group A test requirements (method 5005) | 1, 2, 3, 4, 7, 8, 9, 10, 11 |
| Groups C and D end-point electrical parameters (method 5005) | 2, 8A, 10 |

* PDA applies to subgroup 1.

5. PACKAGING

5.1 Packaging requirements. The requirements for packaging shall be in accordance with MIL-M-38510.

6. NOTES

6.1 Intended use. Microcircuits conforming to this drawing are intended for use when military specifications do not exist and qualified military devices that will perform the required function are not available for OEM application. When a military specification exists and the product covered by this drawing has been qualified for listing on QPL-38510, the device specified herein will be inactivated and will not be used for new design. The QPL-38510 product shall be the preferred item for all applications.

6.2 Replaceability. Microcircuits covered by this drawing will replace the same generic device covered by a contractor-prepared specification or drawing.

6.3 Pin description.

| Pin no. | Name | I/O | Description |
|---|---|---|---|
| 28 | $V_{CC}$ | | Power: +5 V supply. |
| 14 | GND | | Ground. |
| 1 | $\overline{CS}$ | I | Chip select: A low on this pin enables $\overline{RD}$ and $\overline{WR}$ communication between the CPU and the device. INTA functions are independent of $\overline{CS}$. |
| 2 | $\overline{WR}$ | I | Write: A low on this pin when $\overline{CS}$ is low enables the device to accept command words from the CPU. |
| 3 | $\overline{RD}$ | I | Read: A low on this pin when $\overline{CS}$ is low enables the device to release status onto the data bus for the CPU. |
| 4-11 | $D_7$-$D_0$ | I/O | Bidirectional data bus: Control status and interrupt-vector information are transferred via the bus. |
| 12,13,15 | CAS 0-CAS 2 | I/O | Cascade lines: The CAS lines form a private device bus to control a multiple device structure. These pins are outputs for a master device and inputs for a slave device. |
| 16 | $\overline{SP}/\overline{EN}$ | I/O | Slave program/enable buffer. This is a dual function pin. When in the buffered mode, it can be used as an output to control buffer transceivers ($\overline{EN}$). When not in the buffered mode, it is used as an input to designate as a master (SP = 1) or slave (SP = 0). |
| 17 | INT | O | Interrupt: This pin goes high whenever a valid interrupt request is asserted. It is used to interrupt the CPU, thus it is connected to the CPU's interrupt pin. |
| 18-25 | IR0-IR7 | I | Interrupt requests: Asynchronous inputs. An interrupt request is executed by raising an IR input (low to high), and holding it high until it is acknowledged (edge triggered mode), or just by a high level on an IR input (level triggered mode). |

| Pin no. | Name | I/O | Description |
|---|---|---|---|
| 26 | $\overline{INTA}$ | I | Interrupt acknowledge: This pin is used to enable device interrupt-vector data onto the data bus by a sequence of interrupt acknowledge pulses issued by the CPU. |
| 27 | $A_0$ | I | $A_0$ address line: This pin acts in conjunction with the $\overline{CS}$, $\overline{WR}$, and $\overline{RD}$ pins. It is used by the device to decipher various command words the CPU writes and status the CPU wishes to read. It is typically connected to the CPU $A_0$ address line ($A_1$ for iAPX 86, 88). |

6.4 Comments. Comments on this drawing should be directed to DESC-ECS, Dayton, Ohio 45444, or telephone 513-296-5375.

6.5 Approved source of supply. An approved source of supply is listed herein. Additional sources will be added as they become available. The vendor listed herein has agreed to this drawing and a certificate of compliance (see 3.5 herein) has been submitted to DESC-ECS.

| Military drawing part number | Vendor CAGE number | Vendor similar part number 1/ |
|---|---|---|
| 5962-8751801XX | 34649 | MD8259A/B |
| 5962-87518013X | 34649 | MR8259A/B |

1/ Caution. Do not use this number for item acquisition. Items acquired to this number may not satisfy the performance requirements of this drawing.

| Vendor CAGE number | Vendor name and address |
|---|---|
| 34649 | Intel Corporation<br>5000 W Williams Field Road<br>Chandler, AZ 85224 |