REVISIONS			
LTR	DESCRIPTION	DATE (YR-MO-DA)	APPROVED

REV																								
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REV STATUS OF SHEETS	REV																							
	SHEET	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20			

PMIC N/A

STANDARDIZED MILITARY DRAWING

THIS DRAWING IS AVAILABLE FOR USE BY ALL DEPARTMENTS AND AGENCIES OF THE DEPARTMENT OF DEFENSE

AMSC N/A

PREPARED BY: Rick C. Officer

CHECKED BY: Charles Reusing

APPROVED BY: Michael A. Frye

DRAWING APPROVAL DATE: 03 MAY 1988

REVISION LEVEL:

DEFENSE ELECTRONICS SUPPLY CENTER
DAYTON, OHIO 45444

MICROCIRCUIT DIGITAL, BIPOLAR PROGRAMMABLE LOGIC, MONOLITHIC SILICON

SIZE	CAGE CODE	
A	67268	5962-87530

SHEET 1 OF 21

DESC FORM 193
SEP 87

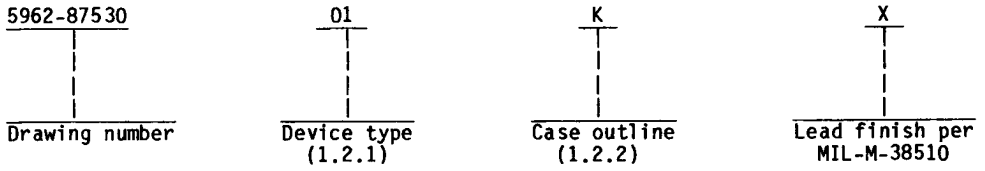
* U.S. GOVERNMENT PRINTING OFFICE: 1987 — 748-129/60911

5962-E290

1. SCOPE

1.1 Scope. This drawing describes device requirements for class B microcircuits in accordance with 1.2.1 of MIL-STD-883, "Provisions for the use of MIL-STD-883 in conjunction with compliant non-JAN devices".

1.2 Part number. The complete part number shall be as shown in the following example:



1.2.1 Device types. The device types shall identify the circuit function as follows:

Device type	Generic number	Circuit function
01	See 6.4	20-Input, 10-Output AND-OR Gate Array with Product Term Sharing.
02	See 6.4	20-Input, 10-Output Registered AND-OR Gate Array with Product Term Sharing.
03	See 6.4	20-Input, 8-Output Registered AND-OR Gate Array with Product Term Sharing.
04	See 6.4	20-Input, 4-Output Registered AND-OR Gate Array with Product Term Sharing.

1.2.2 Case outlines. The case outlines shall be as designated in appendix C of MIL-M-38510, and as follows:

Outline letter	Case outline
K	F-6 (24-lead, 0.640" x 0.420" x 0.090"), flat package
L	D-9 (24-lead, 1.280" x 0.310" x 0.200"), dual-in-line package
3	C-4 (28-terminal, 0.460" sq x 0.100"), square chip carrier package

1.3 Absolute maximum ratings. 1/

Supply voltage range	-0.5 V dc to +7.0 V dc
Storage temperature range	-65°C to +150°C
Maximum power dissipation (P_D) 2/	1.3 W
Lead temperature (soldering, 10 seconds)	260°C
Junction temperature (T_J)	+175°C
Thermal resistance, junction-to-case (θ_{JC}):	
Cases K, L, and 3	See MIL-M-38510, appendix C
Input voltage range	-1.5 V dc to +5.5 V dc
Off-state output voltage, maximum	-0.5 V to +5.5 V

1.4 Recommended operating conditions.

Supply voltage (V_{CC})	4.5 V dc to 5.5 V dc
Case operating temperature (T_C)	-55°C to +125°C
Minimum high-level input voltage (V_{IH})	$\geq$ 2.0 V dc
Maximum low-level input voltage (V_{IL})	$\leq$ 0.8 V dc

1/ Unless otherwise specified, all voltages are referenced to ground.
2/ Must withstand the added P_D due to short circuit test; e.g., I_{OS}.

2. APPLICABLE DOCUMENTS

2.1 Government specification and standard. Unless otherwise specified, the following specification and standard, of the issue listed in that issue of the Department of Defense Index of Specifications and Standards specified in the solicitation, form a part of this drawing to the extent specified herein.

SPECIFICATION

MILITARY

MIL-M-38510 - Microcircuits, General Specification for.

STANDARD

MILITARY

MIL-STD-883 - Test Methods and Procedures for Microelectronics.

(Copies of the specification and standard required by manufacturers in connection with specific acquisition functions should be obtained from the contracting activity or as directed by the contracting activity.)

2.2 Order of precedence. In the event of a conflict between the text of this drawing and the references cited herein, the text of this drawing shall take precedence.

3. REQUIREMENTS

3.1 Item requirements. The individual item requirements shall be in accordance with 1.2.1 of MIL-STD-883, "Provisions for the use of MIL-STD-883 in conjunction with compliant non-JAN devices" and as specified herein.

3.2 Design, construction, and physical dimensions. The design, construction, and physical dimensions shall be as specified in MIL-M-38510 and herein.

3.2.1 Terminal connections. The terminal connections shall be as specified on figure 1.

3.2.2 Truth table.

3.2.2.1 Unprogrammed devices. The truth table for unprogrammed devices for contracts involving no altered item drawing shall be as specified on figure 2. When required in groups A, B, or C (see 4.3), the devices shall be programmed by the manufacturer prior to test in a checkerboard pattern (a minimum of 50 percent of the total number of gates programmed) or to any altered item drawing pattern which includes at least 25 percent of the total number of gates programmed.

3.2.2.2 Programmed devices. The truth table for programmed devices shall be as specified by an attached altered item drawing.

3.2.3 Logic diagrams. The logic diagrams shall be as specified on figure 3.

3.2.4 Case outlines. The case outlines shall be in accordance with 1.2.2 herein.

3.3 Electrical performance characteristics. Unless otherwise specified, the electrical performance characteristics are as specified in table I and apply over the full case operating temperature range.

3.4 Marking. Marking shall be in accordance with MIL-STD-883 (see 3.1 herein). The part shall be marked with the part number listed in 1.2 herein. In addition, the manufacturer's part number may also be marked as listed in 6.4 herein.

TABLE I. Electrical performance characteristics.

Test	Symbol	Conditions 1/ $-55°C \le T_C \le +125°C$	Device types	Group A subgroups	Limits		Unit
					Min	Max	
High level output voltage	V_{OH}	V_{CC} = 4.5 V; I_{OH} = -2 mA V_{IL} = 0.8 V, V_{IH} = 2 V	All	1,2,3	2.4		V
Low level output voltage	V_{OL}	V_{CC} = 4.5 V; I_{OL} = 12 mA V_{IL} = 0.8 V, V_{IH} = 2 V	All	1,2,3		0.5	V
Input clamp voltage	V_{IC}	V_{CC} = 4.5 V; I_I = -18 mA	All	1,2,3		-1.5	V
Low level input current	I_{IL}	V_{CC} = 5.5 V; V_{IL} = 0.4 V 2/	All	1,2,3		-0.25	mA
High level input current	I_{IH}	V_{CC} = 5.5 V; V_{IH} = 2.4 V 2/	All	1,2,3		25	µA
Maximum input current	I_I	V_{CC} = 5.5 V; V_I = 5.5 V	All	1,2,3		1	mA
Output short circuit current 3/	I_{OS}	V_{CC} = 5.5 V; V_O = 0.5 V $V_{IL} \le$ 0.8 V, $V_{IH} \ge$ 2 V	All	1,2,3	-30	-130	mA
Supply current	I_{CC}	V_{CC} = 5.5 V	All	1,2,3		240	mA
Off-state-output current	I_{OZL} 2/	V_{CC} = 5.5 V; V_O = 0.4 V $V_{IL} \le$ 0.8 V, $V_{IH} \ge$ 2.0 V	All	1,2,3		-100	µA
	I_{OZH} 2/	V_{CC} = 5.5 V; V_O = 2.4 V $V_{IL} \le$ 0.8 V, $V_{IH} \ge$ 2.0 V	All	1,2,3		100	µA
Clock to output or feedback	t_{CLK}	R_1 = 390Ω, R_2 = 750Ω V_{IL} = 0 V, V_{IH} = 3 V C_L = 50 pF See figures 4 and 5	02,03, 04	9,10,11		20	ns
Propagation delay high impedance to output high ($\overline{OE}$ to output enabled)	t_{PZH}		02,03, 04	9,10,11		25	ns
Propagation delay high impedance to output low ($\overline{OE}$ to output enabled)	t_{PZL}		02,03, 04	9,10,11		25	ns

See footnotes at end of table.

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TABLE I. Electrical performance characteristics - Continued.

Test	Symbol	Conditions 1/ $-55°C \le T_C \le +125°C$	Device types	Group A subgroups	Limits Min	Limits Max	Unit
Propagation delay output high to high impedance ($\overline{OE}$ to output disabled) 4/	t_{PHZ}	See figures 4 and 5	02,03, 04	9,10,11		25	ns
Propagation delay output low to high impedance ($\overline{OE}$ to output disabled) 4/	t_{PLZ}		02,03, 04	9,10,11		25	ns
Propagation delay high impedance to output high	t_{PZH}	See figures 4 and 5 C_L = 50 pF	01,03, 04	9,10,11		35	ns
Propagation delay high impedance to output low	t_{PZL}	See figures 4 and 5 C_L = 50 pF	01,03, 04	9,10,11		35	ns
Propagation delay output high to high impedance 4/	t_{PHZ}	See figures 4 and 5	01,03, 04	9,10,11		30	ns
Propagation delay output low to high impedance 4/	t_{PLZ}	See figures 4 and 5	01,03, 04	9,10,11		30	ns
Maximum frequency 5/	f_{max}	See figures 4 and 5 C_L = 50 pF	02,03, 04	9,10,11	18		MHz
Propagation delay input to output Fuse intact	t_{PLH}, t_{PHL}	See figures 4 and 5 C_L = 50 pF	01,03, 04	9,10,11		40	ns
Fuse blown	t_{PLH}, t_{PHL}		01,03, 04	9,10,11		45	ns

See footnotes at end of table.

TABLE I. Electrical performance characteristics - Continued.

Test	Symbol	Conditions 1/ $-55°C \le T_C \le +125°C$	Device types	Group A subgroups	Limits		Unit
					Min	Max	
Minimum clock pulse width 5/	$t_{p(CL)}$	See figures 4 and 5 C_L = 50 pF	02,03, 04	9,10,11	20		ns
Minimum setup time 5/	t_{su}	See figures 4 and 5 C_L = 50 pF	02,03, 04	9,10,11	40		ns
Minimum hold time 5/	t_H	See figures 4 and 5 C_L = 50 pF	02,03, 04	9,10,11	0		ns

1/ Unless otherwise specified V_{CC} is 4.5 V to 5.5 V.

2/ I/O terminal leakage is the worst case of I_{IX} or I_{OZX}.

3/ Only one output shorted at a time.

4/ C_L = 5 pF.

5/ Tested only initially and after any design change.

3.5 Processing options. Since the device is capable of being programmed by either the manufacturer or the user to result in a wide variety of configurations, two processing options are provided for selection in the contract, using an altered item drawing.

3.5.1 Unprogrammed device delivered to the user. All testing shall be verified through group A testing as defined in 3.2.2.1 and table II. It is recommended that users perform subgroups 7 and 9 after programming to verify the specific program configuration.

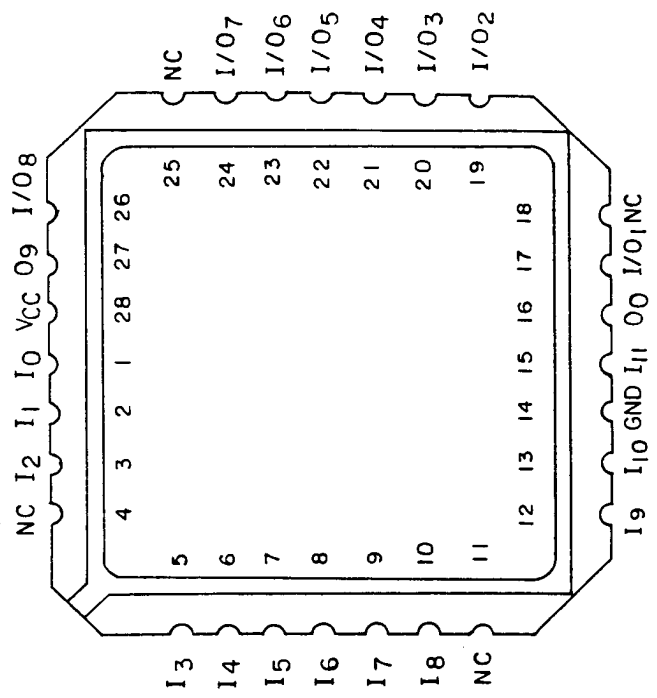
3.5.2 Manufacturer-programmed device delivered to the user. All testing requirements and quality assurance provisions herein, including the requirements of the altered item drawing, shall be satisfied by the manufacturer prior to delivery.

3.6 Certificate of compliance. A certificate of compliance shall be required from a manufacturer in order to be listed as an approved source of supply in 6.4. The certificate of compliance submitted to DESC-ECS prior to listing as an approved source of supply shall state that the manufacturer's product meets the requirements of MIL-STD-883 (see 3.1 herein) and the requirements herein.

3.7 Certificate of conformance. A certificate of conformance as required in MIL-STD-883 (see 3.1 herein) shall be provided with each lot of microcircuits delivered to this drawing.

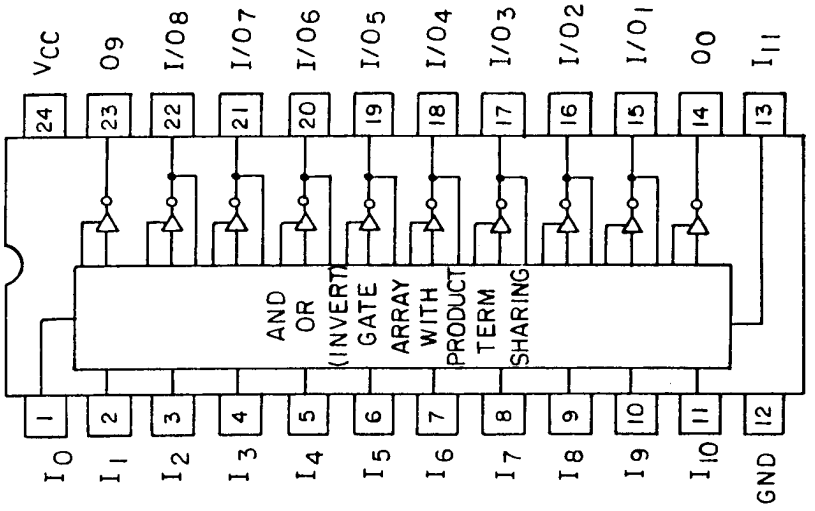
3.8 Notification of change. Notification of change to DESC-ECS shall be required in accordance with MIL-STD-883 (see 3.1 herein).

Device type 01



Case outline 3

Device type 01

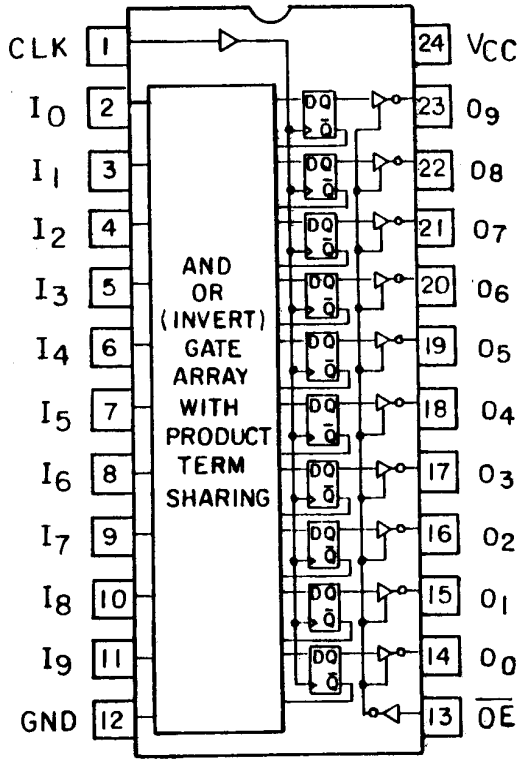


Case outlines K and L

FIGURE 1. Terminal connections.

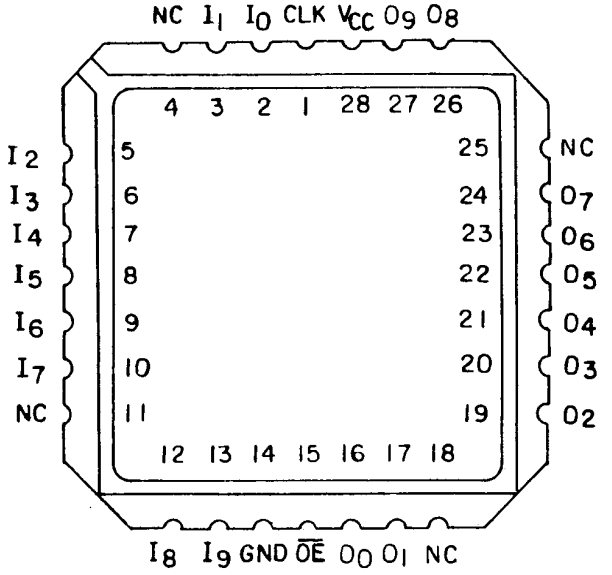
STANDARDIZED MILITARY DRAWING DEFENSE ELECTRONICS SUPPLY CENTER DAYTON, OHIO 45444	SIZE A		5962-87530
		REVISION LEVEL	SHEET 7

Device type 02



Case outlines K and L

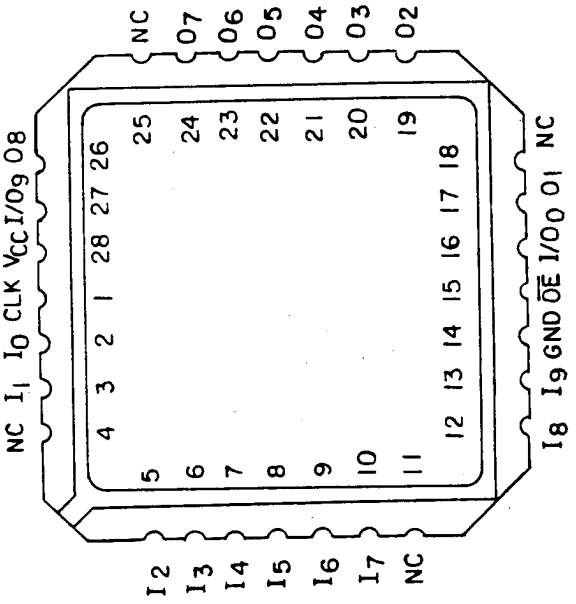
Device type 02



Case outline 3

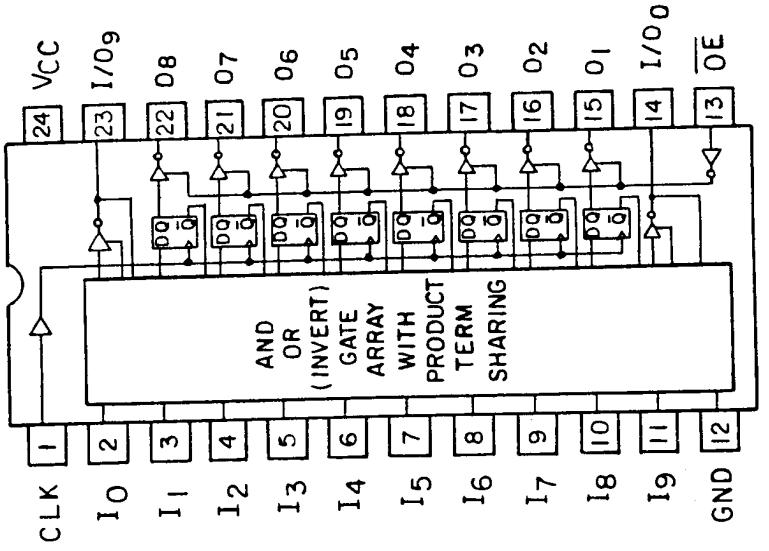
FIGURE 1. Terminal connections - Continued.

Device type 03



Case outline 3

Device type 03

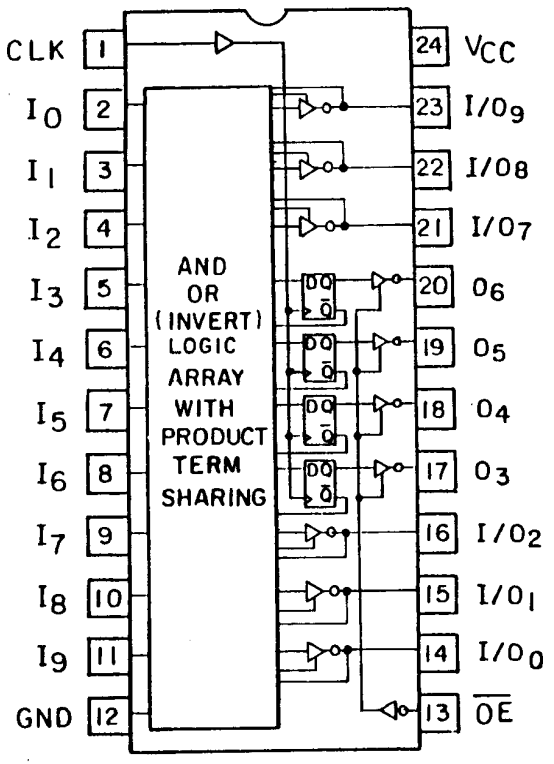


Case outlines K and L

FIGURE 1. Terminal connections - Continued.

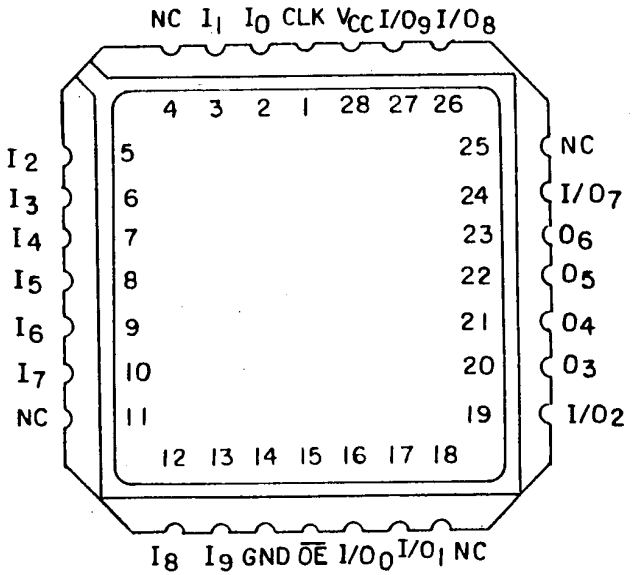
STANDARDIZED MILITARY DRAWING DEFENSE ELECTRONICS SUPPLY CENTER DAYTON, OHIO 45444	SIZE A		5962-87530
		REVISION LEVEL	SHEET 9

Device type 04



Case outlines K and L

Device type 04



Case outline 3

FIGURE 1. Terminal connections - Continued.

Device type	CLK	$\overline{OE}$	I_0	I_1	I_2	I_3	I_4	I_5	I_6	I_7	I_8	I_9	I_{10}	I_{11}
01	--	--	X	X	X	X	X	X	X	X	X	X	X	X
02	CLK	L	X	X	X	X	X	X	X	X	X	X	--	--
03	CLK	L	X	X	X	X	X	X	X	X	X	X	--	--
04	CLK	L	X	X	X	X	X	X	X	X	X	X	--	--

Device type	O_0	O_1	O_2	O_3	O_4	O_5	O_6	O_7	O_8	O_9	O_{10}
01	Z	Z	Z	Z	Z	Z	Z	Z	Z	Z	--
02	H	H	H	H	H	H	H	H	H	H	--
03	Z	H	H	H	H	H	H	H	H	H	--
04	Z	Z	Z	H	H	H	H	H	Z	Z	--

L = Low logic state
H = High logic state
Z = High impedence state
X = Don't care

FIGURE 2. Truth table, unprogrammed.

Device type 01

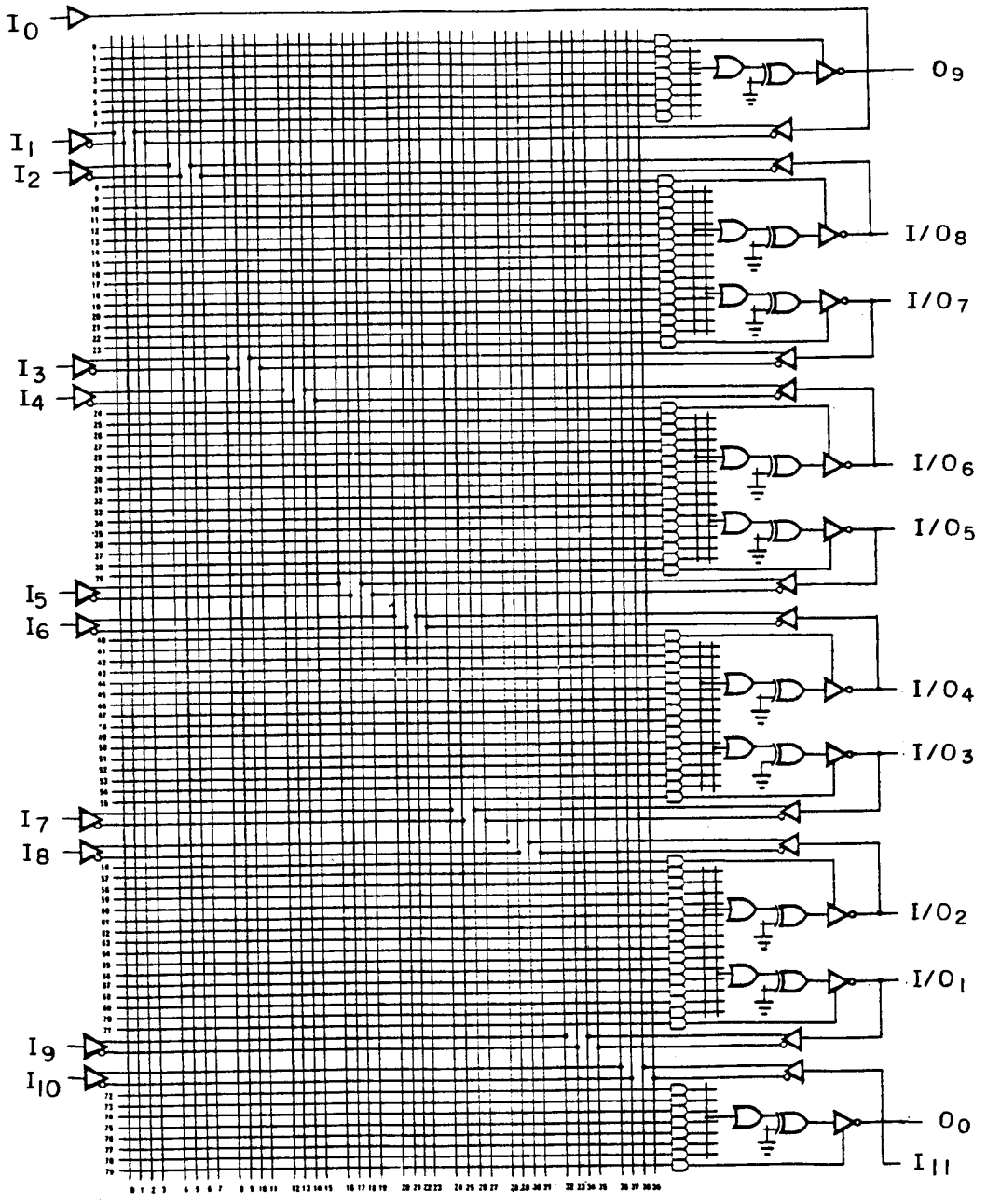


FIGURE 3. Logic diagrams.

Device type 02

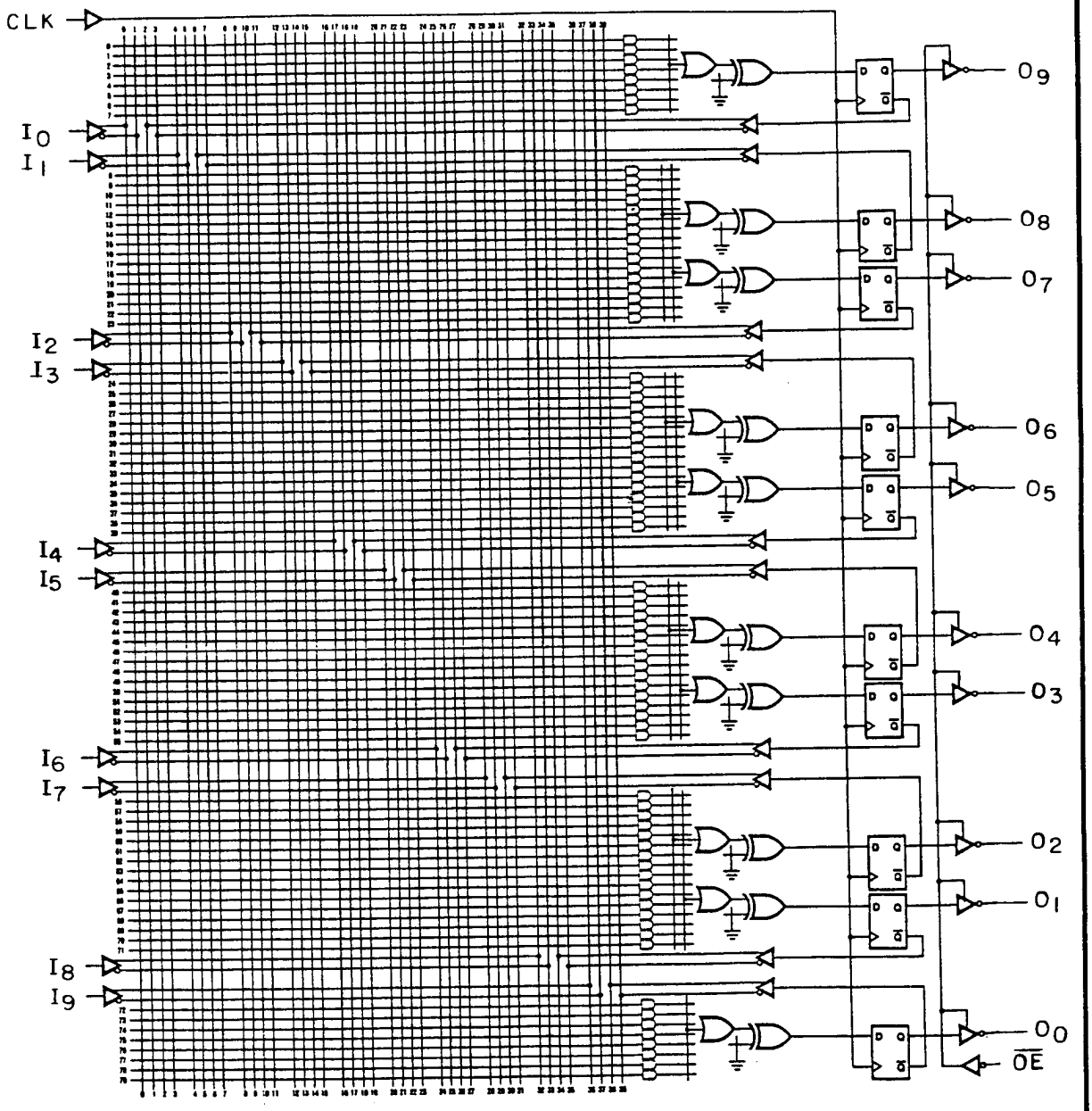


FIGURE 3. Logic diagrams - Continued.

Device type 03

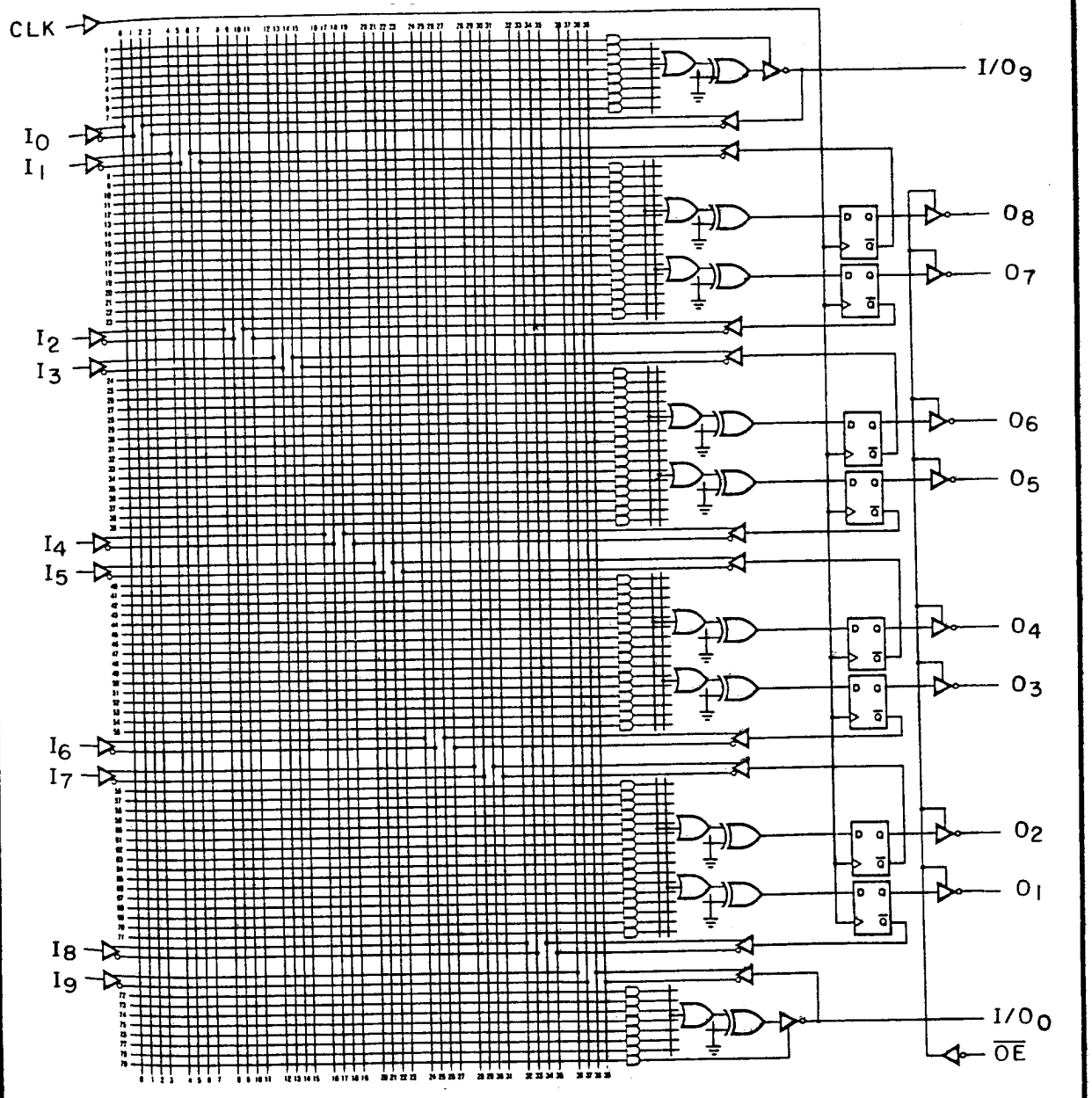


FIGURE 3. Logic diagrams - Continued.

Device type 04

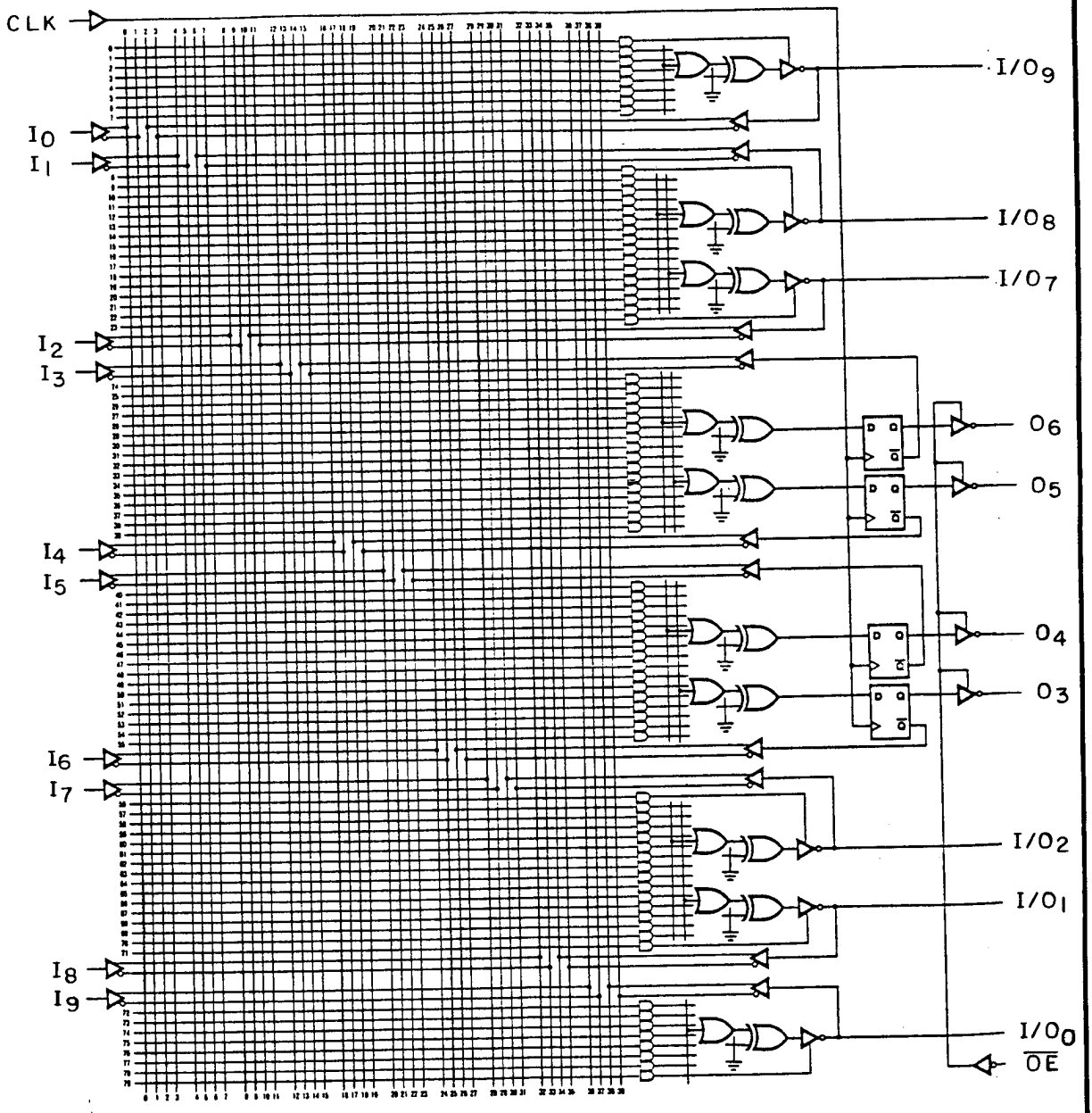


FIGURE 3. Logic diagrams - Continued.

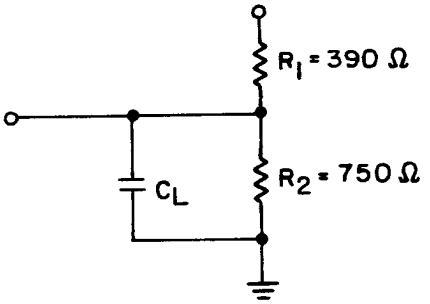
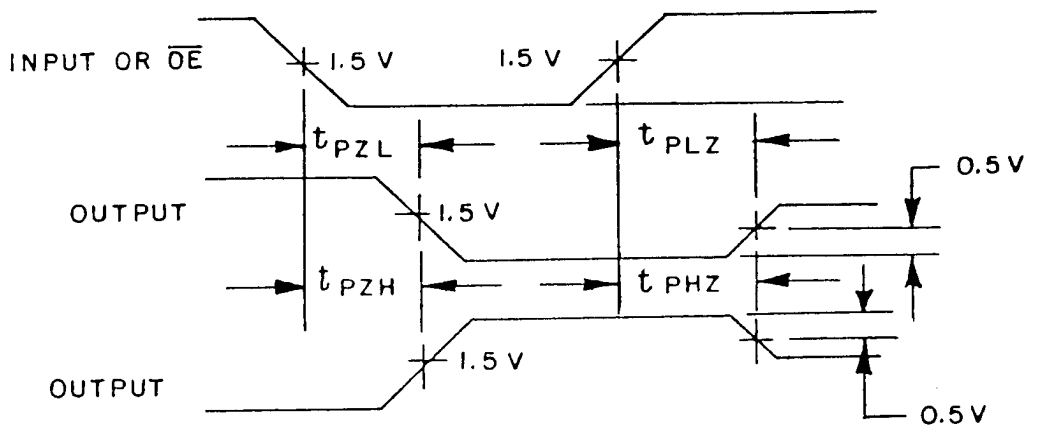
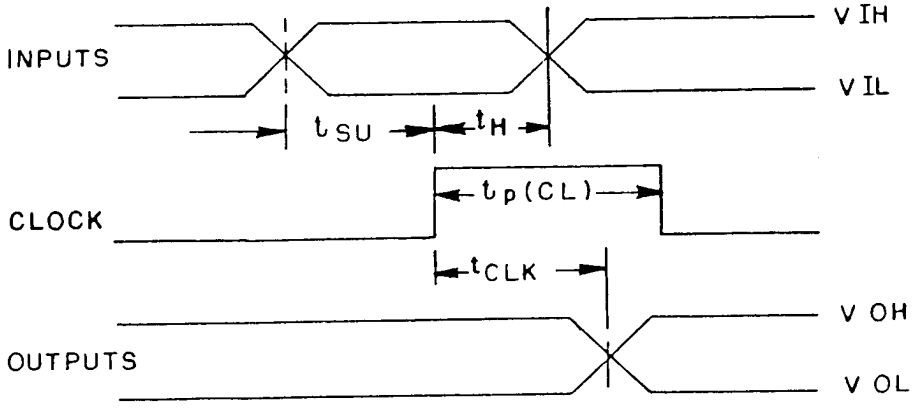


FIGURE 4. Output load circuit.

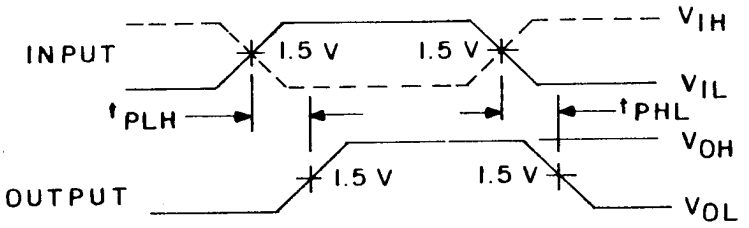


INPUT OR $\overline{OE}$ SWITCHING WAVEFORM



REGISTERED SWITCHING WAVEFORM

FIGURE 5. Switching waveforms.



NON-REGISTERED SWITCHING WAVEFORMS

FIGURE 5. Switching waveforms - Continued.

3.9 Verification and review. DESC, DESC's agent, and the acquiring activity retain the option to review the manufacturer's facility and applicable required documentation. Offshore documentation shall be made available onshore at the option of the reviewer.

4. QUALITY ASSURANCE PROVISIONS

4.1 Sampling and inspection. Sampling and inspection procedures shall be in accordance with section 4 of MIL-M-38510 to the extent specified in MIL-STD-883 (see 3.1 herein).

4.2 Screening. Screening shall be in accordance with method 5004 of MIL-STD-883, and shall be conducted on all devices prior to quality conformance inspection. The following additional criteria shall apply:

a. Burn-in test (method 1015 of MIL-STD-883).

(1) Test condition C or D using the circuit submitted with the certificate of compliance (see 3.5 herein).

(2) T_A = +125°C, minimum.

b. Interim and final electrical test parameters shall be as specified in table II herein, except interim electrical parameter tests prior to burn-in are optional at the discretion of the manufacturer.

4.3 Quality conformance inspection. Quality conformance inspection shall be in accordance with method 5005 of MIL-STD-883 including groups A, B, C, and D inspections. The following additional criteria shall apply.

4.3.1 Group A inspection.

a. Tests shall be as specified in table II herein.

b. Subgroups 4, 5, and 6 in table I, method 5005 of MIL-STD-883 shall be omitted.

c. Unprogrammed devices shall be tested for programmability and ac performance compliance to the requirements of group A, subgroups 9, 10, and 11. Either of two techniques is acceptable:

(1) Testing the entire lot using additional built-in test circuitry which allows the manufacturer to verify programmability and ac performance without programming the user array. If this is done, the resulting test patterns shall be verified on all devices during subgroups 9, 10, and 11, group A testing in accordance with the sampling plan specified in MIL-STD-883, method 5005.

(2) If such compliance cannot be tested on an unprogrammed device, a sample shall be selected to satisfy programmability requirements prior to performing subgroups 9, 10, and 11. Twelve devices shall be submitted to programming (see 3.2.2.1). If more than two devices fail to program, the lot shall be rejected. At the manufacturer's option, the sample may be increased to twenty-four total devices with no more than four total device failures allowable.

d. Ten devices from the programmability sample shall be submitted to the requirements of group A, subgroups 9, 10, and 11. If more than two total devices fail, the lot shall be rejected. At the manufacturer's option, the sample may be increased to twenty total devices with no more than four total device failures allowable.

4.3.2 Groups C and D inspections.

a. End-point electrical parameters shall be as specified in table II herein.

b. Steady-state life test (method 1005 of MIL-STD-883) conditions:

(1) Test condition C or D using the circuit submitted with the certificate of compliance (see 3.5 herein).

(2) T_A = +125°C, minimum.

(3) Test duration: 1,000 hours, except as permitted by method 1005 of MIL-STD-883.

4.4 Programming procedures. The programming procedures shall be as specified by the device manufacturer.

TABLE II. Electrical test requirements. 1/ 2/ 3/

MIL-STD-883 test requirements	Subgroups (per method 5005, table I)
Interim electrical parameters (method 5004)	1
Final electrical test parameters (method 5004) for unprogrammed devices	1*,2,3,7*,8
Final electrical test parameters (method 5004) for programmed devices	1*,2,3,7*,8,9
Group A test requirements (method 5005)	1,2,3,7,8,9,10,11
Groups C and D end-point electrical parameters (method 5005)	1,2,3

1/ (*) indicates PDA applies to subgroups 1 and 7.
2/ Any or all subgroups may be combined when using high-speed testers.
3/ Subgroups 7 and 8 functional tests shall verify that no fuses are blown for unprogrammed devices or that the altered item drawing pattern exists for programmed devices.

5. PACKAGING

5.1 Packaging requirements. The requirements for packaging shall be in accordance with MIL-M-38510.

6. NOTES

6.1 Intended use. Microcircuits conforming to this drawing are intended for use when military specifications do not exist and qualified military devices that will perform the required function are not available for OEM application. When a military specification exists and the product covered by this drawing has been qualified for listing on QPL-38510, the device specified herein will be inactivated and will not be used for new design. The QPL-38510 product shall be the preferred item for all applications.

6.2 Replaceability. Microcircuits covered by this drawing will replace the same generic device covered by a contractor-prepared specification or drawing.

6.3 Comments. Comments on this drawing should be directed to DESC-ECS, Dayton, Ohio 45444, or telephone 513-296-5375.

6.4 Approved source of supply. An approved source of supply is listed herein. Additional sources will be added as they become available. The vendor listed herein has agreed to this drawing and a certificate of compliance (see 3.5 herein) has been submitted to DESC-ECS.

Military drawing part number	Vendor CAGE number	Vendor 1/ similar part number	Replacement military specification part number
5962-8753001LX	50364	PAL20S10MJS/883B	
5962-8753001KX	50364	PAL20S10MW/883B	
5962-87530013X	50364	PAL20S10ML/883B	
5962-8753002LX	50364	PAL20RS10MJS/883B	
5962-8753002KX	50364	PAL20RS10MW/883B	
5962-87530023X	50364	PAL20RS10ML/883B	
5962-8753003LX	50364	PAL20RS8MJS/883B	
5962-8753003KX	50364	PAL20RS8MW/883B	
5962-87530033X	50364	PAL20RS8ML/883B	
5962-8753004LX	50364	PAL20RS4MJS/883B	
5962-8753004KX	50364	PAL20RS4MW/883B	
5962-87530043X	50364	PAL20RS4ML/883B	

1/ Caution. Do not use this number for item acquisition. Items acquired to this number may not satisfy the performance requirements of this drawing.

Vendor CAGE number	Vendor name and address
50364	Monolithic Memories, Incorporated 2175 Mission College Boulevard Santa Clara, CA 95051

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