REVISIONS			
LTR	DESCRIPTION	DATE (YR-MO-DA)	APPROVED
A	Add Figure 4. Technical changes in 1.3, 1.4, table I, and Table II. Change vendors similar part number for case outline 2. Editorial changes throughout. mlp	89-08-23	Michael A. Frye
B	Changes in accordance with NOR 5962-R033-92. tvn	91-12-02	Monica L. Poelking
C	Add package CDFP4-F16. Use new boilerplate. ljs	98-02-04	Raymond Monnin
D	Figure 4 modified to be consistent with Table I. ljs	98-08-12	Raymond Monnin

The original first page of this document has been replaced.

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REV STATUS	REV	D	D	D	D	D	D	D	D	D	D	D	D	D					
OF SHEETS	SHEET	1	2	3	4	5	6	7	8	9	10	11	12	13					

PMIC N/A

PREPARED BY
Monica L. Poelking

CHECKED BY
Monica L. Poelking

APPROVED BY
Michael A. Frye

DRAWING APPROVAL DATE
87-10-21

REVISION LEVEL
D

DEFENSE SUPPLY CENTER COLUMBUS
COLUMBUS, OHIO 43216

STANDARD MICROCIRCUIT DRAWING

THIS DRAWING IS AVAILABLE FOR USE BY ALL DEPARTMENTS AND AGENCIES OF THE DEPARTMENT OF DEFENSE

AMSC N/A

MICROCIRCUIT, DIGITAL, ECL, QUAD 2-INPUT NOR GATE, MONOLITHIC SILICON

SIZE	CAGE CODE	
A	67268	5962-87557

SHEET 1 OF 13

DSCC FORM 2233
APR 97

5962-E457-98

DISTRIBUTION STATEMENT A Approved for public release; distribution is unlimited.

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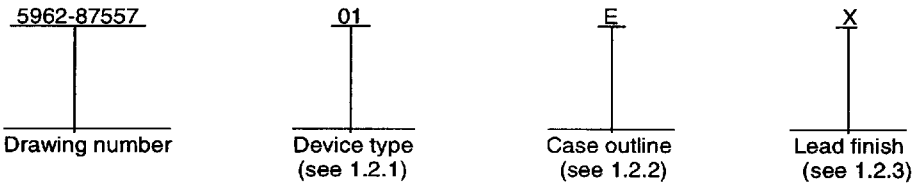
1. SCOPE

1.1 Scope. This drawing describes device requirements for MIL-STD-883 compliant, non-JAN class level B microcircuits in accordance with MIL-PRF-38535, appendix A.

1.2 Part or Identifying Number (PIN). The complete PIN is as shown in the following example:



1.2.1 Device type(s). The device type(s) identify the circuit function as follows:

Device type	Generic number	Circuit function
01	10H502	Quad 2-input NOR gate

1.2.2 Case outline(s). The case outline(s) are as designated in MIL-STD-1835 and as follows:

Outline letter	Descriptive designator	Terminals	Package style
E	GDIP1-T16 or CDIP2-T16	16	Dual -in-line
F	GDFP2-F16 or CDFP3-F16	16	Flat package
X	CDFP4-F16	16	Flat-package
2	CQCC1-N20	20	Square chip carrier

1.2.3 Lead finish. The lead finish is as specified in MIL-PRF-38535, appendix A.

1.3 Absolute maximum ratings.

Supply voltage range (V_{EE})	-8.0 V dc to 0.0 V dc
Input voltage range	-5.2 V dc to 0.0 V dc
Storage temperature range	-65°C to +165°C
Lead temperature (soldering, 10 seconds)	+300°C
Junction temperature (T_J)	+165°C
Maximum power dissipation (P_D) 1/	200 mW
Thermal resistance, junction-to-case (Θ_{JC})	See MIL-STD-1835

1.4 Recommended operating conditions.

Supply voltage range (V_{EE})	-5.46 V dc minimum to -4.94 V dc maximum
Supply voltage range (V_{CC})	-0.02 V dc to 0.02 V dc or 1.98 V dc to 2.02 V dc
Ambient operating temperature range (T_A)	-55°C to +125°C

1/ Must withstand the added P_D due to short circuit test; e.g., I_{OS}.

Minimum high level input voltage (V_{IH}):

T_A = +25°C	-0.780 V dc
T_A = +125°C	-0.650 V dc
T_A = -55°C	-0.840 V dc
Maximum low level input voltage (V_{IL})	-1.950 V dc

2. APPLICABLE DOCUMENTS

2.1 Government specification, standards, and handbooks. The following specification, standards, and handbooks form a part of this drawing to the extent specified herein. Unless otherwise specified, the issues of these documents are those listed in the issue of the Department of Defense Index of Specifications and Standards (DoDISS) and supplement thereto, cited in the solicitation.

SPECIFICATION

DEPARTMENT OF DEFENSE

MIL-PRF-38535 - Integrated Circuits, Manufacturing, General Specification for.

STANDARDS

DEPARTMENT OF DEFENSE

MIL-STD-883 - Test Method Standard Microcircuits.
MIL-STD-973 - Configuration Management.
MIL-STD-1835 - Interface Standard For Microcircuit Case Outlines.

HANDBOOKS

DEPARTMENT OF DEFENSE

MIL-HDBK-103 - List of Standard Microcircuit Drawings (SMD's).
MIL-HDBK-780 - Standard Microcircuit Drawings.

(Unless otherwise indicated, copies of the specification, standards, and handbooks are available from the Standardization Document Order Desk, 700 Robbins Avenue, Building 4D, Philadelphia, PA 19111-5094.)

2.2 Order of precedence. In the event of a conflict between the text of this drawing and the references cited herein, the text of this drawing takes precedence. Nothing in this document, however, supersedes applicable laws and regulations unless a specific exemption has been obtained.

3. REQUIREMENTS

3.1 Item requirements. The individual item requirements shall be in accordance with MIL-PRF-38535, appendix A for non-JAN class level B devices and as specified herein. Product built to this drawing that is produced by a Qualified Manufacturer Listing (QML) certified and qualified manufacturer or a manufacturer who has been granted transitional certification to MIL-PRF-38535 may be processed as QML product in accordance with the manufacturers approved program plan and qualifying activity approval in accordance with MIL-PRF-38535. This QML flow as documented in the Quality Management (QM) plan may make modifications to the requirements herein. These modifications shall not affect form, fit, or function of the device. These modifications shall not affect the PIN as described herein. A "Q" or "QML" certification mark in accordance with MIL-PRF-38535 is required to identify when the QML flow option is used.

3.2 Design, construction, and physical dimensions. The design, construction, and physical dimensions shall be as specified in MIL-PRF-38535, appendix A and herein.

3.2.1 Terminal connections. The terminal connections shall be as specified on figure 1.

3.2.2 Truth table(s). The truth table(s) shall be as specified on figure 2.

3.2.3 Logic diagram(s). The logic diagram(s) shall be as specified on figure 3.

3.2.4 Test circuit and switching waveforms. The test circuit and switching waveforms shall be as specified on figure 4.

3.2.5 Case outlines. The case outlines shall be in accordance with 1.2.2 herein.

3.3 Electrical performance characteristics. Unless otherwise specified herein, the electrical performance characteristics are as specified in table I and shall apply over the full ambient operating temperature range.

3.4 Electrical test requirements. The electrical test requirements shall be the subgroups specified in table II. The electrical tests for each subgroup are described in table I.

3.5 Marking. Marking shall be in accordance with MIL-PRF-38535, appendix A. The part shall be marked with the PIN listed in 1.2 herein. In addition, the manufacturer's PIN may also be marked as listed in MIL-HDBK-103 (see 6.6 herein). For packages where marking of the entire SMD PIN number is not feasible due to space limitations, the manufacturer has the option of not marking the "5962-" on the device.

3.6 Certificate of compliance. A certificate of compliance shall be required from a manufacturer in order to be listed as an approved source of supply in MIL-HDBK-103 (see 6.6 herein). The certificate of compliance submitted to DSCC-VA prior to listing as an approved source of supply shall affirm that the manufacturer's product meets the requirements of MIL-PRF-38535, appendix A and the requirements herein.

3.7 Certificate of conformance. A certificate of conformance as required in MIL-PRF-38535, appendix A shall be provided with each lot of microcircuits delivered to this drawing.

3.8 Notification of change. Notification of change to DSCC-VA shall be required in accordance with MIL-PRF-38535, appendix A.

3.9 Verification and review. DSCC, DSCC's agent, and the acquiring activity retain the option to review the manufacturer's facility and applicable required documentation. Offshore documentation shall be made available onshore at the option of the reviewer.

4. QUALITY ASSURANCE PROVISIONS

4.1 Sampling and inspection. Sampling and inspection procedures shall be in accordance with MIL-PRF-38535, appendix A.

4.2 Screening. Screening shall be in accordance with method 5004 of MIL-STD-883, and shall be conducted on all devices prior to quality conformance inspection. The following additional criteria shall apply:

a. Burn-in test, method 1015 of MIL-STD-883.

(1) Test condition A, B, C or D. The test circuit shall be maintained by the manufacturer under document revision level control and shall be made available to the preparing or acquiring activity upon request. The test circuit shall specify the inputs, outputs, biases, and power dissipation, as applicable, in accordance with the intent specified in test method 1015 of MIL-STD-883.

(2) T_A = +125°C, minimum.

b. Interim and final electrical test parameters shall be as specified in table II herein, except interim electrical parameter tests prior to burn-in are optional at the discretion of the manufacturer.

TABLE I. Electrical performance characteristics.

Test	Symbol	Conditions $-55°C \le T_A \le +125°C$ unless otherwise specified			Group A subgroups	Limits		Unit
						Min	Max	
Cases E, F, 2 and X		Quiescent tests 1/						
			V_{IH}	V_{IL}				
High level output voltage	V_{OH}	Outputs terminated	-0.780	-1.950	1	-1.010	-0.780	V
		through 100Ω	-0.650	-1.950	2	-0.860	-0.650	
		to -2 V	-0.840	-1.950	3	-1.060	-0.840	
Low level output voltage	V_{OL}	V_{CC} = 0.0 V	-0.780	-1.950	1	-1.950	-1.580	V
		V_{EE} = -5.2 V 2/	-0.650	-1.950	2	-1.950	-1.565	
			-0.840	-1.950	3	-1.950	-1.610	
High level threshold output voltage	V_{OHA}		-1.110	-1.480	1	-1.010	-0.780	V
			-0.960	-1.465	2	-0.860	-0.650	
			-1.160	-1.510	3	-1.060	-0.840	
Low level threshold output voltage	V_{OLA}		-1.110	-1.480	1	-1.950	-1.580	V
			-0.960	-1.465	2	-1.950	-1.565	
			-1.160	-1.510	3	-1.950	-1.610	
Power supply drain current 3/	I_{EE}	V_{EE} = -5.46 V V_{CC} = 0.0 V			1 2,3	-26 -29		mA
High level input current	I_{IH}	V_{IH} = -0.780 V at +25°C -0.650 V at +125°C -0.840 V at -55°C			1 2,3		265 425	µA
Low level input current	I_{IL}	V_{EE} = -4.95 V 3/ V_{IL} = -1.950 V V_{CC} = 0.0 V			1,3 2	0.5 0.3		µA
Functional tests		See 4.3.1c			7, 8A, 8B			

See footnotes at end of table.

TABLE I. Electrical performance characteristics - Continued.

Test	Symbol	Conditions $-55°C \le T_A \le +125°C$ unless otherwise specified			Group A subgroups	Limits		Unit
						Min	Max	
Cases E, F and X		Rapid tests 4/						
			V_{IH}	V_{IL}				
High level output voltage	V_{OH}	Outputs terminated	-0.789	-1.950	1	-1.018	-0.789	V
		through 100Ω	-0.659	-1.950	2	-0.869	-0.659	
		to -2 V	-0.849	-1.950	3	-1.069	-0.849	
Low level output voltage	V_{OL}	V_{CC} = 0.0 V	-0.789	-1.950	1	-1.950	-1.583	V
		V_{EE} = -5.2 V 2/	-0.659	-1.950	2	-1.950	-1.568	
			-0.849	-1.950	3	-1.950	-1.613	
High level threshold output voltage	V_{OHA}		-1.118	-1.483	1	-1.018	-0.789	V
			-0.969	-1.468	2	-0.869	-0.659	
			-1.169	-1.513	3	-1.069	-0.849	
Low level threshold output voltage	V_{OLA}		-1.118	-1.483	1	-1.950	-1.583	V
			-0.969	-1.468	2	-1.950	-1.568	
			-1.169	-1.513	3	-1.950	-1.613	
Power supply drain current 3/	I_{EE}	V_{EE} = -5.46 V V_{CC} = 0.0 V			1 2,3	-25 -28		mA
High level input current	I_{IH}	V_{IH} = -0.789 V at +25°C -0.659 V at +125°C -0.849 V at -55°C			1 2,3		250 410	µA
Low level input current	I_{IL}	V_{EE} = -4.94 V 3/ V_{IL} = -1.950 V V_{CC} = 0.0 V			1,3 2	0.5 0.3		µA
Functional tests		See 4.3.1c			7, 8A, 8B			

See footnotes at end of table.

TABLE I. Electrical performance characteristics - Continued.

Test	Symbol	Conditions $-55°C \le T_A \le +125°C$ unless otherwise specified			Group A subgroups	Limits		Unit
						Min	Max	
Case 2		Rapid tests 4/						
			V_{IH}	V_{IL}				
High level output voltage	V_{OH}	Outputs terminated	-0.794	-1.950	1	-1.023	-0.794	V
		through 100Ω	-0.665	-1.950	2	-0.874	-0.665	
		to -2 V	-0.855	-1.950	3	-1.074	-0.855	
Low level output voltage	V_{OL}	V_{CC} = 0.0 V	-0.794	-1.950	1	-1.950	-1.584	V
		V_{EE} = -5.2 V 2/	-0.665	-1.950	2	-1.950	-1.570	
			-0.855	-1.950	3	-1.950	-1.615	
High level threshold output voltage	V_{OHA}		-1.123	-1.484	1	-1.023	-0.794	V
			-0.974	-1.470	2	-0.874	-0.665	
			-1.174	-1.515	3	-1.074	-0.855	
Low level threshold output voltage	V_{OLA}		-1.123	-1.484	1	-1.950	-1.584	V
			-0.974	-1.470	2	-1.950	-1.570	
			-1.174	-1.515	3	-1.950	-1.615	
Power supply drain current 3/	I_{EE}	V_{EE} = -5.46 V V_{CC} = 0.0 V			1 2,3	-25 -28		mA
High level input current	I_{IH}	V_{IH} = -0.794 V at +25°C -0.665 V at +125°C -0.855 V at -55°C			1 2,3		250 410	µA
Low level input current	I_{IL}	V_{EE} = -4.94 V 3/ V_{IL} = -1.950 V V_{CC} = 0.0 V			1,3 2	0.5 0.3		µA
Functional tests		See 4.3.1c			7, 8A, 8B			

See footnotes at end of table.

TABLE I. Electrical performance characteristics - Continued.

Test	Symbol	Conditions $-55°C \le T_A \le +125°C$ unless otherwise specified	Group A subgroups	Limits		Unit
				Min	Max	
Cases E, F, 2 and X		AC tests				
Transition time	t_{TLH}, t_{THL}	V_{EE} = -2.94 V V_{CC} = 2.0 V $C_L \le 5$ pF	9 10 11	0.50 0.55 0.50	1.60 1.70 1.50	ns
Propagation delay time, A, B to Y, $\overline{Y}$	t_{PHH}, t_{PLL}, t_{PLH}, t_{PHL}	Load all outputs through 100Ω to ground See figure 4	9 10 11	0.40 0.40 0.40	1.25 1.50 1.25	ns

1/ The quiescent limits are determined after a device has reached thermal equilibrium. This is defined as the reading taken with the device in a socket with ≥ 500 LFPM of +25° C, +125° C or -55° C (as applicable) air blowing on the unit in a transverse direction with power applied for at least 4 minutes before the reading is taken. This method was used for theoretical limit establishment only. All devices shall be tested to the delta V (rapid test) conditions specified herein. The rapid test method is an equivalent method of testing quiescent conditions.

2/ The high and low level output current varies with temperature and shall be calculated using the following formulas: $I_{OH} = (-2\ V - V_{OH})/100\Omega$ and $I_{OL} = (-2\ V - V_{OL})/100\Omega$.

3/ The I_{EE} limits, although specified in the minimum column, shall not be exceeded, in magnitude, as a maximum value.

4/ The dc rapid test forcing functions and limits are used for all dc testing. These limits are determined for each device type based on the power dissipation and package type. The rapid test (delta V) limits and forcing functions are skewed allowing rapid testing to be performed at standard temperatures without the addition of delta T's.

Case outlines	E	F, X	2
Terminal number	Terminal symbol		
1	V_{CC1}	4B	NC
2	$\overline{1Y}$	$\overline{3Y}$	V_{CC1}
3	$\overline{2Y}$	$\overline{4Y}$	$\overline{1Y}$
4	1A	V_{CC2}	$\overline{2Y}$
5	1B	V_{CC1}	1A
6	2A	$\overline{1Y}$	NC
7	2B	$\overline{2Y}$	1B
8	V_{EE}	1A	2A
9	4Y	1B	2B
10	3A	2A	V_{EE}
11	3B	2B	NC
12	4A	V_{EE}	4Y
13	4B	4Y	3A
14	$\overline{3Y}$	3A	3B
15	$\overline{4Y}$	3B	4A
16	V_{CC2}	4A	NC
17	- - -	- - -	4B
18	- - -	- - -	$\overline{3Y}$
19	- - -	- - -	$\overline{4Y}$
20	- - -	- - -	V_{CC2}

NC = No connection

FIGURE 1. Terminal connections.

Each gate			
Inputs		Outputs	
A	B	$\overline{Y}$	Y
L	L	H	L
L	H	L	H
H	L	L	H
H	H	L	H

H = High level
L = Low level

FIGURE 2. Truth table.

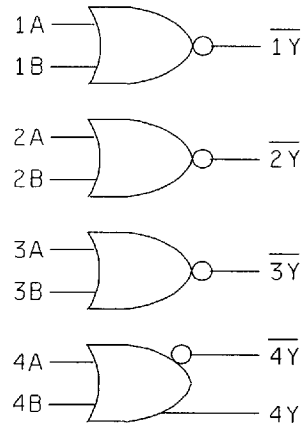
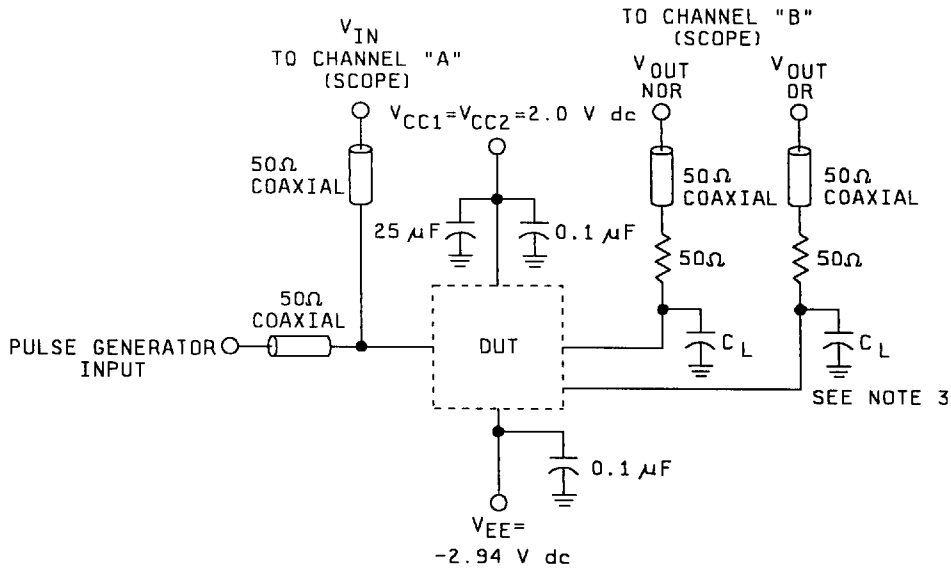
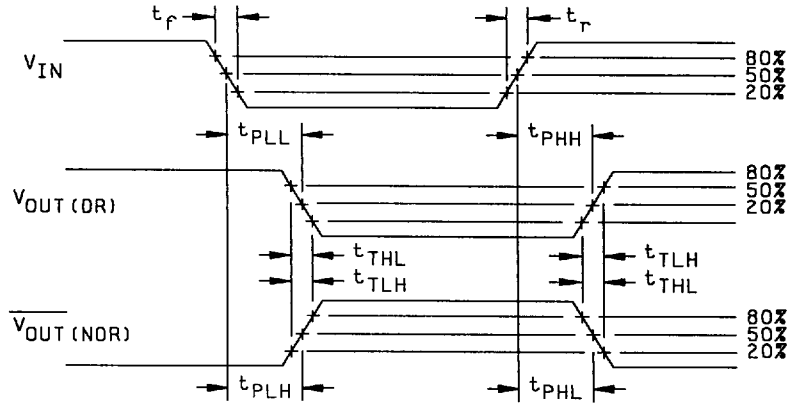


FIGURE 3. Logic diagram.





NOTES

1. All input and output cables to the scope are equal lengths of 50Ω coaxial cable.
2. Outputs not under test should be connected to a 100Ω resistor to ground.
3. C_L (test jig) ≤ 5 pF.
4. OR output from gate 4 only.
5. Pulse generator characteristics:
   PRR = 1 MHz, t_r and t_f = 20 ns ± 0.2 ns (20% to 80%), duty cycle = 50%.

FIGURE 4. Timing waveforms.

TABLE II. Electrical test requirements.

MIL-STD-883 test requirements	Subgroups (in accordance with MIL-STD-883, method 5005, table I)
Interim electrical parameters (method 5004)	1
Final electrical test parameters (method 5004)	1*, 2, 3, 7* 8A, 8B, 9
Group A test requirements (method 5005)	1, 2, 3, 7, 8A 8B, 9, 10, 11
Groups C and D end-point electrical parameters (method 5005)	1, 2, 3

* PDA applies to subgroup 1 and 7.

4.3 Quality conformance inspection. Quality conformance inspection shall be in accordance with method 5005 of MIL-STD-883 including groups A, B, C, and D inspections. The following additional criteria shall apply.

4.3.1 Group A inspection.

a. Tests shall be as specified in table II herein.

b. Subgroups 4, 5 and 6 in table I, method 5005 of MIL-STD-883 shall be omitted.

c. Subgroup 7, 8A and 8B shall include verification of the truth table specified on figure 2 herein.

4.3.2 Groups C and D inspections.

a. End-point electrical parameters shall be as specified in table II herein.

b. Steady-state life test conditions, method 1005 of MIL-STD-883.

(1) Test condition D. The test circuit shall be maintained by the manufacturer under document revision level control and shall be made available to the preparing or acquiring activity upon request. The test circuit shall specify the inputs, outputs, biases, and power dissipation, as applicable, in accordance with the intent specified in test method 1005 of MIL-STD-883.

(2) T_A = +125°C, minimum.

(3) Test duration: 1,000 hours, except as permitted by method 1005 of MIL-STD-883.

5. PACKAGING

5.1 Packaging requirements. The requirements for packaging shall be in accordance with MIL-PRF-38535, appendix A.

6. NOTES

6.1 Intended use. Microcircuits conforming to this drawing are intended for use for Government microcircuit applications (original equipment), design applications, and logistics purposes.

6.2 Replaceability. Microcircuits covered by this drawing will replace the same generic device covered by a contractor-prepared specification or drawing.

6.3 Configuration control of SMD's. All proposed changes to existing SMD's will be coordinated with the users of record for the individual documents. This coordination will be accomplished in accordance with MIL-STD-973 using DD Form 1692, Engineering Change Proposal.

6.4 Record of users. Military and industrial users shall inform Defense Supply Center Columbus when a system application requires configuration control and the applicable SMD. DSCC will maintain a record of users and this list will be used for coordination and distribution of changes to the drawings. Users of drawings covering microelectronics devices (FSC 5962) should contact DSCC-VA, telephone (614) 692-0525.

6.5 Comments. Comments on this drawing should be directed to DSCC-VA, Columbus, Ohio 43216-5000, or telephone (614) 692-0674.

6.6 Approved sources of supply. Approved sources of supply are listed in MIL-HDBK-103. The vendors listed in MIL-HDBK-103 have agreed to this drawing and a certificate of compliance (see 3.6 herein) has been submitted to and accepted by DSCC-VA.

STANDARD MICROCIRCUIT DRAWING BULLETIN

DATE: 98-08-12

Approved sources of supply for SMD 5962-87557 are listed below for immediate acquisition information only and shall be added to MIL-HDBK-103 and QML-38535 during the next revision. MIL-HDBK-103 and QML-38535 will be revised to include the addition or deletion of sources. The vendors listed below have agreed to this drawing and a certificate of compliance has been submitted to and accepted by DSCC-VA. This bulletin is superseded by the next dated revision of MIL-HDBK-103 and QML-38535.

Standard microcircuit drawing PIN 1/	Vendor CAGE number	Vendor similar PIN 2/
5962-8755701EA	0EU86	AS10H502C16/883C
5962-8755701FA	3/	10H502/BFAJC
5962-87557012A	0EU86	AS10H502EC20/883C
5962-8755701XA	0EU86	AS10H502F16/883C

1/ The lead finish shown for each PIN representing a hermetic package is the most readily available from the manufacturer listed for that part. If the desired lead finish is not listed contact the vendor to determine its availability.
2/ Caution. Do not use this number for item acquisition. Items acquired to this number may not satisfy the performance requirements of this drawing.
3/ No longer available from the approved source of supply

Vendor CAGE number	Vendor name and address
0EU86	Austin Semiconductor Inc. 8701 Cross Park Dr. Austin, TX 78754-4566

The information contained herein is disseminated for convenience only and the Government assumes no liability whatsoever for any inaccuracies in the information bulletin.