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	SHEET	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18

PMIC N/A	PREPARED BY <i>Monica E. Pelley</i> CHECKED BY <i>Monica E. Pelley</i> APPROVED BY <i>[Signature]</i>	DEFENSE ELECTRONICS SUPPLY CENTER DAYTON, OHIO 45444 MICROCIRCUIT, DIGITAL, ADVANCED CMOS, UP/DOWN BINARY COUNTER, MONOLITHIC SILICON
STANDARDIZED MILITARY DRAWING THIS DRAWING IS AVAILABLE FOR USE BY ALL DEPARTMENTS AND AGENCIES OF THE DEPARTMENT OF DEFENSE AMSC N/A	DRAWING APPROVAL DATE 13 MARCH 1990	SIZE A
	REVISION LEVEL	CAGE CODE 67268
	SHEET 1	

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• U.S. GOVERNMENT PRINTING OFFICE: 1987 — 748-129/60911

DISTRIBUTION STATEMENT A. Approved for public release; distribution is unlimited.

5962-E1435

1. SCOPE

1.1 Scope. This drawing describes device requirements for class B microcircuits in accordance with 1.2.1 of MIL-STD-883, "Provisions for the use of MIL-STD-883 in conjunction with compliant non-JAN devices".

1.2 Part number. The complete part number shall be as shown in the following example:

5962-89749	01	E	X
Drawing number	Device type (1.2.1)	Case outline (1.2.2)	Lead finish per MIL-M-38510

1.2.1 Device type. The device type shall identify the circuit function as follows:

Device type	Generic number	Circuit function
01	54AC191	Up/down binary counter with preset and ripple clock

1.2.2 Case outlines. The case outlines shall be as designated in appendix C of MIL-M-38510, and as follows:

Outline letter	Case outline
E	D-2 (16-lead, .840" x .310" x .200"), dual-in-line package
F	F-5 (16-lead, .440" x .285" x .085"), flat package
2	C-2 (20-terminal, .358" x .358" x .100"), square chip carrier package

1.3 Absolute maximum ratings.

Supply voltage range 1/	- - - - -	-0.5 V dc to +6.0 V dc
DC input voltage 1/	- - - - -	-0.5 V dc to $V_{CC} + 0.5$ V dc
DC output voltage 1/	- - - - -	-0.5 V dc to $V_{CC} + 0.5$ V dc
Clamp diode current	- - - - -	± 20 mA
DC output current (per pin)	- - - - -	± 50 mA
DC V_{CC} or GND current	- - - - -	± 100 mA
Storage temperature range	- - - - -	-65°C to +150°C
Maximum power dissipation (P_D)	- - - - -	500 mW
Lead temperature (soldering, 10 seconds)	- - - - -	+300°C
Thermal resistance, junction-to-case (θ_{JC})	- - - - -	See MIL-M-38510, appendix C
Junction temperature (T_J) 2/	- - - - -	+175°C

1.4 Recommended operating conditions.

Supply voltage range (V_{CC}) 3/	- - - - -	+3.0 V dc to +5.5 V dc
Input voltage range	- - - - -	0.0 V dc to V_{CC}
Output voltage range	- - - - -	0.0 V dc to V_{CC}
Case operating temperature range (T_C)	- - - - -	-55°C to +125°C
Input rise or fall times:		
$V_{CC} = 3.6$ V to 5.5 V	- - - - -	0 to 8 ns/V

1/ Unless otherwise specified, all voltages are referenced to GND.

2/ Maximum junction temperature shall not be exceeded except for allowable short duration burn-in screening conditions in accordance with method 5004 of MIL-STD-883.

3/ Operation from 2.0 V dc to 3.0 V dc is provided for compatibility with data retention and battery backup systems. Data retention implies no input transitions and no stored data loss with the following conditions: $V_{IH} \geq 70$ percent V_{CC} , $V_{IL} \leq 30$ percent V_{CC} , $V_{OH} \geq 70$ percent V_{CC} at -20 μ A, $V_{OL} \leq 30$ percent V_{CC} at 20 μ A.

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2. APPLICABLE DOCUMENTS

2.1 Government specification, standard, and bulletin. Unless otherwise specified, the following specification, standard, and bulletin of the issue listed in that issue of the Department of Defense Index of Specifications and Standards specified in the solicitation, form a part of this drawing to the extent specified herein.

SPECIFICATION

MILITARY

MIL-M-38510 - Microcircuits, General Specification for.

STANDARD

MILITARY

MIL-STD-883 - Test Methods and Procedures for Microelectronics.

BULLETIN

MILITARY

MIL-BUL-103 - List of Standardized Military Drawing (SMD's).

(Copies of the specification, standard, and bulletin required by manufacturers in connection with specific acquisition functions should be obtained from the contracting activity or as directed by the contracting activity.)

2.2 Order of precedence. In the event of a conflict between the text of this drawing and the references cited herein, the text of this drawing shall take precedence.

3. REQUIREMENTS

3.1 Item requirements. The individual item requirements shall be in accordance with 1.2.1 of MIL-STD-883, "Provisions for the use of MIL-STD-883 in conjunction with compliant non-JAN devices" and as specified herein.

3.2 Design, construction, and physical dimensions. The design, construction, and physical dimensions shall be as specified in MIL-M-38510 and herein.

3.2.1 Terminal connections. The terminal connections shall be as specified on figure 1.

3.2.2 Truth tables. The truth tables shall be as specified on figure 2.

3.2.3 Logic diagram. The logic diagram shall be as specified on figure 3.

3.2.4 Case outlines. The case outlines shall be in accordance with 1.2.2 herein.

3.3 Electrical performance characteristics. Unless otherwise specified herein, the electrical performance characteristics are as specified in table I and shall apply over the full case operating temperature range.

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3.4 Electrical test requirements. The electrical test requirements shall be the subgroups specified in table II. The electrical tests for each subgroup are described in table I.

3.5 Marking. Marking shall be in accordance with MIL-STD-883 (see 3.1 herein). The part shall be marked with the part number listed in 1.2 herein. In addition, the manufacturer's part number may also be marked as listed in MIL-BUL-103 (see 6.6 herein).

3.6 Certificate of compliance. A certificate of compliance shall be required from a manufacturer in order to be listed as an approved source of supply in MIL-BUL-103 (see 6.6 herein). The certificate of compliance submitted to DESC-ECS prior to listing as an approved source of supply shall affirm that the manufacturer's product meets the requirements of MIL-STD-883 (see 3.1 herein) and the requirements herein.

3.7 Certificate of conformance. A certificate of conformance as required in MIL-STD-883 (see 3.1 herein) shall be provided with each lot of microcircuits delivered to this drawing.

3.8 Notification of change. Notification of change to DESC-ECS shall be required in accordance with MIL-STD-883 (see 3.1 herein).

3.9 Verification and review. DESC, DESC'S agent, and the acquiring activity retain the option to review the manufacturer's facility and applicable required documentation. Offshore documentation shall be made available onshore at the option of the reviewer.

4. QUALITY ASSURANCE PROVISIONS

4.1 Sampling and inspection. Sampling and inspection procedures shall be in accordance with section 4 of MIL-M-38510 to the extent specified in MIL-STD-883 (see 3.1 herein).

4.2 Screening. Screening shall be in accordance with method 5004 of MIL-STD-883, and shall be conducted on all devices prior to quality conformance inspection. The following additional criteria shall apply:

a. Burn-in test, method 1015 of MIL-STD-883.

(1) Test condition A, B, C, or D using the circuit submitted with the certificate of compliance (see 3.6 herein).

(2) $T_A = +125^{\circ}\text{C}$, minimum.

b. Interim and final electrical test parameters shall be as specified in table II herein, except interim electrical parameter tests prior to burn-in are optional at the discretion of the manufacturer.

4.3 Quality conformance inspection. Quality conformance inspection shall be in accordance with method 5005 of MIL-STD-883 including groups A, B, C, and D inspections. The following additional criteria shall apply.

4.3.1 Group A inspection.

a. Tests shall be as specified in table II herein.

b. Subgroups 5 and 6 in table I, method 5005 of MIL-STD-883 shall be omitted.

c. Subgroup 4 (C_{IN} and C_{PD} measurements) shall be measured only for the initial test and after process or design changes which may affect capacitance. Test all applicable pins on five devices with zero failures.

d. Subgroup 7 and 8 tests shall verify the truth table as specified on figure 2.

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TABLE I. Electrical performance characteristics.

Test	Symbol	Conditions -55°C ≤ T _C ≤ +125°C unless otherwise specified		Group A subgroups	Limits		Unit
					Min	Max	
High level output voltage	V _{OH}	V _{IN} = V _{IH} minimum or V _{IL} maximum, I _{OH} = -50 μA <u>1/</u>	V _{CC} = 3.0 V	1, 2, 3	2.9		V
			V _{CC} = 4.5 V		4.4		
			V _{CC} = 5.5 V		5.4		
		V _{IN} = V _{IH} minimum or V _{IL} maximum, I _{OH} = -12 mA <u>1/</u>	V _{CC} = 3.0 V		2.4		
			V _{CC} = 4.5 V		3.7		
			V _{CC} = 5.5 V		4.7		
Low level output voltage	V _{OL}	V _{IN} = V _{IH} minimum or V _{IL} maximum, I _{OL} = 50 μA <u>1/</u>	V _{CC} = 3.0 V	1, 2, 3		0.1	V
			V _{CC} = 4.5 V			0.1	
			V _{CC} = 5.5 V			0.1	
		V _{IN} = V _{IH} minimum or V _{IL} maximum, I _{OL} = 12 mA <u>1/</u>	V _{CC} = 3.0 V			0.5	
			V _{CC} = 4.5 V			0.5	
			V _{CC} = 5.5 V			0.5	
		V _{IN} = V _{IH} minimum or V _{IL} maximum, I _{OL} = 50 mA <u>1/</u>	V _{CC} = 5.5 V			1.65	

See footnotes at end of table.

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TABLE 1. Electrical performance characteristics - Continued.

Test	Symbol	Conditions -55°C < T _C < +125°C unless otherwise specified		Group A subgroups	Limits		Unit
					Min	Max	
High level input voltage	V _{IH}	<u>2/</u>	V _{CC} = 3.0 V	1, 2, 3	2.1		V
			V _{CC} = 4.5 V		3.15		
			V _{CC} = 5.5 V		3.85		
Low level input voltage	V _{IL}	<u>2/</u>	V _{CC} = 3.0 V	1, 2, 3		0.9	V
			V _{CC} = 4.5 V			1.35	
			V _{CC} = 5.5 V			1.65	
Input leakage current	I _{IL}	V _{IN} = 0.0 V	V _{CC} = 5.5 V	1, 2, 3		-1.0	μA
	I _{IH}	V _{IN} = 5.5 V				1.0	
Quiescent current	I _{CCH}	V _{IN} = V _{CC} or GND, V _{CC} = 5.5 V		1, 2, 3		160	μA
	I _{CCL}					160	
	I _{CCZ}					160	
Input capacitance	C _{IN}	See 4.3.1c		4		8.0	pF
Power dissipation capacitance <u>3/</u>	C _{PD}	See 4.3.1c		4		85	pF
Functional tests		Tested at V _{CC} = 3.0 V and repeated at V _{CC} = 5.5 V, see 4.3.1d		7, 8			

See footnotes at end of table.

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TABLE 1. Electrical performance characteristics - Continued.

Test	Symbol	Conditions -55°C < T _C < +125°C unless otherwise specified		Group A subgroups	Limits		Unit
					Min	Max	
Propagation delay time, CP to Qn	t _{PHL1}	C _L = 50 pF, R _L = 500Ω, see figure 4 4/	V _{CC} = 3.0 V	9 10,11	1.0 1.0	13.0 16.0	ns
			V _{CC} = 4.5 V	9 10,11	1.5 1.5	10.0 12.0	
	t _{PLH1}		V _{CC} = 3.0 V	9 10,11	1.0 1.0	13.0 16.5	ns
			V _{CC} = 4.5 V	9 10,11	1.5 1.5	10.0 12.0	
Propagation delay time, CP to TC	t _{PHL2}		V _{CC} = 3.0 V	9 10,11	1.0 1.0	15.5 19.0	ns
			V _{CC} = 4.5 V	9 10,11	1.5 1.5	11.5 14.5	
	t _{PLH2}		V _{CC} = 3.0 V	9 10,11	1.0 1.0	15.0 19.5	ns
			V _{CC} = 4.5 V	9 10,11	1.5 1.5	11.0 14.0	
Propagation delay time, CP to RC	t _{PHL3}	V _{CC} = 3.0 V	9 10,11	1.0 1.0	10.0 12.5	ns	
		V _{CC} = 4.5 V	9 10,11	1.5 1.5	8.0 9.5		
	t _{PLH3}	V _{CC} = 3.0 V	9 10,11	1.0 1.0	11.5 14.0	ns	
		V _{CC} = 4.5 V	9 10,11	1.5 1.5	9.0 10.5		

See footnotes at end of table.

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TABLE I. Electrical performance characteristics - Continued.

TABLE I. Electrical performance characteristics - Continued.							
Test	Symbol	Conditions -55°C < T _C < +125°C unless otherwise specified		Group A subgroups	Limits		Unit
					Min	Max	
Propagation delay time, CE to RC	t _{PHL4}	C _L = 50 pF, R _L = 500Ω, see figure 4 4/	V _{CC} = 3.0 V	9 10,11	1.0 1.0	10.5 12.5	ns
			V _{CC} = 4.5 V	9 10,11	1.5 1.5	7.5 9.5	
	t _{PLH4}		V _{CC} = 3.0 V	9 10,11	1.0 1.0	11.5 14.0	ns
			V _{CC} = 4.5 V	9 10,11	1.5 1.5	8.0 10.0	
Propagation delay time, U/D to RC	t _{PHL5}	V _{CC} = 3.0 V	9 10,11	1.0 1.0	12.5 15.0	ns	
		V _{CC} = 4.5 V	9 10,11	1.5 1.5	9.0 11.0		
	t _{PLH5}	V _{CC} = 3.0 V	9 10,11	1.0 1.0	12.5 14.5	ns	
		V _{CC} = 4.5 V	9 10,11	1.5 1.5	9.0 11.0		
Propagation delay time, U/D to TC	t _{PHL6}	V _{CC} = 3.0 V	9 10,11	1.0 1.0	11.0 13.5	ns	
		V _{CC} = 4.5 V	9 10,11	1.5 1.5	8.5 10.0		
	t _{PLH6}	V _{CC} = 3.0 V	9 10,11	1.0 1.0	11.0 14.0	ns	
		V _{CC} = 4.5 V	9 10,11	1.5 1.5	8.5 10.5		

See footnotes at end of table.

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TABLE I. Electrical performance characteristics - Continued.

Test	Symbol	Conditions -55°C < T _C < +125°C unless otherwise specified		Group A subgroups	Limits		Unit
					Min	Max	
Propagation delay time, P _n to Q _n	t _{PHL7}	C _L = 50 pF, R _L = 500Ω, see figure 4 4/	V _{CC} = 3.0 V	9 10,11	1.0 1.0	12.0 15.5	ns
			V _{CC} = 4.5 V	9 10,11	1.5 1.5	9.0 10.5	
	t _{PLH7}		V _{CC} = 3.0 V	9 10,11	1.0 1.0	13.5 16.5	ns
			V _{CC} = 4.5 V	9 10,11	1.5 1.5	9.0 11.5	
Propagation delay time, P _L to Q _n	t _{PHL8}		V _{CC} = 3.0 V	9 10,11	1.0 1.0	12.5 15.5	ns
			V _{CC} = 4.5 V	9 10,11	1.5 1.5	9.5 11.5	
	t _{PLH8}		V _{CC} = 3.0 V	9 10,11	1.0 1.0	14.0 18.0	ns
			V _{CC} = 4.5 V	9 10,11	1.5 1.5	10.0 12.5	
Maximum clock frequency, CP	f _{MAX}	V _{CC} = 3.0 V	9 10,11	70 55		MHz	
		V _{CC} = 4.5 V	9 10,11	90 80			
Setup time, P _n to P _L (high or low)	t _{s1}	V _{CC} = 3.0 V	9 10,11	3.5 4.0		ns	
		V _{CC} = 4.5 V	9 10,11	2.5 3.0			

See footnotes at end of table.

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TABLE 1. Electrical performance characteristics - Continued.

Test	Symbol	Conditions -55°C < T _C < +125°C unless otherwise specified	Group A subgroups	Limits		Unit
				Min	Max	
Setup time, \overline{CE} to CP (low)	t _{s2}	C _L = 50 pF, R _L = 500Ω, see figure 4 4/	V _{CC} = 3.0 V	9 10,11	7.0 9.0	ns
			V _{CC} = 4.5 V	9 10,11	5.0 6.0	
Setup time, $\overline{U/D}$ to CP (high or low)	t _{s3}		V _{CC} = 3.0 V	9 10,11	9.0 10.5	ns
			V _{CC} = 4.5 V	9 10,11	6.0 7.5	
Hold time, Pn to \overline{PL} (high or low)	t _{h1}		V _{CC} = 3.0 V	9 10,11	1.0 1.5	ns
			V _{CC} = 4.5 V	9 10,11	2.0 2.0	
Hold time, \overline{CE} to CP (low)	t _{h2}		V _{CC} = 3.0 V	9 10,11	0.0 0.0	ns
			V _{CC} = 4.5 V	9 10,11	0.5 0.5	
Hold time, $\overline{U/D}$ to CP (high or low)	t _{h3}		V _{CC} = 3.0 V	9 10,11	0.0 0.0	ns
			V _{CC} = 4.5 V	9 10,11	1.0 1.0	
CP pulse width (high)	t _{w1}		V _{CC} = 3.0 V	9 10,11	5.0 5.0	ns
			V _{CC} = 4.5 V	9 10,11	5.0 5.0	

See footnotes at end of table.

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TABLE I. Electrical performance characteristics - Continued.

Test	Symbol	Conditions -55°C ≤ T _C ≤ +125°C unless otherwise specified	Group A subgroups	Limits		Unit
				Min	Max	
CP pulse width (low)	t _{w2}	C _L = 50 pF, R _L = 500Ω, see figure 4 4/	V _{CC} = 3.0 V	9 10,11	5.0 6.0	ns
			V _{CC} = 4.5 V	9 10,11	6.0 6.0	
PL pulse width (low)	t _{w3}		V _{CC} = 3.0 V	9 10,11	5.0 5.0	ns
			V _{CC} = 4.5 V	9 10,11	5.0 5.0	
Recovery time, PL to CP	t _{rec}		V _{CC} = 3.0 V	9 10,11	1.0 1.5	ns
			V _{CC} = 4.5 V	9 10,11	1.0 1.0	

1/ The V_{OH} and V_{OL} tests will be tested at V_{CC} = 3.0 V and V_{CC} = 4.5 V. V_{OH} and V_{OL} are guaranteed, if not tested, for V_{CC} = 5.5 V. Limits shown apply to operation at V_{CC} = 3.3 V ± 0.3 V and V_{CC} = 5.0 V ± 0.5 V. Transmission driving tests are performed at V_{CC} = 5.5 V with a 2 ms duration maximum.

2/ The V_{IH} and V_{IL} tests are not required and shall be applied as forcing functions for the V_{OH} and V_{OL} tests.

3/ Power dissipation capacitance (C_{PD}), determines the dynamic power consumption, P_D = (C_{PD} + C_L)(V_{CC} × V_{CC})f + I_{CC}(V_{CC}), and the dynamic current consumption (I_S), is I_S = (C_{PD} + C_L) V_{CC} f + I_{CC}.

4/ AC limits at V_{CC} = 5.5 V are equal to limits at V_{CC} = 4.5 V and guaranteed by testing at V_{CC} = 4.5 V. Minimum ac limits are guaranteed for V_{CC} = 5.5 V by guardbanding V_{CC} = 4.5 V limits to 1.5 ns (minimum).

4.3.2 Groups C and D inspections.

a. End-point electrical parameters shall be as specified in table II herein.

b. Steady-state life test conditions, method 1005 of MIL-STD-883.

(1) Test condition A, B, C, or D using the circuit submitted with the certificate of compliance (see 3.6 herein).

(2) T_A = +125°C, minimum.

(3) Test duration: 1,000 hours, except as permitted by method 1005 of MIL-STD-883.

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Device type	01	
Case outlines	E and F	2
Terminal number	Terminal symbol	
1	P1	NC
2	Q1	P1
3	Q0	Q1
4	CE	Q0
5	U/D	CE
6	Q2	NC
7	Q3	U/D
8	GND	Q2
9	P3	Q3
10	P2	GND
11	PL	NC
12	TC	P3
13	RC	P2
14	CP	PL
15	PO	TC
16	VCC	NC
17	---	RC
18	---	CP
19	---	PO
20	---	VCC

NC = No connection



FIGURE 1. Terminal connections.

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Mode select table

Inputs				Mode
\overline{PL}	\overline{CE}	$\overline{U/D}$	CP	
H	L	L	\uparrow	Count up
H	L	H	\uparrow	Count down
L	X	X	X	Preset (asynchronous)
H	H	X	X	No change (hold)

\overline{RC} truth table

Inputs			Outputs
\overline{CE}	TC*	CP	\overline{RC}
L	H		
H	X	X	H
X	L	X	H


* TC is generated internally
H = High voltage level
L = Low voltage level
X = Irrelevant
 \uparrow = Low-to-high transition
 = Low clock pulse

FIGURE 2. Truth tables.

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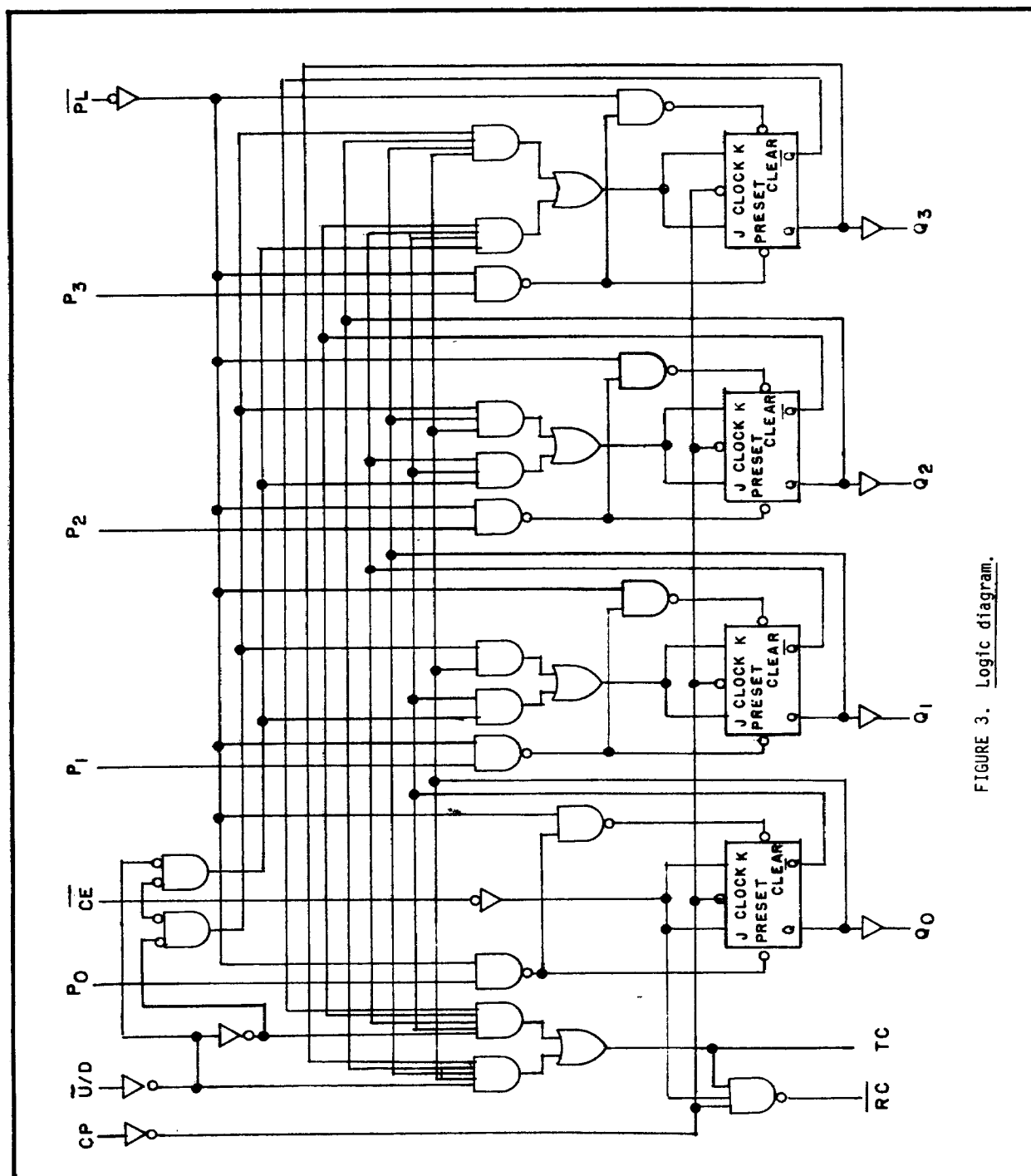
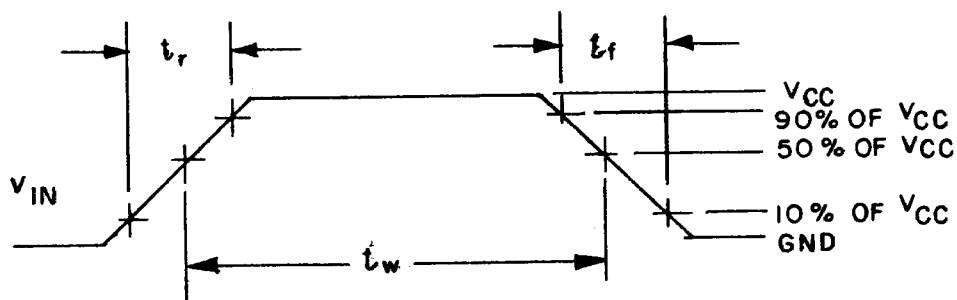
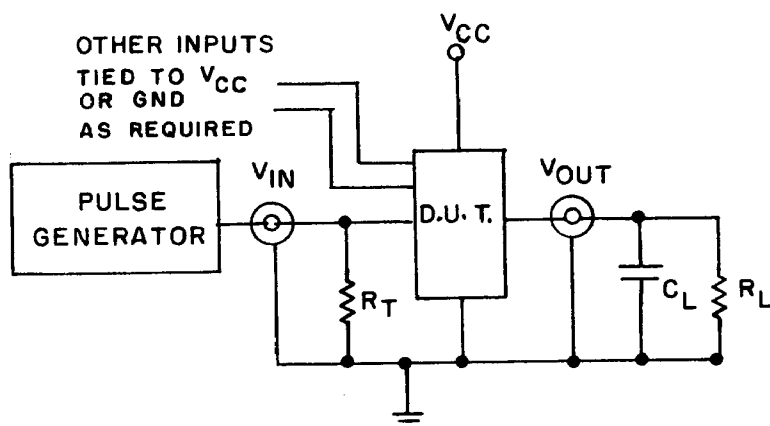


FIGURE 3. Logic diagram.

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NOTES:

1. C_L includes probe and jig capacitance.
2. $C_L = 50 \text{ pF}$, $R_L = 500\Omega$, R_T = termination resistance and should be equal to Z_{OUT} of the pulse generator.
3. $t_r = t_f = 3.0 \text{ ns}$ (10 percent to 90 percent, unless otherwise specified).
Duty cycle = 50 percent.

FIGURE 4. Test circuit and switching waveforms.

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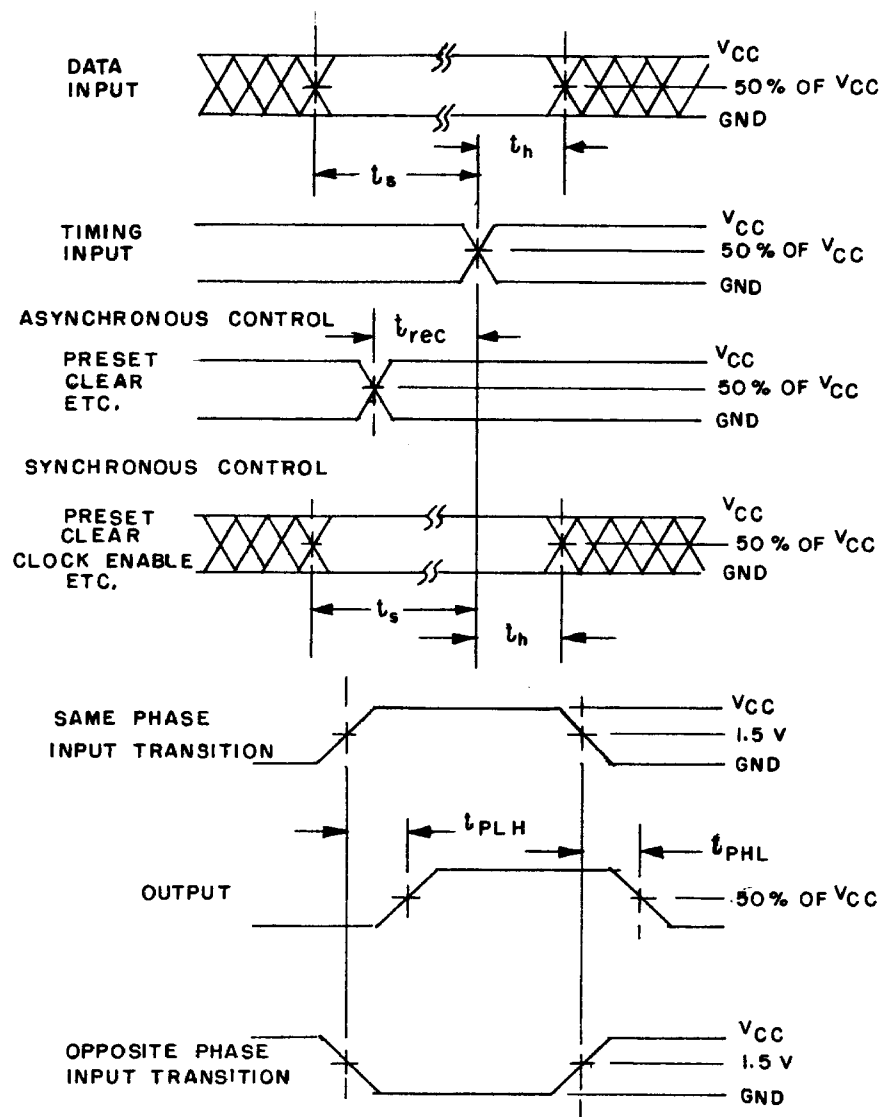


FIGURE 4. Test circuit and switching waveforms - Continued.

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TABLE II. Electrical test requirements.

MIL-STD-883 test requirements	Subgroups (per method 5005, table 1)
Interim electrical parameters (method 5004)	---
Final electrical test parameters (method 5004)	1*, 2, 3, 7, 8, 9
Group A test requirements (method 5005)	1, 2, 3, 4, 7, 8, 9, 10, 11
Groups C and D end-point electrical parameters (method 5005)	1,2,3

*PDA applies to subgroup 1.

5. PACKAGING

5.1 Packaging requirements. The requirements for packaging shall be in accordance with MIL-M-38510.

6. NOTES

6.1 Intended use. Microcircuits conforming to this drawing are intended for use when military specifications do not exist and qualified military devices that will perform the required function are not available for OEM application. When a military specification exists and the product covered by this drawing has been qualified for listing on QPL-38510, the device specified herein will be inactivated and will not be used for new design. The QPL-38510 product shall be the preferred item for all applications.

6.2 Replaceability. Microcircuits covered by this drawing will replace the same generic device covered by a contractor-prepared specification or drawing.

6.3 Configuration control of SMD's. All proposed changes to existing SMD's will be coordinated with the users of record for the individual documents. This coordination will be accomplished in accordance with MIL-STD-481 using DD Form 1693, Engineering Change Proposal (Short Form).

6.4 Record of users. Military and industrial users shall inform Defense Electronics Supply Center when a system application requires configuration control and the applicable SMD. DESC will maintain a record of users and this list will be used for coordination and distribution of changes to the drawings. Users of drawings covering microelectronic devices (FSC 5962) should contact DESC-ECS, telephone (513) 296-8527.

6.5 Comments. Comments on this drawing should be directed to DESC-ECS, Dayton, Ohio 45444, or telephone 513-296-5375.

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6.6 Approved source of supply. An approved source of supply is listed in MIL-BUL-103. Additional sources will be added to MIL-BUL-103 as they become available. The vendor listed in MIL-BUL-103 has agreed to this drawing and a certificate of compliance (see 3.6 herein) has been submitted to and accepted by DESC-ECS. The approved source of supply listed below is for information purposes only and is current only to the date of the last action of this document.

Military drawing part number	Vendor CAGE number	Vendor similar part number 1/
5962-8974901EX	27014	54AC191DMQB
5962-8974901FX	27014	54AC191FMQB
5962-89749012X	27014	54AC191LMQB

1/ Caution. Do not use this number for item acquisition. Items acquired to this number may not satisfy the performance requirements of this drawing.

Vendor CAGE
number

27014

Vendor name
and address

National Semiconductor
2900 Semiconductor Drive
P.O. Box 58090
Santa Clara, CA 95052-8090

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U. S. GOVERNMENT PRINTING OFFICE: 1985-550-547

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