REVISIONS			
LTR	DESCRIPTION	DATE (YR-MO-DA)	APPROVED
A	Page 11: Correction to terminal connections. Editorial changes throughout.	1988 MAY 11	M. A. Frye
B	Add one vendor, CAGE 54186 for devices 01, 02, and 03. Make changes to 1.3 and table I. Editorial changes throughout.	1989 JUNE 23	Thomas J. Johnson

REV																								
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REV STATUS OF SHEETS	REV	B	B	A	B	B	B	B	A	B	A	A			A	A	B							
	SHEET	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16							

PMIC N/A

STANDARDIZED MILITARY DRAWING

THIS DRAWING IS AVAILABLE FOR USE BY ALL DEPARTMENTS AND AGENCIES OF THE DEPARTMENT OF DEFENSE

AMSC N/A

PREPARED BY: Marcia B. Kelleher

CHECKED BY: Dan DiCenzo

APPROVED BY: Michael A. Frye

DRAWING APPROVAL DATE: 2 December 1987

REVISION LEVEL: B

DEFENSE ELECTRONICS SUPPLY CENTER
DAYTON, OHIO 45444

MIROCIRCUIT, CMOS, DUAL, 8-BIT MULTIPLYING DIGITAL TO ANALOG CONVERTER, MONOLITHIC SILICON

SIZE	CAGE CODE	
A	67268	5962-87701

SHEET 1 OF 16

DESC FORM 193
SEP 87

* U.S. GOVERNMENT PRINTING OFFICE: 1987 — 748-129/60911

1. SCOPE

1.1 Scope. This drawing describes device requirements for class B microcircuits in accordance with 1.2.1 of MIL-STD-883, "Provisions for the use of MIL-STD-883 in conjunction with compliant non-JAN devices".

1.2 Part number. The complete part number shall be as shown in the following example:

5962-87701	01	R	X
Drawing number	Device type (1.2.1)	Case outline (1.2.2)	Lead finish per MIL-M-38510

1.2.1 Device types. The device types shall identify the circuit function as follows:

Device type	Generic number	Circuit function
01	7528	CMOS dual 8-bit buffered DAC, ±4 LSB's of gain error
02	7528	CMOS dual 8-bit buffered DAC, ±2 LSB's of gain error
03	7528	CMOS dual 8-bit buffered DAC, ±1 LSB's of gain error

1.2.2 Case outlines. The case outlines shall be as designated in appendix C of MIL-M-38510, and as follows:

Outline letter	Case outline
R	D-8 (20-lead, 1.060" x .310" x .200"), dual-in-line package
2	C-2 (20-terminal, .358" x .358" x .100"), square chip carrier package

1.3 Absolute maximum ratings.

Supply voltage	+5 V dc to +15 V dc
V_{DD} to AGND	0 V dc, +17 V dc
V_{DD} to DGND	0 V dc, +17 V dc
Digital input voltage to DGND	-0.3 V dc to +15 V dc
V_{RFBA}, V_{RFBB} to DGND	±25 V dc
V_{REFA}, V_{REFB} to AGND	±25 V dc
V pin 1 to DGND	-0.3 V dc to V_{DD}
V pin 2, V pin 20 to AGND	-0.3 V dc to +15 V dc
AGND to DGND	-0.3 V, V_{DD} + 0.3 V
DGND to AGND	+0.3 V
Power dissipation (P_D)	
Up to +75°C	450 mW
Derate above +75°C	6 mW/°C
Storage temperature range	-65°C to +150°C
Lead temperature (soldering, 10 seconds)	+300°C
Thermal resistance (θ_{JC})	See MIL-M-38510, appendix C
Thermal resistance (θ_{JA})	+120°C

1.4 Recommended operating conditions.

Operating ambient temperature range (T_A)	-55°C to +125°C
Supply voltage range (V_{DD})	+4.75 V dc to +5.25 V dc and +14.25 V dc to +15.75 V dc
V_{REF} DACA = V_{REF} DACB	+10 V dc
OUT DACA = OUT DACB	0 V dc

2. APPLICABLE DOCUMENTS

2.1 Government specification and standard. Unless otherwise specified, the following specification and standard, of the issue listed in that issue of the Department of Defense Index of Specifications and Standards specified in the solicitation, form a part of this drawing to the extent specified herein.

SPECIFICATION

MILITARY

MIL-M-38510 - Microcircuits, General Specification for.

STANDARD

MILITARY

MIL-STD-883 - Test Methods and Procedures for Microelectronics.

(Copies of the specification and standard required by manufacturers in connection with specific acquisition functions should be obtained from the contracting activity or as directed by the contracting activity.)

2.2 Order of precedence. In the event of a conflict between the text of this drawing and the references cited herein, the text of this drawing shall take precedence.

3. REQUIREMENTS

3.1 Item requirements. The individual item requirements shall be in accordance with 1.2.1 of MIL-STD-883, "Provisions for the use of MIL-STD-883 in conjunction with compliant non-JAN devices" and as specified herein.

3.2 Design, construction, and physical dimensions. The design, construction, and physical dimensions shall be as specified in MIL-M-38510 and herein.

3.2.1 Terminal connections. The terminal connections shall be as specified on figure 1.

3.2.2 Functional diagram and mode selection. The functional diagram and mode selection shall be as specified on figure 2.

3.2.3 Write cycle timing diagram. The write cycle timing diagram shall be as specified on figure 3.

3.2.4 Case outlines. The case outlines shall be in accordance with 1.2.2 herein.

3.3 Electrical performance characteristics. Unless otherwise specified, the electrical performance characteristics are as specified in table I and apply over the full ambient operating temperature range.

3.4 Marking. Marking shall be in accordance with MIL-STD-883 (see 3.1 herein). The part shall be marked with the part number listed in 1.2 herein. In addition, the manufacturer's part number may also be marked as listed in 6.4 herein.

3.5 Certificate of compliance. A certificate of compliance shall be required from a manufacturer in order to be listed as an approved source of supply in 6.4. The certificate of compliance submitted to DESC-ECS prior to listing as an approved source of supply shall state that the manufacturer's product meets the requirements of MIL-STD-883 (see 3.1 herein) and the requirements herein.

TABLE I. Electrical performance characteristics.

Test	Symbol	Conditions 1/ $-55°C \le T_A \le +125°C$ unless otherwise specified	Device types	Group A subgroups	Limits		Unit
					Min	Max	
Resolution	RES	V_{DD} = +5 V	All	1,2,3		8	Bits
		V_{DD} = +15 V	All	1,2,3		8	
Relative accuracy 2/	RA	V_{DD} = +5 V	01	1,2,3		±1	LSB
			02	1		±1	
				2,3		±.5	
		V_{DD} = +5 V T_A = +25°C		12		±.5	
		V_{DD} = +5 V	03	1		±1	
				2,3		±.5	
		V_{DD} = +5 V T_A = +25°C		12		±.5	
		V_{DD} = +15 V	01	1,2,3		±1	
			02	1		±1	
				2,3		±.5	
		V_{DD} = +15 V T_A = +25°C		12		±.5	
		V_{DD} = +15 V	03	1		±1	
				2,3		±.5	
		V_{DD} = +15 V T_A = +25°C		12		±.5	

See footnotes at end of table.

TABLE I. Electrical performance characteristics - Continued.

Test	Symbol	Conditions 1/ $-55°C \le T_A \le +125°C$ unless otherwise specified		Device types	Group A subgroups	Limits Min	Limits Max	Unit
Gain error 3/	A_E	DAC register loaded with 1111 1111 1111	V_{DD} = +5 V	01	1		±4	LSB
					2,3		±6	
				02	1,2,3		±4	
			V_{DD} = +5 V, T_A = +25°C		12		±2	
			V_{DD} = +5 V	03	1		±4	
					2,3		±3	
			V_{DD} = +5 V, T_A = +25°C		12		±1	
			V_{DD} = +15 V	01	1		±4	
					2,3		±5	
				02	1		±4	
					2,3		±3	
			V_{DD} = +15 V, T_A = +25°C		12		±1	
			V_{DD} = + 15 V	03	1		±4	
					2,3		±1	
			V_{DD} = +15 V, T_A = +25°C		12		±1	
Differential nonlinearity	DNL	V_{DD} = +5 V, all grades guaranteed monotonic to 8-bits over operating temperature range		All	1,2,3		±1	LSB
		V_{DD} = +15 V, all grades guaranteed monotonic to 8-bits over operating temperature range		All	1,2,3		±1	

See footnotes at end of table.

TABLE I. Electrical performance characteristics - Continued.

Test	Symbol	Conditions 1/ $-55°C \le T_A \le +125°C$ unless otherwise specified		Device types	Group A subgroups	Limits		Unit
						Min	Max	
Power supply rejection $\Delta gain/\Delta V_{DD}$	PSRR	ΔV_{DD} = ±5%	V_{DD} = +5 V	All	1		.02	±%/%
					2,3		.04	
			V_{DD} = +15 V	All	1		.01	
					2,3		.02	
Output leakage current pin 2	I_{OL}	DAC latches loaded with 0000 0000	V_{DD} = +5 V	All	1		±50	nA
					2,3		±400	
			V_{DD} = +15 V	All	1		±50	
					2,3		±200	
Output leakage current pin 20			V_{DD} = +5 V	All	1		±50	
					2,3		±400	
			V_{DD} = +15 V	All	1		±50	
					2,3		±200	
Reference input resistance V_{REFA}, V_{REFB}	R_{IN}		V_{DD} = +5 V	All	1,2,3	8	15	kΩ
			V_{DD} = +15 V	All	1,2,3	8	15	
Digital input high voltage	V_{IH}		V_{DD} = +5 V	All	1,2,3	2.4		V
			V_{DD} = +15 V	All	1,2,3	13.5		
Digital input low voltage	V_{IL}		V_{DD} = +5 V	All	1,2,3		0.8	
			V_{DD} = +15 V	All	1,2,3		1.5	
Digital input current	I_{IN}	V_{IN} = 0 V or V_{DD}	V_{DD} = +5 V	All	1		±1	µA
					2,3		±10	
			V_{DD} = +15 V	All	1		±1	
					2,3		±10	

See footnotes at end of table.

TABLE I. Electrical performance characteristics - Continued.

Test	Symbol	Conditions 1/ $-55°C \le T_A \le +125°C$ unless otherwise specified		Device types	Group A subgroups	Limits Min	Limits Max	Unit
Supply current from V_{DD}	I_{DD}	All digital inputs = V_{IL} or V_{IH}	V_{DD} = +5 V	All	1,2,3		2	mA
			V_{DD} = +15 V	All	1,2,3		2	
		All digital inputs = 0 V or V_{DD}	V_{DD} = +5 V	All	1		100	µA
					2,3		500	
			V_{DD} = +15 V	All	1		100	
					2,3		500	
Gain temperature coefficient	$\Delta AE/\Delta t$	4/	V_{CC} = +5 V	All	1,2,3		±70	ppm/°C
			V_{CC} = +15 V	All	1,2,3		±35	
Feedthrough error V_{REFA} to OUTA	FT_{REFA}	4/ 5/ V_{REF} = ±10 V, 100 kHz sinewave, DAC latches loaded with 0000 0000	V_{CC} = +5 V	All	4,5,6		-70	dB
			V_{DD} = +15 V	All	4,5,6		-70	
Feedthrough error V_{REFB} to OUTB	FT_{REFB}		V_{CC} = +5 V	All	4,5,6		-70	
			V_{DD} = +15 V	All	4,5,6		-70	
Digital input capacitance	C_{IN}	T_A = +25°C 6/ DB0-DB7	V_{DD} = +5 V	All	4		10	pF
			V_{DD} = +15 V	All	4		20	
		$\overline{WR}$,$\overline{CS}$,$\overline{DACA}$/DACB T_A = +25°C 6/	V_{DD} = +5 V	All	4		10	
			V_{DD} = +15 V	All	4		15	

See footnotes at end of table.

TABLE I. Electrical performance characteristics - Continued.

Test	Symbol	Conditions 1/ $-55°C \le T_A \le +125°C$ unless otherwise specified		Device types	Group A subgroups	Limits		Unit
						Min	Max	
Output capacitance pin 2	C_{OUTA}	4/ DAC latches loaded with 0000 0000 $T_A = +25°C$	$V_{DD} = +5$ V	All	4		50	pF
			$V_{DD} = +15$ V	All	4		50	
Output capacitance pin 20	C_{OUTB}	4/ DAC latches loaded with 0000 0000 $T_A = +25°C$	$V_{DD} = +5$ V	All	4		50	
			$V_{DD} = +15$ V	All	4		50	
Output capacitance pin 2	C_{OUTA}	4/ DAC latches loaded with 1111 1111 $T_A = +25°C$	$V_{DD} = +5$ V	All	4		120	
			$V_{DD} = +15$ V	All	4		120	
Output capacitance pin 20	C_{OUTB}		$V_{DD} = +5$ V	All	4		120	
			$V_{DD} = +15$ V	All	4		120	
Chip select to write setup time	t_{CS}	7/	$V_{DD} = +5$ V	All	9	200		ns
					10,11	230		
			$V_{DD} = +15$ V	All	9	60		
					10,11	80		
Chip select to write hold time	t_{CH}	7/	$V_{DD} = +5$ V	All	9	20		
					10,11	30		
			$V_{DD} = +15$ V	All	9	10		
					10,11	15		
Write pulse width	t_{WR}	7/ $t_{CS} \ge t_{WR}$, $t_{CH} \ge 0$	$V_{DD} = +5$ V	All	9	180		
					10,11	200		
			$V_{DD} = +15$ V	All	9	60		
					10,11	80		

See footnotes at end of table.

TABLE I. Electrical performance characteristics - Continued.

Test	Symbol	Conditions 1/ $-55°C \le T_A \le +125°C$ unless otherwise specified		Device types	Group A subgroups	Limits Min	Limits Max	Unit
Data valid to write setup time	t_{DS}	7/	V_{DD} = +5 V	All	9	110		ns
					10,11	130		
			V_{DD} = +15 V	All	9	50		
					10,11	70		
Data valid to write hold time	t_{DH}	7/	V_{DD} = +5 V	All	9,10,11	10		
			V_{DD} = +15 V	All	9,10,11	10		
Data select to write setup time	t_{AS}	7/	V_{DD} = +5 V	All	9	200		
					10,11	230		
			V_{DD} = +15 V	All	9	60		
					10,11	80		
Data select to write hold time	t_{AH}	7/	V_{DD} = +5 V	All	9	20		
					10,11	30		
			V_{DD} = +15 V	All	9	10		
					10,11	15		
Reference input resistance match	$\frac{R_{MIN}}{\Delta V_{REF}}$	4/	V_{DD} = +5 V	All	1,2,3		±1	%
			V_{DD} = +15 V	All	1,2,3		±1	
Channel-to-channel isolation V_{REFA} to OUTB	CH_{ISO}	4/ V_{REFA} = ±10 V, 100 kHz sinewave, V_{REFB} = 0 V	V_{DD} = +5 V	All	4,5,6		60	dB
			V_{DD} = +15 V	All	4,5,6		60	

See footnotes at end of table.

TABLE I. Electrical performance characteristics - Continued.

Test	Symbol	Conditions 1/ $-55°C \le T_A \le +125°C$ unless otherwise specified		Device types	Group A subgroups	Limits		Unit
						Min	Max	
Channel-to-channel isolation V_{REFB} to OUTA	CH_{ISO}	4/ V_{REFB} = ±10 V, 100 kHz sinewave, V_{REFA} = 0 V	V_{DD} = +5 V	All	4,5,6		60	dB
			V_{DD} = +15 V	All	4,5,6		60	
Output current settling time	t_{SL}	4/	V_{DD} = +5 V	All	9,10,11		350	ns
			V_{DD} = +15 V	All	9,10,11		180	

1/ V_{OUT1} = 0 V; V_{REF} = +10 V, AGND = DGND unless otherwise specified.

2/ See 4.3.1d.

3/ Measured using internal RFBA and RFBB. Gain error is adjustable.

4/ Guaranteed if not tested.

5/ Feedthrough error can be reduced by connecting the metal lid to ground.

6/ See 4.3.1c.

7/ Timing in accordance with figure 3.

3.6 Certificate of conformance. A certificate of conformance as required in MIL-STD-883 (see 3.1 herein) shall be provided with each lot of microcircuits delivered to this drawing.

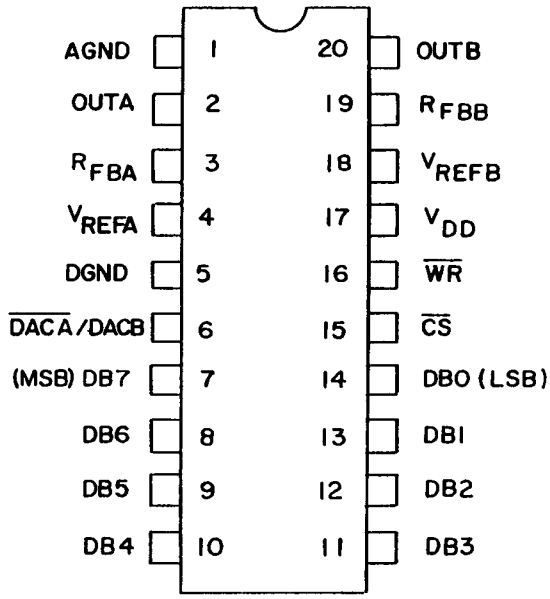
3.7 Notification of change. Notification of change to DESC-ECS shall be required in accordance with MIL-STD-883 (see 3.1 herein).

3.8 Verification and review. DESC, DESC's agent, and the acquiring activity retain the option to review the manufacturer's facility and applicable required documentation. Offshore documentation shall be made available onshore at the option of the reviewer.

4. QUALITY ASSURANCE PROVISIONS

4.1 Sampling and inspection. Sampling and inspection procedures shall be in accordance with section 4 of MIL-M-38510 to the extent specified in MIL-STD-883 (see 3.1 herein).

Case R



Case 2

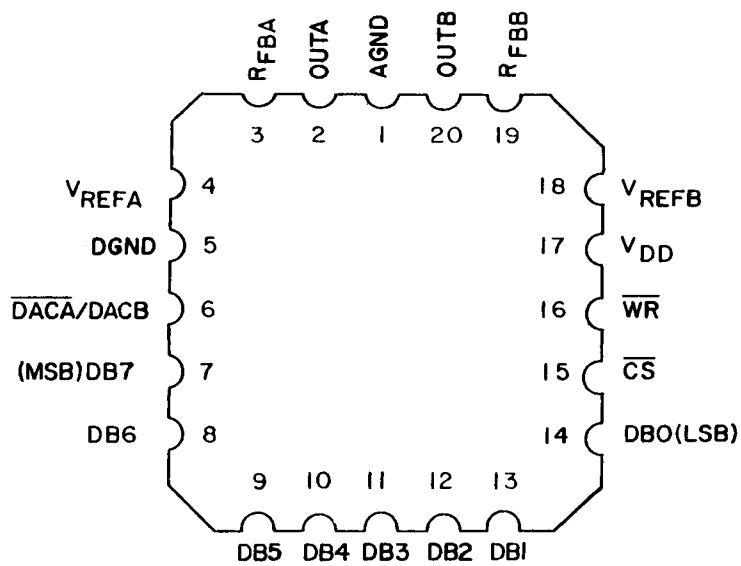
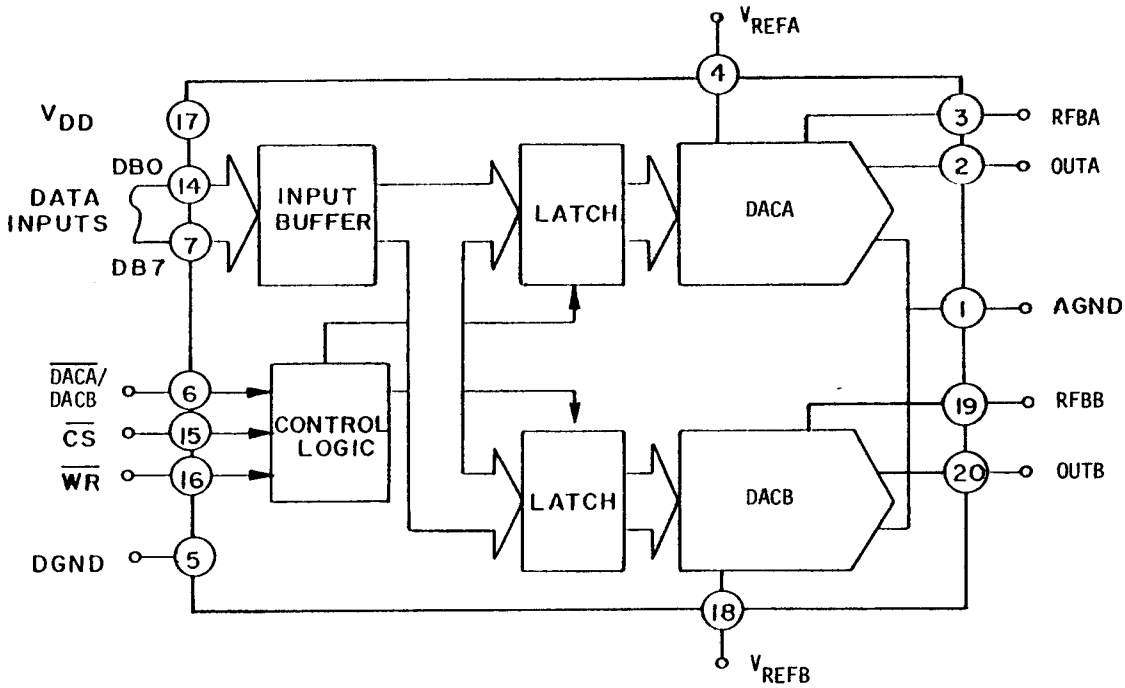


FIGURE 1. Terminal connections.

STANDARDIZED MILITARY DRAWING DEFENSE ELECTRONICS SUPPLY CENTER DAYTON, OHIO 45444	SIZE A		5962-87701
		REVISION LEVEL A	SHEET 11

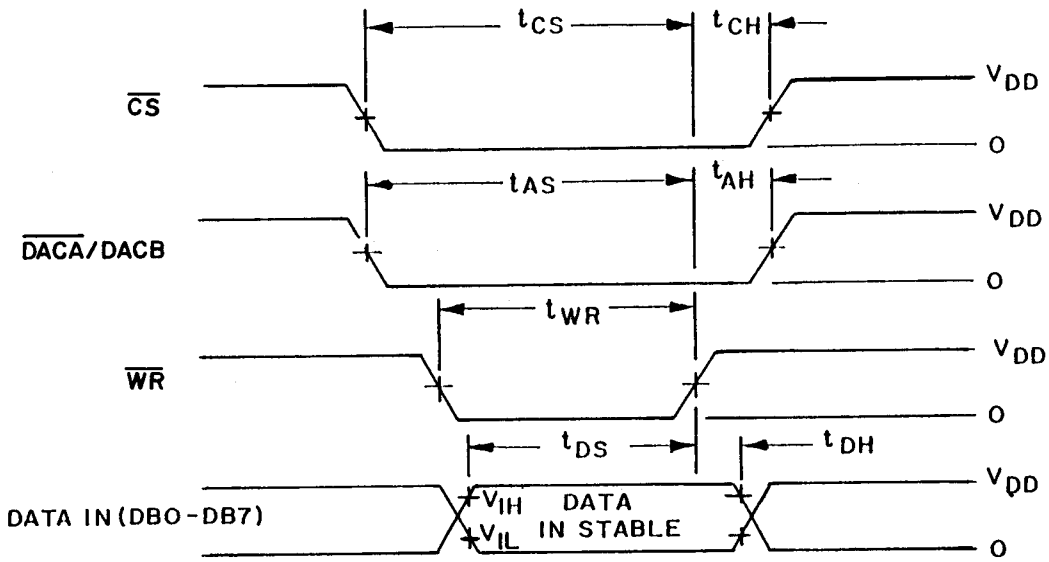


Mode selection table

DACA/ DACB	CS	WR	DACA	DACB
L	L	L	Write	Hold
H	L	L	Hold	Write
X	H	X	Hold	Hold
X	X	H	Hold	Hold

L = Low state
H = High state
X = Don't care

FIGURE 2. Functional diagram and mode selection.



NOTES:
1. All input signal rise and fall times measured from 10% to 90% of V_{pp}.
   V_{pp} = +5 V, $t_r = t_f$ = 20 ns;
   V_{pp} = +15 V, $t_r = t_f$ = 40 ns.
2. Timing measurement reference level is $\frac{V_{IH} + V_{IL}}{2}$.

FIGURE 3. Write cycle timing diagram.

4.2 Screening. Screening shall be in accordance with method 5004 of MIL-STD-883, and shall be conducted on all devices prior to quality conformance inspection. The following additional criteria shall apply:

a. Burn-in test, method 1015 of MIL-STD-883.

(1) Test condition A, B, C, or D using the circuit submitted with the certificate of compliance (see 3.5 herein).

(2) T_A = +125°C, minimum.

b. Interim and final electrical test parameters shall be as specified in table II herein, except interim electrical parameter tests prior to burn-in are optional at the discretion of the manufacturer.

c. Optional subgroup 12 is used for grading and part selection at +25°C, it is not included in PDA.

4.3 Quality conformance inspection. Quality conformance inspection shall be in accordance with method 5005 of MIL-STD-883 including groups A, B, C, and D inspections. The following additional criteria shall apply.

4.3.1 Group A inspection.

a. Tests shall be as specified in table II herein.

b. Subgroups 7 and 8 in table I, method 5005 of MIL-STD-883 shall be omitted.

c. Subgroup 4 (C_{IN} measurement) shall be measured only for the initial test and after process or design changes which may affect input capacitance.

d. Optional subgroup 12 is used for grading and part selection at +25°C.

4.3.2 Groups C and D inspections.

a. End-point electrical parameters shall be as specified in table II herein.

b. Steady-state life test conditions, method 1005 of MIL-STD-883.

(1) Test condition A, B, C, or D using the circuit submitted with the certificate of compliance (see 3.5 herein).

(2) T_A = +125°C, minimum.

(3) Test duration: 1,000 hours, except as permitted by method 1005 of MIL-STD-883.

TABLE II. Electrical test requirements.

MIL-STD-883 test requirements	Subgroups (per method 5005, table I)
Interim electrical parameters (method 5004)	1
Final electrical test parameters (method 5004)	1*,2,3,12
Group A test requirements (method 5005)	1,2,3,4,5,6,9, 10**,11**,12
Groups C and D end-point electrical parameters (method 5005)	1

* PDA applies to subgroup 1.
** Subgroups 10 and 11, if not tested, shall be guaranteed to the specified limits in table I.

5. PACKAGING

5.1 Packaging requirements. The requirements for packaging shall be in accordance with MIL-M-38510.

6. NOTES

6.1 Intended use. Microcircuits conforming to this drawing are intended for use when military specifications do not exist and qualified military devices that will perform the required function are not available for OEM application. When a military specification exists and the product covered by this drawing has been qualified for listing on QPL-38510, the device specified herein will be inactivated and will not be used for new design. The QPL-38510 product shall be the preferred item for all applications.

6.2 Replaceability. Microcircuits covered by this drawing will replace the same generic device covered by a contractor-prepared specification or drawing.

6.3 Comments. Comments on this drawing should be directed to DESC-ECS, Dayton, Ohio 45444, or telephone 513-296-5375.

6.4 Approved sources of supply. Approved sources of supply are listed herein. Additional sources will be added as they become available. The vendors listed herein have agreed to this drawing and a certificate of compliance (see 3.5 herein) has been submitted to DESC-ECS.

Military drawing part number	Vendor CAGE number	Vendor similar part number 1/
5962-8770101RX	24355	AD7528SQ/883B
	54186	MP7528SD/883
	06665	PM7528BR/883B
5962-87701012X	24355	AD7528SE/883B
	54186	MP7528SL/883
	06665	PM7528BRC/883B
5962-8770102RX	24355	AD7528TQ/883B
	54186	MP7528TD/883
	06665	PM7528BR/883B
5962-87701022X	24355	AD7528TE/883B
	54186	MP7528TL/883
	06665	PM7528BRC/883B
5962-8770103RX	24355	AD7528UQ/883B
	54186	MP7528UD/883
	06665	PM7528AR/883B
5962-87701032X	24355	AD7528UE/883B
	54186	MP7528UL/883
	06665	PM7528ARC/883B

1/ Caution. Do not use this number for item acquisition. Items acquired to this number may not satisfy the performance requirements of this drawing.

Vendor CAGE number	Vendor name and address
06665	Precision Monolithics Incorporated 1500 Space Park Drive Santa Clara, CA 95050
24355	Analog Devices 1 Technology Way Norwood, MA 02062
54186	Micro Power Systems 3100 Alfred Street Santa Clara, CA 95054