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LTR	DESCRIPTION	DATE (YR-MO-DA)	APPROVED																
A	Change to table I parameter t_{SCT} . Correction to vendor similar part number. Editorial changes throughout.	1990 JAN 08	<i>M. J. Long</i>																

REV	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15
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REV STATUS OF SHEETS	REV	A		A		A							A	A	A
	SHEET	1	2	3	4	5	6	7	8	9	10	11	12	13	14

PMIC N/A STANDARDIZED MILITARY DRAWING THIS DRAWING IS AVAILABLE FOR USE BY ALL DEPARTMENTS AND AGENCIES OF THE DEPARTMENT OF DEFENSE AMSC N/A	PREPARED BY <i>James E. Jamison</i> CHECKED BY <i>Charles Reusing</i> APPROVED BY <i>M. J. Long</i> DRAWING APPROVAL DATE 12 January 1988 REVISION LEVEL A	DEFENSE ELECTRONICS SUPPLY CENTER DAYTON, OHIO 45444 MICROCIRCUITS, MEMORY, DIGITAL, 512 X 8 BIT NONVOLATILE STATIC RAM, MONOLITHIC SILICON <table style="width: 100%;"> <tr> <td style="width: 15%;">SIZE A</td> <td style="width: 35%;">CAGE CODE 67268</td> <td style="width: 50%;">5962-87712</td> </tr> <tr> <td colspan="3">SHEET 1 OF 1</td> </tr> </table>	SIZE A	CAGE CODE 67268	5962-87712	SHEET 1 OF 1		
SIZE A	CAGE CODE 67268	5962-87712						
SHEET 1 OF 1								

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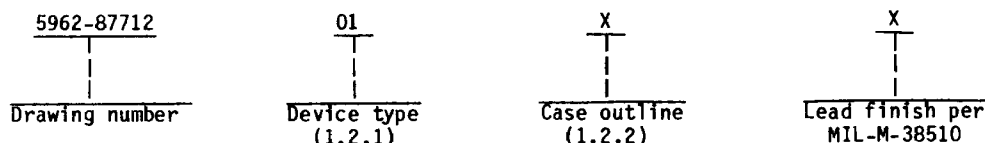
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5962-E1476

1. SCOPE

1.1 Scope. This drawing describes device requirements for class B microcircuits in accordance with 1.2.1 of MIL-STD-883, "Provisions for the use of MIL-STD-883 in conjunction with compliant non-JAN devices".

1.2 Part number. The complete part number shall be as shown in the following example:



1.2.1 Device types. The device types shall identify the circuit function as follows:

Device type	Generic number	Circuit function	Access time
01	2004	512 x 8 bit, nonvolatile static RAM	250 ns
02	2004	512 x 8 bit, nonvolatile static RAM	300 ns

1.2.2 Case outlines. The case outlines shall be as designated in appendix C of MIL-M-38510, and as follows:

Outline letter	Case outline
X	D-10 (28-lead, .600" row spacing) dual-in-line package
Y	C-12 (32-terminal, .560" x .458" x .120") rectangular chip carrier package

1.3 Absolute maximum ratings.

Temperature under bias	-65°C to +135°C
Storage temperature	-65°C to +150°C
Voltage on any pin with respect to ground	-1.0 V to +7.0 V dc
DC output current	5.0 mA
Lead temperature (soldering, 10 seconds)	300°C
Power dissipation (P _D)	0.75 W
Thermal resistance, junction-to-case (θ _{JC})	See MIL-M-38510, appendix C
Junction temperature (T _J)	200°C

1.4 Recommended operating conditions.

Supply voltage (V _{CC})	4.5 V dc to 5.5 V dc
Minimum high level input voltage (V _{IH})	+2.3 V dc
Maximum high level input voltage (V _{IH})	+V _{CC} + 0.5 V dc
Minimum low level input voltage (V _{IL})	-0.5 V dc
Maximum low level input voltage (V _{IL})	+0.8 V dc
Case operating temperature range (T _C)	-55°C to +125°C

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2. APPLICABLE DOCUMENTS

2.1 Government specification, standard, and bulletin. Unless otherwise specified, the following specification, standard, and bulletin of the issue listed in that issue of the Department of Defense Index of Specifications and Standards specified in the solicitation, form a part of this drawing to the extent specified herein.

SPECIFICATION

MILITARY

MIL-M-38510 - Microcircuits, General Specification for.

STANDARD

MILITARY

MIL-STD-883 - Test Methods and Procedures for Microelectronics.

BULLETIN

MILITARY

MIL-BUL-103 - List of Standardized Military Drawings (SMD's).

(Copies of the specification, standard, and bulletin required by manufacturers in connection with specific acquisition functions should be obtained from the contracting activity or as directed by the contracting activity.)

2.2 Order of precedence. In the event of a conflict between the text of this drawing and the references cited herein, the text of this drawing shall take precedence.

3. REQUIREMENTS

3.1 Item requirements. The individual item requirements shall be in accordance with 1.2.1 of MIL-STD-883, "Provisions for the use of MIL-STD-883 in conjunction with compliant non-JAN devices" and as specified herein.

3.2 Design, construction, and physical dimensions. The design, construction, and physical dimensions shall be as specified in MIL-M-38510 and herein.

3.2.1 Terminal connections. The terminal connections shall be as specified on figure 1.

3.2.2 Truth table. The truth table shall be as specified on figure 2.

3.2.3 Block diagram. The block diagram shall be as specified on figure 3.

3.2.4 Case outlines. The case outlines shall be in accordance with 1.2.2 herein.

3.3 Electrical performance characteristics. Unless otherwise specified herein, the electrical performance characteristics are as specified in table I and apply over the full case operating temperature range.

3.4 Electrical test requirements. The electrical test requirements shall be the subgroups specified in table II. The electrical tests for each subgroup are described in table I.

3.5 Marking. Marking shall be in accordance with MIL-STD-883 (see 3.1 herein). The part shall be marked with the part number listed in 1.2 herein. In addition, the manufacturer's part number may also be marked as listed in MIL-BUL-103 (see 6.6 herein).

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TABLE I. Electrical performance characteristics.

Test	Symbol	Conditions -55°C < T _C < +125°C V _{SS} = 0 V, 4.5 V < V _{CC} < 5.5 V unless otherwise specified	Device type	Group A subgroups	Limits		Unit
					Min	Max	
Input low voltage	V _{IL}		1,2,3	01,02	-0.1	0.8	V
Input high voltage	V _{IH}		1,2,3	01,02	2.0	V _{CC} + 1.0	V
Output low voltage	V _{OL}	I _{OL} = 2.1 mA	1,2,3	01,02		0.4	V
Output high voltage	V _{OH}	I _{OH} = -400 µA	1,2,3	01,02	2.4		V
Power supply current (active)	I _{CC1}	T _E = V _{IL} , I _{I/O} = 0 mA, all other inputs = V _{CC}	1,2,3	01,02		120	mA
Power supply current (standby)	I _{CC2}	All inputs = V _{CC} , I _{I/O} = 0 mA	1,2,3	01,02		90	mA
Input capacitance	C _{IN}	V _{I/O} = 0 V, T _A = 25°C, frequency = 1.0 MHz <u>1/</u> see 4.3.1c	4	01,02		6	pF
Output capacitance	C _{OUT}	V _{I/O} = 0 V, T _A = 25°C, frequency = 1.0 MHz <u>1/</u> see 4.3.1c	4	01,02		10	pF
Read cycle time	t _{AVAV}	See figure 4 <u>2/</u>	9,10,11	01	250		ns
				02	300		
Chip enable access time	t _{ELDV}	See figure 4 <u>2/</u>	9,10,11	01		250	ns
				02		300	
Address access time	t _{AVAQ}	See figure 4 <u>2/</u>	9,10,11	01		250	ns
				02		300	
Output enable access time	t _{OLQV}	See figure 4 <u>2/</u>	9,10,11	01		100	ns
				02		150	
Chip enable output to low Z	t _{ELDX}	See figure 4 <u>2/</u>	9,10,11	01,02	10		ns

See footnotes at end of table.

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TABLE I. Electrical performance characteristics - Continued.

Test	Symbol	Conditions -55°C < T _C < +125°C V _{SS} = 0 V, 4.5 V < V _{CC} ≤ 5.5 V unless otherwise specified	Device type	Group A subgroups	Limits		Unit
					Min	Max	
Chip enable output to high Z	t _{ELDZ}	See figure 4 <u>2/</u>	9,10,11	01,02	10	100	ns
Output enable output to low Z	t _{OLQX}	See figure 4 <u>2/</u>	9,10,11	01,02	10		ns
Output enable output to high Z	t _{OHQZ}	See figure 4 <u>2/</u>	9,10,11	01,02	10	100	ns
Output hold from address change	t _{AVQX}	See figure 4 <u>1/ 2/</u>	9,10,11	01,02	0		ns
Write cycle time	t _{ELEH}	See figure 5 <u>2/</u>	9,10,11	01	250		ns
				02	300		
Chip enable to end of write input	t _{ELWH}	See figure 5 <u>2/</u>	9,10,11	01	250		ns
				02	300		
Address setup time	t _{AVWL}	See figure 5 <u>2/</u>	9,10,11	01,02	0		ns
Write pulse width	t _{WLWH}	See figure 5 <u>2/</u>	9,10,11	01	150		ns
				02	200		
Write recovery time	t _{EHAX}	See figure 5 <u>2/</u>	9,10,11	01,02	0		ns
Data valid to end of write cycle	t _{DVWH}	See figure 5 <u>2/</u>	9,10,11	01	150		ns
				02	200		
Data hold time	t _{WHDX}	See figure 5 <u>2/</u>	9,10,11	01,02	0		ns
Write enable to output in high Z	t _{WLQZ}	See figure 5 <u>2/</u>	9,10,11	01,02	10	100	ns
Output active from end of write cycle	t _{WHQX}	See figure 5 <u>2/</u>	9,10,11	01,02	10		ns
Output enable to output in high Z	t _{OHQZ}	See figure 5 <u>2/</u>	9,10,11	01,02	10	100	ns
Store cycle time	t _{SCT}	See figure 6 <u>2/</u>	9,10,11	01,02		10	ms

See footnotes at end of table.

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TABLE 1. Electrical performance characteristics - Continued.

Test	Symbol	Conditions -55°C < T _C < +125°C V _{SS} = 0 V, 4.5 V < V _{CC} < 5.5 V unless otherwise specified	Device type	Group A subgroups	Limits		Unit
					Min	Max	
Store pulse width	t _{SP}	See figure 6 <u>2/</u>	9,10,11	01	150		ns
				02	200		
Nonvolatile enable to output in high Z	t _{NHZ}	See figure 6 <u>2/</u>	9,10,11	01,02		100	ns
Output enable from end of store	t _{OEST}	See figure 6 <u>2/</u>	9,10,11	01,02	10		ns
OE Disable to store function	t _{SOE}	See figure 6 <u>2/</u>	9,10,11	01,02	20		ns
NE setup time from WE	t _{NS}	See figure 6 <u>2/</u>	9,10,11	01,02	0		ns
Array recall cycle time	t _{RCC}	See figure 6 <u>2/</u>	9,10,11	01,02		5	μs
Recall pulse width to initiate recall	t _{RCP}	See figure 6 <u>2/ 3/</u>	9,10,11	01	150		ns
				02	200		
WE setup to NE	t _{RWE}	See figure 6 <u>2/</u>	9,10,11	01,02	0		ns

1/ Tested initially and after any design or process changes which may affect this parameter, and is guaranteed to the limits specified in table 1.

2/ AC test conditions:
 Input high level V_{IH} = 3.0 V.
 Input low level V_{IL} = 0.0 V.
 Input rise/fall times t_R = 10 ns.
 Output voltage high V_{IH} > 1.5 V.
 Output voltage low V_{IL} < 1.5 V.
 Output load C_L = 100 pF.
 Input and output timing levels = 1.5 V.

3/ This device features internal control of the recall cycle time, t_{RCP} is the minimum input pulse width required to initiate a recall. Once initiated, the recall cycle will have a completion time of t_{RDV} which varies. As t_{RCP} is increased above its minimum value, the cycle time t_{RCC} remains constant and t_{RDV} is reduced accordingly until reaching its minimum value. If t_{RCP} is increased further, t_{RDV} remains constant and the entire cycle time will increase.

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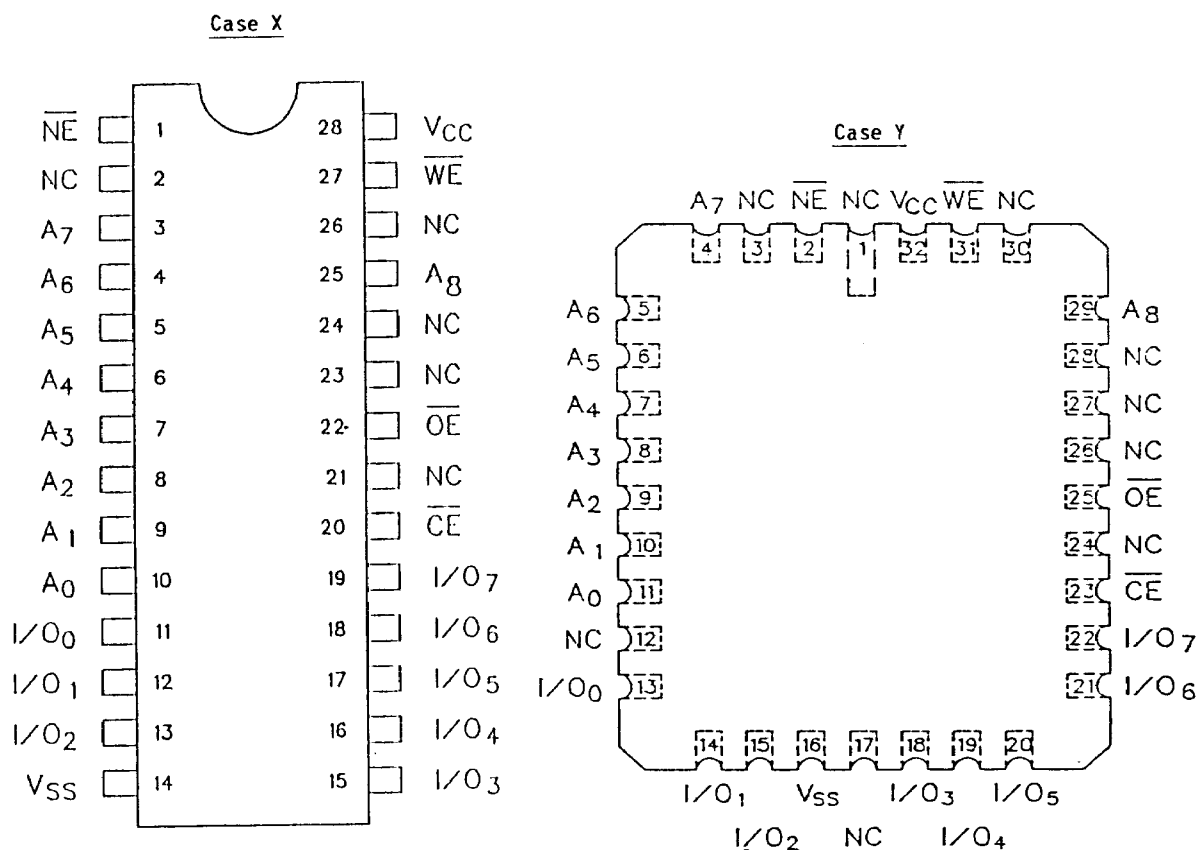


FIGURE 1. Terminal connections.

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CE	WE	NE	OE	Mode	I/O	Power
H	X	X	X	Not selected	Output high Z	Standby
L	H	H	L	Read RAM	Output data	Active
L	L	H	X	Write "1" into RAM	Input data high	Active
L	L	H	X	Write "0" into RAM	Input data low	Active
L	H	L	L	Array recall	Output high Z	Active
L	L	L	H	Nonvolatile storage	Output high Z	Active
L	H	H	H	Output disable	Output high Z	Active
L	L	L	L	Not allowed	Output high Z	Active
L	H	L	H	No operation	Output high Z	Active

FIGURE 2. Truth table.

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Device types 01 and 02

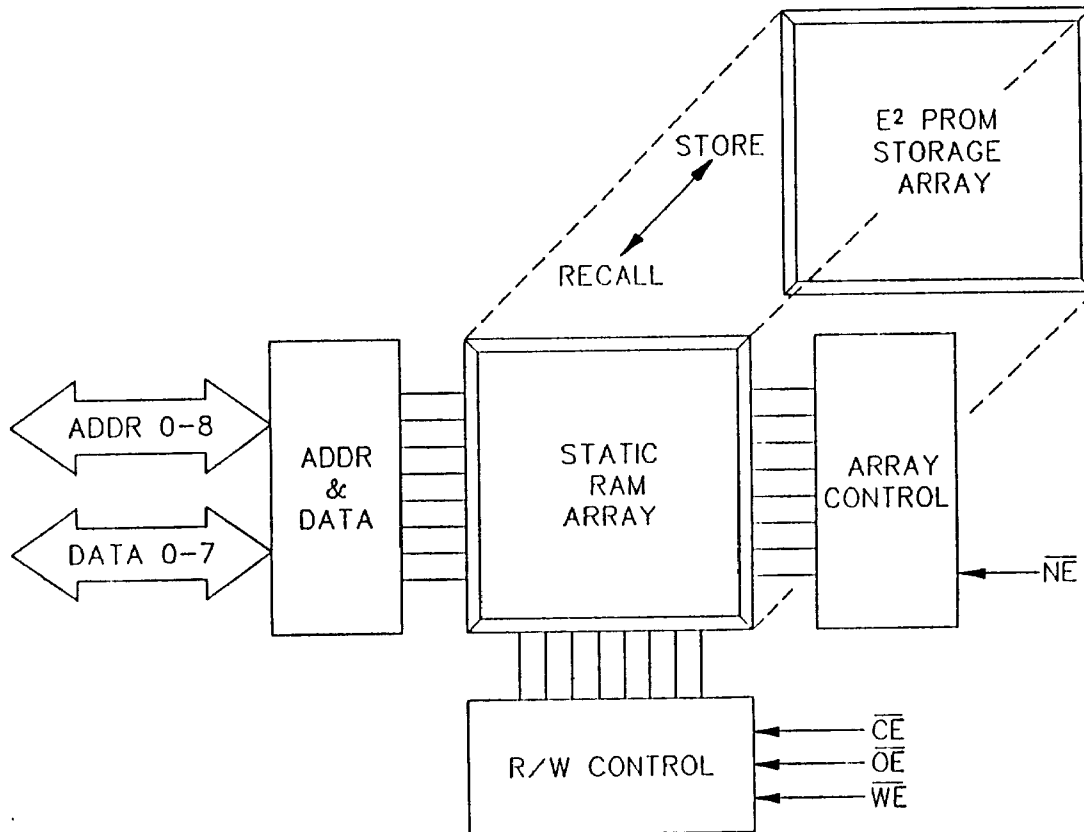


FIGURE 3. Block diagram.

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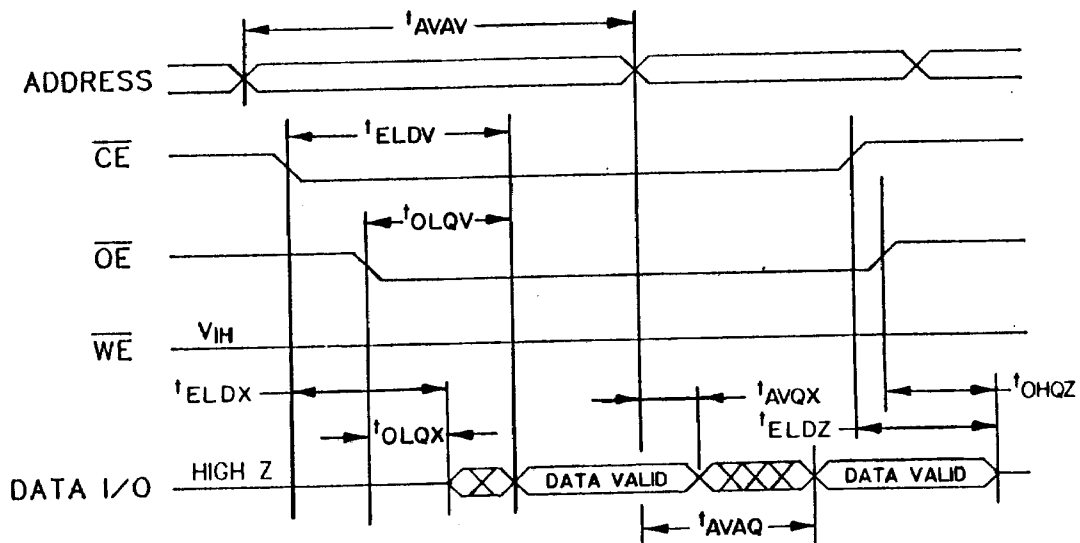


FIGURE 4. Switching waveforms (read cycle).

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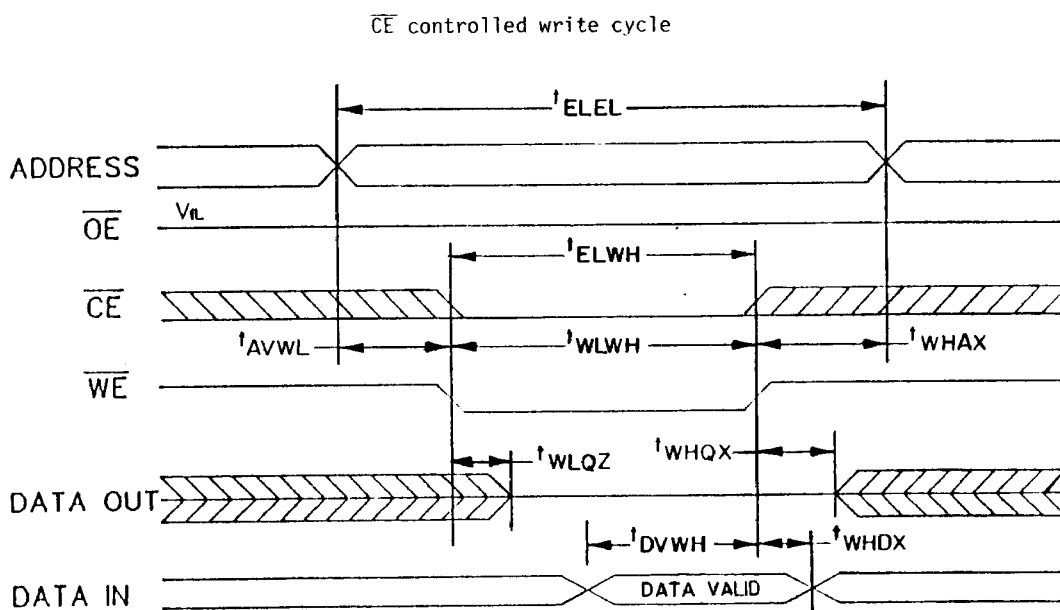
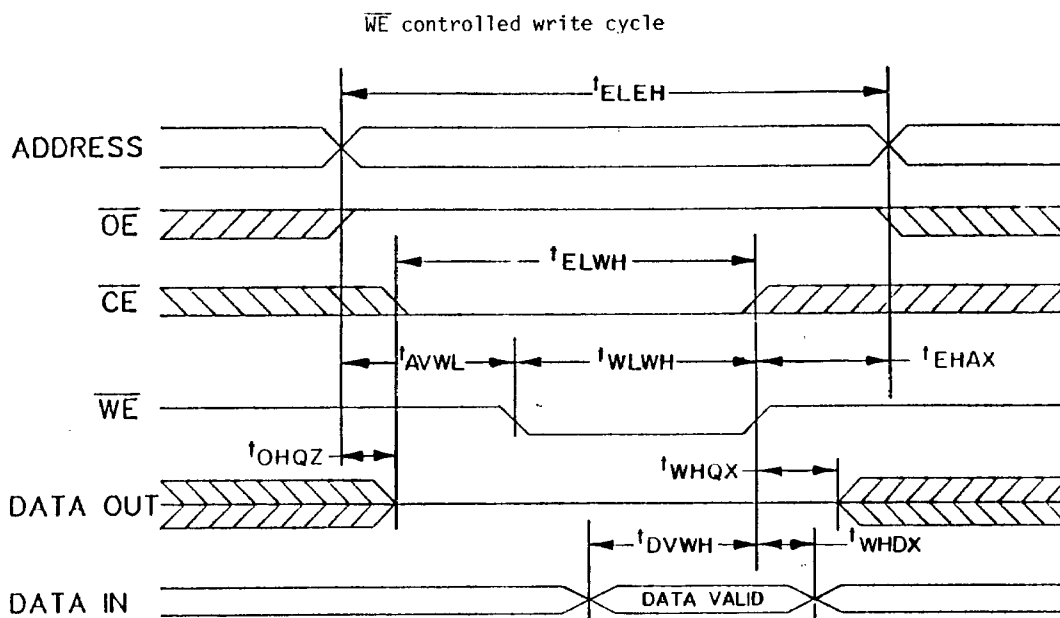


FIGURE 5. Switching waveforms (write cycle).

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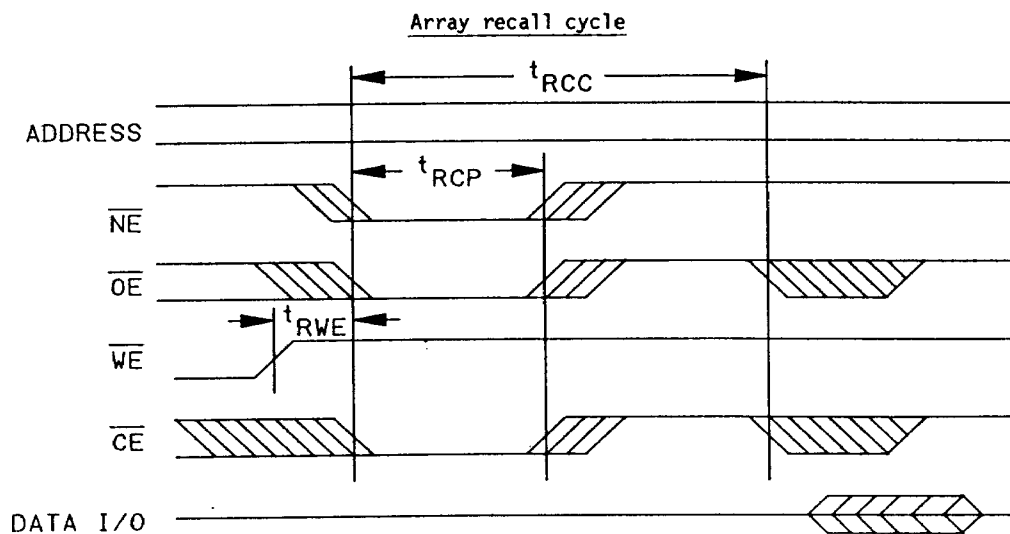
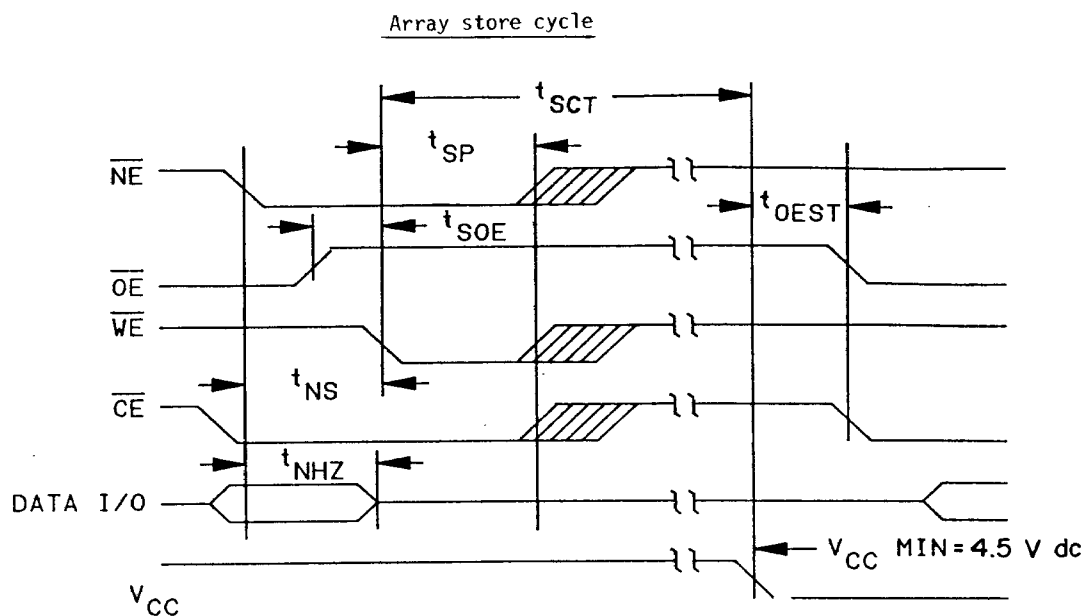


FIGURE 6. Switching waveforms (store/recall cycle).

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3.6 Certificate of compliance. A certificate of compliance shall be required from a manufacturer in order to be listed as an approved source of supply in MIL-BUL-103 (see 6.6 herein). The certificate of compliance submitted to DESC-ECS prior to listing as an approved source of supply shall affirm that the manufacturer's product meets the requirements of MIL-STD-883 (see 3.1 herein) and the requirements herein.

3.7 Certificate of conformance. A certificate of conformance as required in MIL-STD-883 (see 3.1 herein) shall be provided with each lot of microcircuits delivered to this drawing.

3.8 Notification of change. Notification of change to DESC-ECS shall be required in accordance with MIL-STD-883 (see 3.1 herein).

3.9 Verification and review. DESC, DESC's agent, and the acquiring activity retain the option to review the manufacturer's facility and applicable required documentation. Offshore documentation shall be made available onshore at the option of the reviewer.

4. QUALITY ASSURANCE PROVISIONS

4.1 Sampling and inspection. Sampling and inspection procedures shall be in accordance with section 4 of MIL-M-38510 to the extent specified in MIL-STD-883 (see 3.1 herein).

4.2 Screening. Screening shall be in accordance with method 5004 of MIL-STD-883, and shall be conducted on all devices prior to quality conformance inspection. The following additional criteria shall apply:

a. Burn-in test, method 1015 of MIL-STD-883.

(1) Test condition C or D using the circuit submitted with the certificate of compliance (see 3.6 herein).

(2) $T_A = +125^{\circ}\text{C}$, minimum.

b. Interim and final electrical test parameters shall be as specified in table II herein, except interim electrical parameter tests prior to burn-in are optional at the discretion of the manufacturer.

4.3 Quality conformance inspection. Quality conformance inspection shall be in accordance with method 5005 of MIL-STD-883 including groups A, B, C, and D inspections. The following additional criteria shall apply.

4.3.1 Group A inspection.

a. Tests shall be as specified in table II herein.

b. Subgroups 5 and 6 in table I, method 5005 of MIL-STD-883 shall be omitted.

c. Subgroup 4 (C_{IN} and C_{OUT} measurements) shall be measured only for the initial qualification and after process or design changes which may affect capacitance. Sample size is 15 devices with no failures, and all input and output terminals tested.

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TABLE II. Electrical test requirements.

MIL-STD-883 test requirements	Subgroups (per method 5005, table I)
Interim electrical parameters (method 5004)	---
Final electrical test parameters (method 5004)	1*,2,3,7*,8, 9,10,11
Group A test requirements (method 5005)	1,2,3,4**,7,8, 9,10,11
Groups C and D end-point electrical parameters (method 5005)	2,8(Hot),10

* PDA applies to subgroups 1 and 7.
** See 4.3.1c.

4.3.2 Groups C and D inspections.

- End-point electrical parameters shall be as specified in table II herein.
- Steady-state life test conditions, method 1005 of MIL-STD-883:
 - Test condition C or D using the circuit submitted with the certificate of compliance (see 3.6 herein).
 - $T_A = +125^\circ\text{C}$, minimum.
 - Test duration: 1,000 hours, except as permitted by method 1005 of MIL-STD-883.

5. PACKAGING

5.1 Packaging requirements. The requirements for packaging shall be in accordance with MIL-M-38510.

6. NOTES

6.1 Intended use. Microcircuits conforming to this drawing are intended for use when military specifications do not exist and qualified military devices that will perform the required function are not available for OEM application. When a military specification exists and the product covered by this drawing has been qualified for listing on QPL-38510, the device specified herein will be inactivated and will not be used for new design. The QPL-38510 product shall be the preferred item for all applications.

6.2 Replaceability. Microcircuits covered by this drawing will replace the same generic device covered by a contractor-prepared specification or drawing.

6.3 Configuration control of SMD's. All proposed changes to existing SMD's will be coordinated with the users of record for the individual documents. This coordination will be accomplished in accordance with MIL-STD-481 using DD Form 1693, Engineering Change Proposal (Short Form).

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6.4 Record of users. Military and industrial users shall inform the Defense Electronics Supply Center when a system application requires configuration control and the applicable SMD. DESC will maintain a record of users and this list will be used for coordination and distribution of changes to the drawings. Users of drawings covering microelectronics devices (FSC 5962) should contact DESC-ECS, telephone (513) 296-6022.

6.5 Comments. Comments on this drawing should be directed to DESC-ECS, Dayton, Ohio 45444, or telephone (513) 296-5375.

6.6 Approved source of supply. An approved source of supply is listed in MIL-BUL-103. Additional sources will be added to MIL-BUL-103 as they become available. The vendor listed in MIL-BUL-103 has agreed to this drawing and a certificate of compliance (see 3.6 herein) has been submitted to and accepted by DESC-ECS. The approved source of supply listed below is for information purposes only and is current only to the last action of this document.

Military drawing part number	Vendor CAGE number	Vendor similar part number <u>1/</u>
5962-8771201XX	60395	X2004DMB-25
5962-8771201YX	60395	X2004EMB-25
5962-8771202XX	60395	X2004DMB
5962-8771202YX	60395	X2004EMB

1/ Caution. Do not use this number for item acquisition. Items acquired to this number may not satisfy the performance requirements of this drawing.

Vendor CAGE
number

60395

Vendor name
and address

XICOR, Incorporated
851 Buckeye Court
Milpitas, CA 95035

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