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Defense Electronics Supply Center
Dayton, Ohio

Original date of drawing:
09 October 1987

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SIZE	CODE IDENT. NO.
A	67268

REV

MILITARY DRAWING

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TITLE: MICROCIRCUIT, DIGITAL, 1M (64K x 16) BIT, NMOS, UVEPROM, MONOLITHIC SILICON

DWG NO. 5962-87744

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5962-E641

DISTRIBUTION STATEMENT A. Approved for public release; distribution is unlimited.

DESC FORM 193
MAY 86

1. SCOPE

1.1 Scope. This drawing describes device requirements for class B microcircuits in accordance with 1.2.1 of MIL-STD-883, "Provisions for the use of MIL-STD-883 in conjunction with compliant non-JAN devices".

1.2 Part number. The complete part number shall be as shown in the following example:

5962-87744	01	Q	X
Drawing number	Device type (1.2.1)	Case outline (1.2.2)	Lead finish per MIL-M-38510

1.2.1 Device types. The device types shall identify the circuit function as follows:

Device type	Generic number	Circuit function	Access time
01	(See 6.4)	1M (64K x 16) UVEPROM	200 ns
02	(See 6.4)	1M (64K x 16) UVEPROM	250 ns

1.2.2 Case outline. The case outline shall be as designated in appendix C of MIL-M-38510, and as follows:

Outline letter	Case outline
Q	D-5 (40-lead, 9/16" x 2 1/16"), dual-in-line package 1/

1.3 Absolute maximum ratings.

Storage temperature	-65°C to +125°C
All input or output voltage with respect to ground	-0.6 V dc to +6.25 V dc
Voltage on A_9 with respect to ground	-0.6 V dc to +13.0 V dc
V_{PP} supply voltage with respect to ground during programming	-0.6 V dc to +14.0 V dc
V_{CC} supply voltage with respect to ground	-0.6 V dc to +7.0 V dc
Power dissipation (P_D)	1.1 W
Lead temperature (soldering, 10 seconds)	+300°C
Thermal resistance, junction-to-case (O_{JC}) Case Q	See MIL-M-38510, appendix C
Junction temperature (T_J)	+200°C

1.4 Recommended operating conditions.

Case operating temperature range (T_C)	-55°C to +125°C
Supply voltage (V_{CC})	5 V dc ±10%

1/ Lid shall be transparent to permit ultraviolet light erasure.

2. APPLICABLE DOCUMENTS

2.1 Government specification and standard. Unless otherwise specified, the following specification and standard, of the issue listed in that issue of the Department of Defense Index of Specifications and Standards specified in the solicitation, form a part of this drawing to the extent specified herein.

SPECIFICATION

MILITARY

MIL-M-38510 - Microcircuits, General Specification for.

STANDARD

MILITARY

MIL-STD-883 - Test Methods and Procedures for Microelectronics.

(Copies of the specification and standard required by manufacturers in connection with specific acquisition functions should be obtained from the contracting activity or as directed by the contracting activity.)

2.2 Order of precedence. In the event of a conflict between the text of this drawing and the references cited herein, the text of this drawing shall take precedence.

3. REQUIREMENTS

3.1 Item requirements. The individual item requirements shall be in accordance with 1.2.1 of MIL-STD-883, "Provisions for the use of MIL-STD-883 in conjunction with compliant non-JAN devices" and as specified herein.

3.2 Design, construction, and physical dimensions. The design, construction, and physical dimensions shall be as specified in MIL-M-38510 and herein.

3.2.1 Terminal connections. The terminal connections shall be as specified on figure 1.

3.2.2 Truth table. The truth table shall be as specified on figure 2.

3.2.2.1 Unprogrammed or erased devices. The truth table for unprogrammed devices shall be as specified on figure 2.

3.2.2.2 Programmed devices. The requirements for supplying programmed devices are not part of this drawing.

3.2.3 Block diagram. The block diagram shall be as specified on figure 3.

3.2.4 Case outline. The case outline shall be in accordance with 1.2.2 herein.

3.3 Electrical performance characteristics. Unless otherwise specified, the electrical performance characteristics are as specified in table I and apply over the full recommended case operating temperature range.

3.4 Marking. Marking shall be in accordance with MIL-STD-883 (see 3.1 herein). The part shall be marked with the part number listed in 1.2 herein. In addition, the manufacturer's part number may also be marked as listed in 6.4 herein.

TABLE I. Electrical performance characteristics.

Test	Symbol	Conditions $-55°C < T_C < +125°C$ $V_{CC} = 5\ V \pm 10\%$ unless otherwise specified	Group A subgroups	Device types	Limits		Unit
					Min	Max	
Input load current	I_{LI}	$V_{IN} = 5.5\ V$	1,2,3	All		1	µA
Output leakage current	I_{LO}	$V_{OUT} = 5.5\ V$	1,2,3	All		1	µA
V_{PP} load current read	I_{PP1}	$V_{PP} = 5.5\ V$	1,2,3	All		1	µA
V_{CC} current standby	I_{SB}	$\overline{CE} = V_{IH}$	1,2,3	All		50	mA
V_{CC} current active	I_{CC}	$\overline{CE} = \overline{OE} = V_{IL}$	1,2,3	All		200	mA
Input low voltage	V_{IL}		1,2,3	All	-0.1 (1)	0.8	V
Input high voltage	V_{IH}		1,2,3	All	2.0	V_{CC} +1 1/	V
Output low voltage	V_{OL}	$I_{OL} = 2.1\ mA$	1,2,3	All		0.45	V
Output high voltage	V_{OH}	$I_{OH} = -400\ \mu A$	1,2,3	All	2.0		V
Input capacitance	C_{IN} 1/	$T_C = +25°C$, f = 1 MHz $V_{IN} = 0\ V$	4	All		6	pF
Output capacitance	C_{OUT} 1/	$T_C = +25°C$, f = 1 MHz $V_{OUT} = 0\ V$	4	All		12	pF
V_{PP} input capacitance	C_{VPP} 1/	$T_C = +25°C$, f = 1 MHz $V_{PP} = 0\ V$	4	All		25	pF
Address to output delay	t_{ACC}	See figures 4 and 5	9,10,11	01 02		200 250	ns ns
$\overline{CE}$ to output delay	t_{CE}	See figures 4 and 5	9,10,11	01 02		200 250	ns ns

See footnote at end of table.

TABLE I. Electrical performance characteristics - Continued.

Test	Symbol	Conditions $-55°C \le T_C \le +125°C$, $V_{CC} = 5\ V \pm 10\%$ unless otherwise specified	Group A subgroups	Device types	Limits		Unit
					Min	Max	
$\overline{OE}$ to output delay	t_{OE}	See figures 4 and 5	9,10,11	01 02		80 85	ns ns
$\overline{OE}$ high to output float	t_{DF} 1/	See figures 4 and 5	9,10,11	All	0	60	ns
Output hold from addresses, $\overline{CE}$ or $\overline{OE}$ whichever occurred first	t_{OH} 1/	See figures 4 and 5	9,10,11	All	0		ns

1/ Guaranteed but not tested.

3.5 Processing EPROMS. All testing requirements and quality assurance provisions herein shall be satisfied by the manufacturer prior to deliver.

3.5.1 Erasure of EPROMS. When specified, devices shall be erased in accordance with the procedures and characteristics specified in 4.4.

3.5.2 Programmability of EPROMS. When specified, devices shall be programmed to the specified pattern using the procedures and characteristics specified in 4.5 and table III.

3.5.3 Verification of erasure of programmability of EPROMS. When specified, devices shall be verified as either programmed to the specified pattern or erased. As a minimum, verification shall consist of performing a functional test (subgroup 7) to verify that all bits are in the proper state. Any bit that does not verify to be in the proper state shall constitute a device failure, and shall be removed from the lot.

3.6 Certificate of compliance. A certificate of compliance shall be required from a manufacturer in order to be listed as an approved source of supply in 6.4. The certificate of compliance submitted to DESC-ECS prior to listing as an approved source of supply shall state that the manufacturer's product meets the requirements of MIL-STD-883 (see 3.1 herein) and the requirements herein.

3.7 Certificate of conformance. A certificate of conformance as required in MIL-STD-883 (see 3.1 herein) shall be provided with each lot of microcircuits delivered to this drawing.

3.8 Notification of change. Notification of change to DESC-ECS shall be required in accordance with MIL-STD-883 (see 3.1 herein).

3.9 Verification and review. DESC, DESC's agent, and the acquiring activity retain the option to review the manufacturer's facility and applicable required documentation. Offshore documentation shall be made available onshore at the option of the reviewer.

Pin names

A_0-A_{17}	Address
$\overline{CE}$	Chip enable
$\overline{OE}$	Output enable
O_0-O_{15}	Outputs
$\overline{PRGM}$	Program
NC	No connection

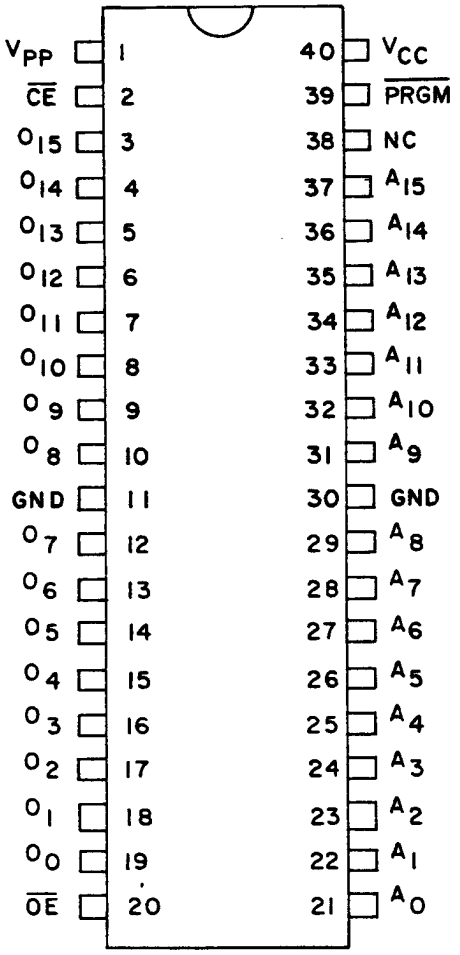


FIGURE 1. Terminal connections.

Pins / Mode		$\overline{CE}$	$\overline{OE}$	$\overline{PRGM}$	A_9	A_0	V_{PP}	V_{CC}	Outputs
Read		V_{IL}	V_{IL}	X	X(1)	X	X	5.0 V	D_{OUT}
Output disable		V_{IL}	V_{IH}	X	X	X	X	5.0 V	HIGH Z
Standby		V_{IH}	X	X	X	X	X	5.0 V	HIGH Z
Programming		V_{IL}	V_{IH}	V_{IL}	X	X	(Note 4)	(Note 4)	D_{IN}
Program verify		V_{IL}	V_{IL}	V_{IH}	X	X	(Note 4)	(Note 4)	D_{OUT}
Program inhibit		V_{IH}	X	X	X	X	(Note 4)	(Note 4)	HIGH Z
Intelligent Identifier	Manufacturer(3)	V_{IL}	V_{IL}	X	V_H (2)	V_{IL}	V_{CC}	5.0 V	0089 H
	Device(3)	V_{IL}	V_{IL}	X	V_H (2)	V_{IH}	V_{CC}	5.0 V	00FFH

NOTES:
1. X can be V_{IL} or V_{IH}
2. V_H = 12.0 V ±0.5 V
3. A_1-A_8, A_{10}-A_{15} = V_{IL}
4. See table III for V_{CC} and Vpp voltages.

FIGURE 2. Truth table.

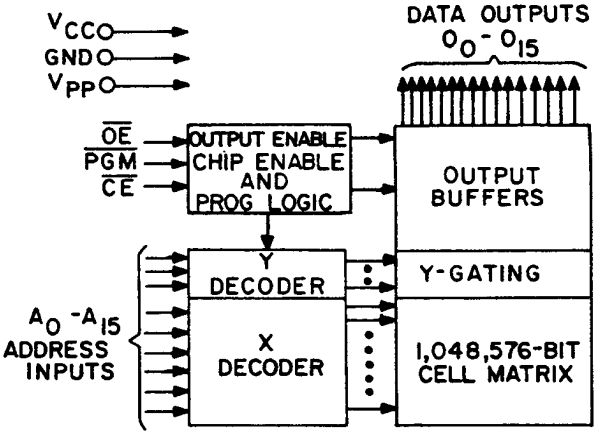


FIGURE 3. Block diagram.

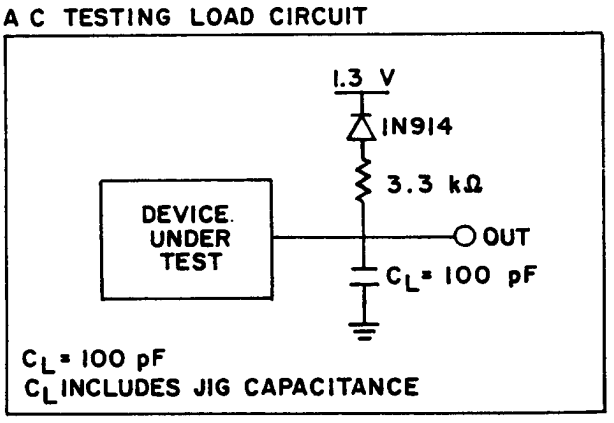
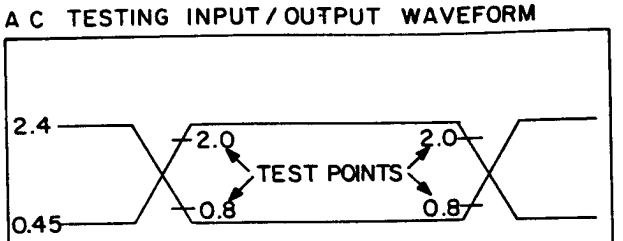


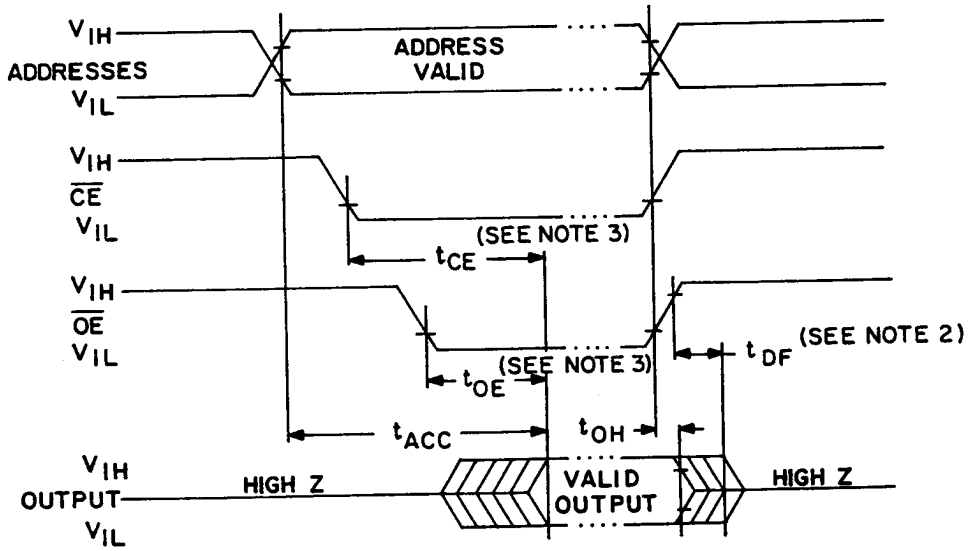
FIGURE 4. Load circuit.

A C TESTING INPUT / OUTPUT WAVEFORM



A C TESTING INPUTS ARE DRIVEN AT 2.4 V FOR A LOGIC "1" AND 0.45 V FOR A LOGIC "0". TIMING MEASUREMENTS ARE MADE AT 2.0 V FOR A LOGIC "1" AND 0.8 V FOR A LOGIC "0".

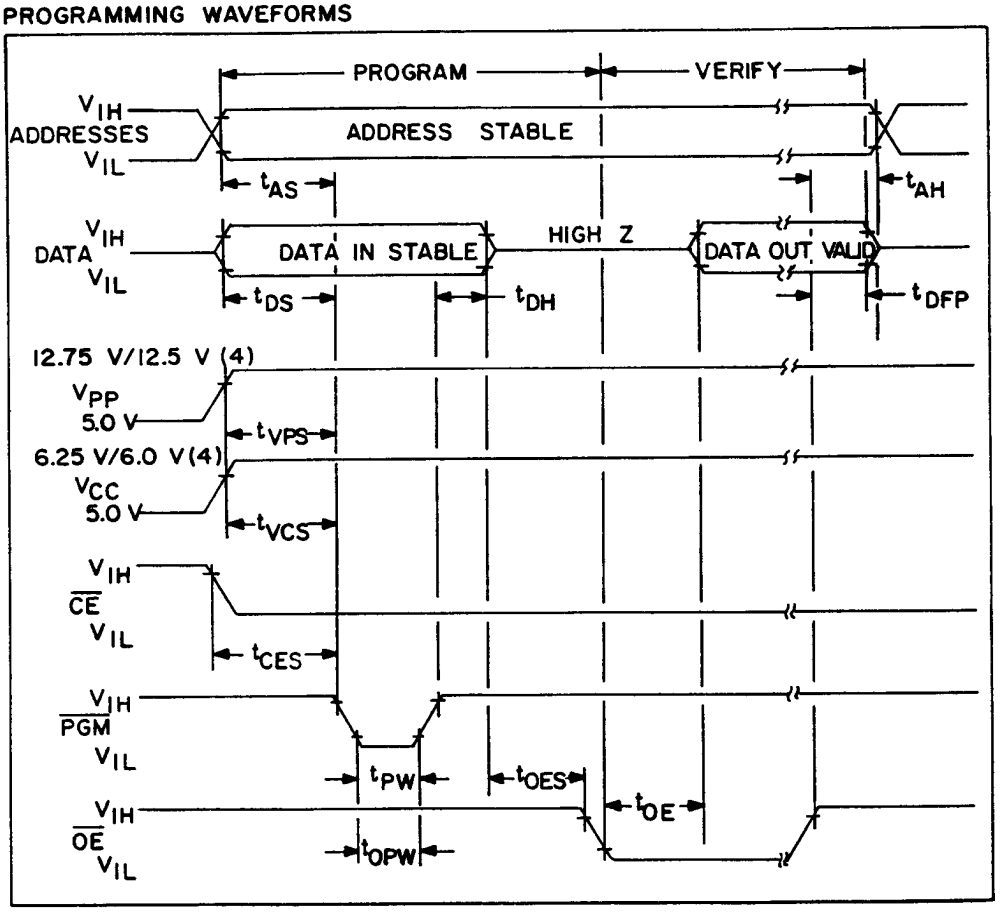
A C WAVEFORMS



NOTES:
1. Typical values are for T_C = +25°C and nominal supply voltages.
2. This parameter is only sampled and is not 100 percent tested.
3. $\overline{OE}$ may be delayed up to t_{CE}-t_{OE} after the falling edge of $\overline{CE}$ without impact on t_{CE}.

FIGURE 5. Waveforms.

PROGRAMMING WAVEFORMS



NOTES:
1. The input timing reference level is 0.8 for V_{IL} and 2 V for a V_{IH}.
2. t_{OE} and t_{DFP} are characteristics of the device but must be accommodated by the programmer.
3. When programming the device, a 0.1 µF capacitor is required across Vpp and ground to suppress spurious voltage transients which can damage the device.
4. 12.75 V Vpp and 6.25 V V_{CC} for quick-pulse programming algorithm; 12.5 V Vpp and 6.0 V V_{CC} for intelligent programming algorithm.

FIGURE 6. Programming waveforms.

4. QUALITY ASSURANCE PROVISIONS

4.1 Sampling and inspection. Sampling and inspection procedures shall be in accordance with section 4 of MIL-M-38510 to the extent specified in MIL-STD-883 (see 3.1 herein).

4.2 Screening. Screening shall be in accordance with method 5004 of MIL-STD-883, and shall be conducted on all devices prior to quality conformance inspection. The following additional criteria shall apply:

a. Burn-in test (method 1015 of MIL-STD-883).

(1) Test condition A, B, C, or D using the circuit submitted with the certificate of compliance (see 3.5 herein).

(2) T_A = +125°C, minimum.

b. Interim and final electrical test parameters shall be as specified in table II herein, except interim electrical parameter tests prior to burn-in are optional at the discretion of the manufacturer.

c. A data retention stress test shall be included as part of the screening procedure and shall consist of the following steps:

Margin test.

(1) Program greater than 95 percent of the bit locations, including the slowest programming cell (see 3.5.2). The remaining cells shall provide a worst case speed pattern.

(2) Bake, unbiased, for 72 hours at +140°C to screen for data retention lifetime.

(3) Perform a margin test using V_m = + 5.9 at +25°C using loose timing (i.e., t_{ACC} = 1 µs).

(4) Perform dynamic burn-in (see 4.2a).

(5) Margin at V_m = +5.9 V.

(6) Perform electrical test (see 4.2).

(7) Erase (see 3.5.1), except devices submitted for groups A, B, C, and D testing.

(8) Verify erasure (see 3.5.3).

4.3 Quality conformance inspection. Quality conformance inspection shall be in accordance with method 5005 of MIL-STD-883 including groups A, B, C, and D inspections. The following additional criteria shall apply.

4.3.1 Group A inspection.

a. Tests shall be as specified in table II herein.

b. Subgroups 5 and 6 in table I, method 5005 of MIL-STD-883 shall be omitted.

c. Subgroup 4 (i.e., C_{IN} measurement) shall be measured only for the initial test and after process or design changes which may affect input capacitance.

d. All devices selected for testing shall have the EPROM programmed with a checkerboard pattern or equivalent. After completion of all testing, the devices shall be erased and verified (except devices submitted for groups C and D testing).

e. Subgroups 7 and 8 tests shall consist of verifying the EPROM pattern specified.

TABLE II. Electrical test requirements.

MIL-STD-883 test requirements	Subgroups (per method 5005, table I)
Interim electrical parameters (method 5004)	---
Final electrical test parameters (method 5004)	1*, 2, 3, 7*, 8, 9, 10, 11
Group A test requirements (method 5005)	1, 2, 3, 7, 8, 9, 10, 11
Groups C and D end-point electrical parameters (method 5005)	2, 8(HOT), 10
Additional electrical subgroups for group C periodic inspections	---

*PDA applies to subgroups 1 and 7.

4.3.2 Groups C and D inspections.

a. End-point electrical parameters shall be as specified in table II herein.

b. Steady-state life test (method 1005 of MIL-STD-883) conditions:

(1) Test condition A, B, C, or D using the circuit submitted with the certificate of compliance (see 3.5 herein).

(2) T_A = +125°C, minimum.

(3) Test duration: 1,000 hours, except as permitted by appendix B of MIL-M-38510 and method 1005 of MIL-STD-883.

4.4 Erasing procedures. The recommended erasure procedure is exposure to shortwave ultraviolet light which has a wavelength of 2537 Angstroms (Å). The integrated dose (i.e., ultraviolet intensity times exposure time) for erasure should be a minimum of fifteen ws/cm^2. The erasure time with this dosage is approximately 15 to 20 minutes using an ultraviolet lamp with a 12000 $\mu W/cm^2$ power rating. The device should be placed within one inch of the lamp tubes during erasure. The maximum integrated dose the device can be exposed to without damage is 7258 ws/cm^2 (1 week at 12000 $\mu W/cm^2$). Exposure of the device to high intensity ultraviolet light for long periods may cause permanent damage.

4.5 Programming procedures. The programming characteristics in table III and the following procedures shall be used for programming the device.

a. Connect the device in the electrical configuration for programming the waveforms of figure 6 and programming characteristics of table III shall apply.

b. Initially and after each erasure all bits are in the "1" state. Information is introduced by selectively programming "0" into the desired bit locations. A programmed "0" can be changed to a "1" by ultraviolet light erasure (see 4.4).

c. Programming occurs when V_{PP} is raised to its programming voltage (see table II) and $\overline{CE}$ and $\overline{PRGM}$ are both at TTL low.

5. PACKAGING

5.1 Packaging requirements. The requirements for packaging shall be in accordance with MIL-M-38510.

6. NOTES

6.1 Intended use. Microcircuits conforming to this drawing are intended for use when military specifications do not exist and qualified military devices that will perform the required function are not available for OEM application. When a military specification exists and the product covered by this drawing has been qualified for listing on QPL-38510, the device specified herein will be inactivated and will not be used for new design. The QPL-38510 product shall be the preferred item for all applications.

6.2 Replaceability. Microcircuits covered by this drawing will replace the same generic device covered by a contractor-prepared specification or drawing.

6.3 Comments. Comments on this drawing should be directed to DESC-ECS, Dayton, Ohio 45444, or telephone 513-296-5375.

TABLE III. Programming characteristics.

Parameter	Symbol	Conditions 1/ 2/ T_C = +25°C ±5°C	Group A subgroups	Device types	Limits Min	Limits Max	Unit
Input leakage current (all inputs)	I_{LI}	V_{IN} = 6 V		All		10	µA
Input low level (all inputs)	V_{IL}			All	-0.1	0.8	V
Input high level	V_{IH}			All	2.0	V_{CC} +1	V
Output low voltage during verify	V_{OL}	I_{OL} = 2.1 mA		All		0.45	V
Output high voltage during verify	V_{OH}	I_{OH} = -400 µA		All	2.4		V
V_{CC} supply current (program and verify)	I_{CC2} 3/	CE = $\overline{PRGM}$ = V_{IL}		All		160	mA
V_{PP} supply current (program)	I_{PP2}	CE = $\overline{PRGM}$ = V_{IL}		All		50	mA
A9 intelligent identifier voltage	V_{ID}	V_{CC} = 5 V		All	11.5	12.5	V
Intelligent programming algorithm	V_{PP}			All	12.0	13.0	V
Quick-pulse programming algorithm	V_{PP}			All	12.5	13.0	V
Intelligent programming algorithm	V_{CC}			All	5.75	6.25	V
Quick-pulse programming algorithm	V_{CC}			All	6.0	6.5	V
Address setup time	t_{AS}			All	2		µs

See footnotes at end of table.

TABLE III. Programming characteristics - Continued.

Parameter	Symbol	Conditions 1/ 2/ T_C = +25°C ±5°C	Group A subgroups	Device types	Limits Min	Limits Max	Unit
OE setup time	t_{OES}			All	2		µs
Data setup time	t_{DS}			All	2		µs
Address hold time	t_{AH}			All	0		µs
Data hold time	t_{DH}			All	2		µs
OE high to output float delay	t_{DFP} 4/			All	0	130	ns
Vpp setup time	t_{VPS}			All	2		µs
V_{CC} setup time	t_{VCS}			All	2		µs
CE setup time	t_{CES}			All	2		µs
PRGM initial program pulse width	t_{PW}	Intelligent programming Quick-pulse programming		All All	0.95 95	1.05 105	ms µs
PRGM overprogram pulse width	t_{OPW}	5/		All	2.85	78.75	ms
Data valid from OE	t_{OE}			All		150	ns

1/ V_{CC} must be applied simultaneously or before Vpp and removed simultaneously or after Vpp.

2/ See figure 6.

3/ The maximum current value is with outputs O_0 -O_{15} unloaded.

4/ This parameter is only sampled and is not 100 percent tested. Output float is defined as the point where data is no longer driven (see timing diagram).

5/ The length of the overprogram pulse (intelligent programming algorithm only) may vary from 2.85 ms to 78.75 ms as a function of the iteration counter value X.

6.4 Approved source of supply. An approved source of supply is listed herein. Additional sources will be added as they become available. The vendor listed herein has agreed to this drawing and a certificate of compliance (see 3.6 herein) has been submitted to DESC-ECS.

Military drawing part number	Vendor CAGE number	Vendor similar part number 1/	Replacement military specification part number
5962-8774401QX	34649	MD27210-20/B	
5962-8774402QX	34649	MD27210-25/B	

1/ Caution. Do not use this number for item acquisition. Items acquired to this number may not satisfy the performance requirements of this drawing.

Vendor CAGE number	Vendor name and address
34649	Intel Corporation 3065 Bowers Avenue Santa Clara, CA 95051

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