REVISIONS			
LTR	DESCRIPTION	DATE (YR-MO-DA)	APPROVED
A	Made corrections to table I and figure 1. Changed drawing to reflect MIL-H-38534 processing. Editorial changes throughout.	91-04-22	W. Heckman
B	Correct I_{EE} and I_{CC} limits. Change to reflect MIL-PRF-38534 processing. Editorial changes throughout.	98-01-15	K. A. Cottongim

REV																				
SHEET																				
REV																				
SHEET																				
REV STATUS OF SHEETS				REV	B	B	B	B	B	B	B	B	B	B	B	B	B			
				SHEET	1	2	3	4	5	6	7	8	9	10	11	12				

PMIC N/A

STANDARD MICROCIRCUIT DRAWING

THIS DRAWING IS AVAILABLE FOR USE BY ALL DEPARTMENTS AND AGENCIES OF THE DEPARTMENT OF DEFENSE

AMSC N/A

PREPARED BY
Donald R. Osborne

CHECKED BY
Ray Monnin

APPROVED BY
Michael Frye

DRAWING APPROVAL DATE
88-07-06

REVISION LEVEL
B

DEFENSE SUPPLY CENTER COLUMBUS
P. O. BOX 3990
COLUMBUS, OHIO 43216-5000

MICROCIRCUIT, HYBRID, LINEAR, QUAD, 12-BIT, DIGITAL-TO-ANALOG CONVERTER

SIZE	CAGE CODE	5962-88510
A	67268	

SHEET 1 OF 12

DSCC FORM 2233
APR 97

5962-E141-98

1. SCOPE

1.1 Scope. This drawing describes device requirements for class H hybrid microcircuits to be processed in accordance with MIL-PRF-38534 and a choice of case outlines and lead finishes are available and are reflected in the Part or Identifying Number (PIN).

1.2 PIN. The PIN shall be as shown in the following example:

5962-88510	01	X	A
Drawing number	Device type (see 1.2.1)	Case outline (see 1.2.2)	Lead finish (see 1.2.3)

1.2.1 Device type(s). The device type(s) shall identify the circuit function as follows:

Device type	Generic number	Circuit function
01	AD394S	Quad 12 bit DAC (bipolar)
02	AD394T	Quad 12 bit DAC (bipolar)
03	AD395S 1/	Quad 12 bit DAC (unipolar)
04	AD395T 1/	Quad 12 bit DAC (unipolar)

1.2.2 Case outline(s). The case outline(s) shall be as designated in MIL-STD-1835 and as follows:

Outline letter	Descriptive designator	Terminals	Package style
X	See figure 1	28	Dual-in-line

1.2.3 Lead finish. The lead finish shall be as specified in MIL-PRF-38534.

1.3 Absolute maximum ratings. 2/

$+V_S$ to DGND	-0.3 V dc to +17 V dc
$-V_S$ to DGND	+0.3 V dc to -17 V dc
Digital inputs (pins 1 through 16) to DGND	-0.3 V dc to +7 V dc
V_{REFIN} to AGND	±25 V dc
AGND to DGND	±0.6 V dc
Outputs (pins 18, 21, 24, and 27):	
Shorted to AGND or DGND	Indefinite
Shorted to $\pm V_S$	Momentary
Storage temperature range	-65°C to +150°C
Lead temperature (soldering, 10 seconds)	+300°C
Junction temperature (T_J)	+175°C
Thermal resistance, junction-to-case (θ_{JC})	8°C/W
Thermal resistance, junction-to-ambient (θ_{JA})	25°C/W

1.4 Recommended operating conditions.

$\pm V_S$ to DGND	±15 V dc ±10%
V_{REFIN} to AGND	+10 V dc
Ambient operating temperature range (T_A)	-55°C to +125°C

1/ These generic numbers are inactive for new design.
2/ Stresses above the absolute maximum rating may cause permanent damage to the device. Extended operation at the maximum levels may degrade performance and affect reliability.

2. APPLICABLE DOCUMENTS

2.1 Government specification, standards, and handbook. The following specification, standards, and handbook form a part of this drawing to the extent specified herein. Unless otherwise specified, the issues of these documents are those listed in the issue of the Department of Defense Index of Specifications and Standards (DoDISS) and supplement thereto, cited in the solitation.

SPECIFICATION

DEPARTMENT OF DEFENSE

MIL-PRF-38534 - Hybrid Microcircuits, General Specification for.

STANDARDS

DEPARTMENT OF DEFENSE

MIL-STD-883 - Test Methods and Procedures for Microelectronics.
MIL-STD-973 - Configuration Management.
MIL-STD-1835 - Microcircuit Case Outlines.

HANDBOOK

DEPARTMENT OF DEFENSE

MIL-HDBK-780 - Standard Microcircuit Drawings.

(Unless otherwise indicated, copies of the specification, standards, and handbook are available from the Standardization Document Order Desk, 700 Robbins Avenue, Building 4D, Philadelphia, PA 19111-5094.)

2.2 Order of precedence. In the event of a conflict between the text of this drawing and the references cited herein, the text of this drawing takes precedence. Nothing in this document, however, supersedes applicable laws and regulations unless a specific exemption has been obtained.

3. REQUIREMENTS

3.1 Item requirements. The individual item performance requirements for device class H shall be in accordance with MIL-PRF-38534. Compliance with MIL-PRF-38534 may include the performance of all tests herein or as designated in the device manufacturer's Quality Management (QM) plan or as designated for the applicable device class. Therefore, the tests and inspections herein may not be performed for the applicable device class (see MIL-PRF-38534). Futhermore, the manufacturers may take exceptions or use alternate methods to the tests and inspections herein and not perform them. However, the performance requirements as defined in MIL-PRF-38534 shall be met for the applicable device class.

3.2 Design, construction, and physical dimensions. The design, construction, and physical dimensions shall be as specified in MIL-PRF-38534 and herein.

3.2.1 Case outline(s). The case outline(s) shall be in accordance with 1.2.2 herein and figure 1.

3.2.2 Terminal connections. The terminal connections shall be as specified on figure 2.

3.2.3 Timing diagram(s). The timing diagram(s) shall be as specified on figure 3.

3.2.4 Truth table(s). The truth table(s) shall be as specified on figure 4.

3.3 Electrical performance characteristics. Unless otherwise specified herein, the electrical performance characteristics are as specified in table I and shall apply over the full specified operating temperature range.

3.4 Electrical test requirements. The electrical test requirements shall be the subgroups specified in table II. The electrical tests for each subgroup are defined in table I.

3.5 Marking of Device(s). Marking of device(s) shall be in accordance with MIL-PRF-38534. The device shall be marked with the PIN listed in 1.2 herein. In addition, the manufacturer's vendor similar PIN may also be marked as listed in QML-38534.

3.6 Data. In addition to the general performance requirements of MIL-PRF-38534, the manufacturer of the device described herein shall maintain the electrical test data (variables format) from the initial quality conformance inspection group A lot sample, for each device type listed herein. Also, the data should include a summary of all parameters manually tested, and for those which, if any, are guaranteed. This data shall be maintained under document revision level control by the manufacturer and be made available to the preparing activity (DSCC-VA) upon request.

3.7 Certificate of compliance. A certificate of compliance shall be required from a manufacturer in order to supply to this drawing. The certificate of compliance (original copy) submitted to DSCC-VA shall affirm that the manufacturer's product meets the performance requirements of MIL-PRF-38534 and herein.

3.8 Certificate of conformance. A certificate of conformance as required in MIL-PRF-38534 shall be provided with each lot of microcircuits delivered to this drawing.

4. QUALITY ASSURANCE PROVISIONS

4.1 Sampling and inspection. Sampling and inspection procedures shall be in accordance with MIL-PRF-38534 or as modified in the device manufacturer's Quality Management (QM) plan. The modification in the QM plan shall not affect the form, fit, or function as described herein.

4.2 Screening. Screening shall be in accordance with MIL-PRF-38534. The following additional criteria shall apply:

a. Burn-in test, method 1015 of MIL-STD-883.

(1) Test condition A, B, C, or D. The test circuit shall be maintained by the manufacturer under document revision level control and shall be made available to either DSCC-VA or the acquiring activity upon request. Also, the test circuit shall specify the inputs, outputs, biases, and power dissipation, as applicable, in accordance with the intent specified in test method 1015 of MIL-STD-883.

(2) T_A as specified in accordance with table I of method 1015 of MIL-STD-883.

b. Interim and final electrical test parameters shall be as specified in table II herein, except interim electrical parameter tests prior to burn-in are optional at the discretion of the manufacturer.

TABLE I. Electrical performance characteristics.

Test	Symbol	Conditions 1/ $-55°C \le T_A \le +125°C$ unless otherwise specified	Device types	Group A subgroups	Limits		Unit
					Min	Max	
Input voltage high	V_{IH}	Pins 1 through 16	All	1	2.4		V
				2, 3 2/	2.4		
Input voltage low	V_{IL}	Pins 1 through 16	All	1		0.8	V
				2, 3 2/		0.8	
Input current high	I_{IH}	V_{IN} = +5 V	All	1		40	µA
				2, 3 2/		40	
Input current low	I_{IL}	V_{IN} = 0 V	All	1		40	µA
				2, 3 2/		40	
Output voltage range	V_{OUT}	External +10.000 V ref BC = 111111111111 to 000000000000	01, 02	1, 2, 3 3/	-10	+10	V
			03, 04	1, 2, 3 3/	-10	0	V
Gain error	Ae	External +10.000 V ref BC = 111111111111	01, 03	4		0.1	±% fs 4/
			02, 04	4		0.05	
		End-point electrical	All	4		0.2	
Gain error temperature coefficient	$TC/_{Ae}$	External +10.000 V ref BC = 111111111111	01, 03	5, 6		10	±ppm/ °C
			02, 04	5, 6		5	
Offset error	V_{OS}	External +10.000 V ref BC = 000000000000	01, 03	1		0.05	±% fs 4/
			02, 04	1		0.025	
		End-point electrical	All	1		0.1	
Offset temperature coefficient	$TC/_{BPZ}$	External +10.000 V ref BC = 000000000000	01, 03	2, 3		10	±ppm/ °C
			02, 04	2, 3		5	

See footnotes at end of table.

TABLE I. Electrical performance characteristics - Continued.

Test	Symbol	Conditions 1/ $-55°C \le T_A \le +125°C$ unless otherwise specified	Device types	Group A subgroups	Limits Min	Limits Max	Unit
Differential linearity error	DLE	5/ 6/	01, 03	1		0.75	±LSB
			02, 04	1		0.5	
			All	2, 3		1	
		End-point electrical	All	1		1.5	
Integral linearity error 7/	ILE	8/	01, 03	1, 2, 3		0.75	±LSB
			02, 04	1, 2, 3		0.5	
		End-point electrical	All	1		1	
Digital feed-through 9/	DFTe	See figure 3 $T_A = +25°C$	All	4	-0.5	+0.5	±LSB
Power supply voltages	$+V_S$		All	1, 2, 3		+15	V
	$-V_S$				-15		
Negative supply current	I_{EE}	Data input bits = 11111111111 No load $T_A = +25°C$	All	1		22	mA
Positive supply current	I_{CC}	Data input bits = 111111111111 No load $T_A = +25°C$	All	1		28	mA
Power supply gain sensitivity gain/ V_S ($+V_S$ and $-V_S$)	+PSRR	Data input bits = 111111111111 $+V_S$ = +15 V ±10% $T_A = +25°C$	All	1		0.006	±% fs per %
	-PSRR	Data input bits = 111111111111 $-V_S$ = -15 V ±10% $T_A = +25°C$	All	1		0.006	±% fs per %
Functional tests		See 4.3.1b	All	7			
				8 2/			

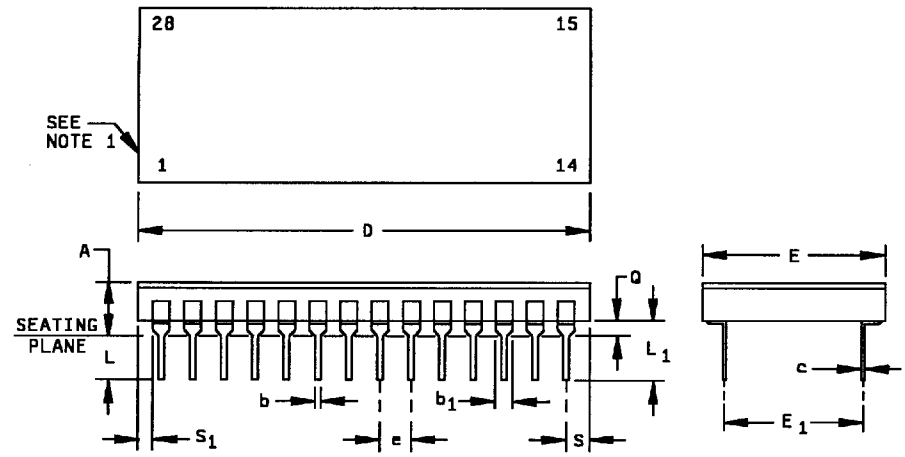
See footnotes at end of table.

TABLE I. Electrical performance characteristics - Continued.

Test	Symbol	Conditions 1/ $-55°C \le T_A \le +125°C$ unless otherwise specified	Device types	Group A subgroups	Limits		Unit
					Min	Max	
Chip select pulse width 2/	t_{CS}	See figure 3	All	9, 10, 11		170	ns
Data setup time 2/	t_{DS}	See figure 3	All	9, 10, 11	150		ns
Data hold time 2/	t_{DH}	See figure 3	All	9, 10, 11	5		
Settling time 2/	t_{SETT}	See figure 3	All	9, 10, 11		15	µs

1/ $\pm V_S = \pm 15$ V dc.
2/ Parameter shall be tested as part of device initial characterization and after design and process changes and therefore shall be guaranteed to the limits specified in table I.
3/ This parameter is verified as a test condition while testing other parameters.
4/ Full scale range = 20 V for a ±10 V bipolar range. Full scale range = 10 V for a 0 V to 10 V unipolar range.
5/ Monoticity is tested over the full military temperature range.
6/ Differential linearity is measured at the following codes to code-1: Codes = 1, 2, 4, 8, 16, 32, 64, 128, 256, 512, 1024, and 2048.
7/ Integral nonlinearity is a measure of the maximum deviation from a straight line passing through the end points of the transfer function.
8/ Integral linearity is measured at the following codes: Codes = 1, 2, 4, 8, 16, 32, 64, 128, 256, 512, 768, 1024, 1280, 1536, 1792, 2048, 2304, 2560, 2816, 3072, 3328, 3584, and 3840.
9/ Digital feed-through is defined as the change in DAC's outputs steady-state value as a result of the same DAC's inputs digitally being driven from all 1's to all 0's with CS = 1.

Case outline X.



Symbol	Inches		Millimeters		Notes
	Min	Max	Min	Max	
A		0.225		5.75	
b	0.014	0.023	0.36	0.58	
b_1	0.030	0.070	0.76	1.78	2
c	0.008	0.015	0.20	0.38	
D		1.575		40.00	
E	0.770	0.810	19.56	20.57	

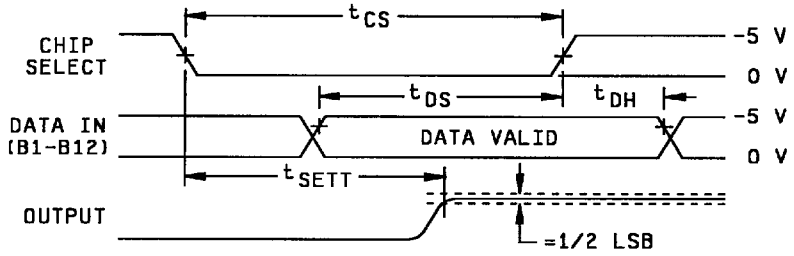
Symbol	Inches		Millimeters		Notes
	Min	Max	Min	Max	
E_1	0.590	0.610	14.99	15.50	6
e	0.100 BSC		2.54 BSC		4, 7
L	0.125	0.200	3.18	5.08	
L_1	0.180		4.57		
Q	0.015	0.060	0.38	1.52	3
S		0.137		3.48	5
S_1	0.100		0.13		5

NOTES:
1. Index area: A notch or a lead one identification mark is located adjacent to lead one.
2. The minimum limit for dimension b_1 may be 0.023" (0.58 mm) for all four corner leads only.
3. Dimension Q shall be measured from the seating plane to the base plane.
4. The base pin spacing is 0.100" (2.54 mm) between centerlines.
5. Applies to all four corners.
6. E_1 shall be measured at the centerline of all the leads at the standoffs.
7. Twenty-six spaces.

FIGURE 1. Case outline.

Device types	All	Device types	All
Case outline	X	Case outline	X
Terminal number	Terminal symbol	Terminal number	Terminal symbol
1	MSB	15	$\overline{CS3}$
2	B2	16	$\overline{CS4}$
3	B3	17	DGND
4	B4	18	$V_{OUT}4$
5	B5	19	$V_{IN}4$
6	B6	20	-15 V
7	B7	21	$V_{OUT}3$
8	B8	22	$V_{IN}3$
9	B9	23	AGND
10	B10	24	$V_{OUT}2$
11	B11	25	$V_{IN}2$
12	LSB	26	+15 V
13	$\overline{CS1}$	27	$V_{OUT}1$
14	$\overline{CS2}$	28	$V_{IN}1$

FIGURE 2. Terminal connections.



NOTES:
1. $t_r = t_f = 20$ ns. All input signal rise and fall times measured from 10 percent to 90 percent of V_{DD} (±5 V typical).
2. Timing measurement reference level is $(V_{IH} - V_{IL})/2$.

MODE SELECTION

Write mode
CS low DAC respond to
Data bus (B1-B12) inputs

Hold mode
CS high data bus (B1-B12)
locked out DAC holds last data present
when CS assumed high state

FIGURE 3. Timing diagram.

$\overline{CS1}$	$\overline{CS2}$	$\overline{CS3}$	$\overline{CS4}$	Operation
1	1	1	1	All DACs latched
0	1	1	1	Load DAC 1 from data bus
1	0	1	1	Load DAC 2 from data bus
1	1	0	1	Load DAC 3 from data bus
1	1	1	0	Load DAC 4 from data bus
0	0	0	0	All DACs simultaneously loaded

FIGURE 4. Truth table.

TABLE II. Electrical test requirements.

MIL-PRF-38534 test requirements	Subgroups (in accordance with MIL-PRF-38534, group A test table)
Interim electrical parameters	1
Final electrical parameters	1*, 2, 3, 4, 5, 6, 7, 9
Group A test requirements	1, 2, 3, 4, 5, 6, 7, 8**, 9**, 10**, 11**
Group C end-point electrical parameters	1, 4

* PDA applies to subgroup 1.
** Subgroups 8, 9, 10, and 11 shall be tested as part of device characterization and after design and process changes and therefore shall be guaranteed to the limits specified in table I.

4.3 Conformance and periodic inspections. Conformance inspection (CI) and periodic inspection (PI) shall be in accordance with MIL-PRF-38534 and as specified herein.

4.3.1 Group A inspection (CI). Group A inspection shall be in accordance with MIL-PRF-38534 and as follows:

a. Tests shall be as specified in table II herein.

b. Subgroups 7 and 8 shall include verification of the truth table (see figure 4).

4.3.2 Group B inspection (PI). Group B inspection shall be in accordance with MIL-PRF-38534.

4.3.3 Group C inspection (PI). Group C inspection shall be in accordance with MIL-PRF-38534 and as follows:

a. End-point electrical parameters shall be as specified in table II herein.

b. Steady-state life test, method 1005 of MIL-STD-883.

(1) Test condition A, B, C, or D. The test circuit shall be maintained by the manufacturer under document revision level control and shall be made available to either DSCC-VA or the acquiring activity upon request. Also, the test circuit shall specify the inputs, outputs, biases, and power dissipation, as applicable, in accordance with the intent specified in test method 1005 of MIL-STD-883.

(2) T_A as specified in accordance with table I of method 1005 of MIL-STD-883.

(3) Test duration: 1,000 hours, except as permitted by method 1005 of MIL-STD-883.

4.3.4 Group D inspection (PI). Group D inspection shall be in accordance with MIL-PRF-38534.

5. PACKAGING

5.1 Packaging requirements. The requirements for packaging shall be in accordance with MIL-PRF-38534.

6. NOTES

6.1 Intended use. Microcircuits conforming to this drawing are intended for use for Government microcircuit applications (original equipment), design applications, and logistics purposes.

6.2 Replaceability. Microcircuits covered by this drawing will replace the same generic device covered by a contractor-prepared specification or drawing.

6.3 Configuration control of SMD's. All proposed changes to existing SMD's will be coordinated with the users of record for the individual documents. This coordination will be accomplished in accordance with MIL-STD-973 using DD Form 1692, Engineering Change Proposal.

6.4 Record of users. Military and industrial users shall inform Defense Supply Center Columbus when a system application requires configuration control and the applicable SMD. DSCC will maintain a record of users and this list will be used for coordination and distribution of changes to the drawings. Users of drawings covering microelectronic devices (FSC 5962) should contact DSCC-VA, telephone (614) 692-7603.

6.5 Comments. Comments on this drawing should be directed to DSCC-VA, P. O. Box 3990, Columbus, Ohio 43216-5000, or telephone (614) 692-0676.

6.6 Sources of supply. Sources of supply are listed in QML-38534. The vendors listed in QML-38534 have submitted a certificate of compliance (see 3.7 herein) to DSCC-VA and have agreed to this drawing.

STANDARD MICROCIRCUIT DRAWING SOURCE APPROVAL BULLETIN

DATE: 98-01-15

Approved sources of supply for SMD 5962-88510 are listed below for immediate acquisition only and shall be added to QML-38534 during the next revision. QML-38534 will be revised to include the addition or deletion of sources. The vendors listed below have agreed to this drawing and a certificate of compliance has been submitted to and accepted by DSCC-VA. This bulletin is superseded by the next dated revision of QML-38534.

Standard microcircuit drawing PIN 1/	Vendor CAGE number	Vendor similar PIN 2/
5962-8851001XA 5962-8851001XC	34031 34031	AD394SD/883B AD394SD/883B
5962-8851002XC	34031	AD394TD/883B
5962-8851003XX	3/	AD395SD/883B
5962-8851004XX	3/	AD395TD/883B

1/ The lead finish shown for each PIN, representing a hermetic package, is the most readily available from the manufacturer listed for that part. If the desired lead finish is not listed contact the Vendor to determine availability.

2/ Caution. Do not use this number for item acquisition. Items acquired to this number may not satisfy the performance requirements of this drawing.

3/ Not available from a QML source.

Vendor CAGE number	Vendor name and address
34031	Analod Devices, Incorporated 7910 Triad Center Drive Greensboro, NC 27409-9605

The information contained herein is disseminated for convenience only and the Government assumes no liability whatsoever for any inaccuracies in this information bulletin.