REVISIONS			
LTR	DESCRIPTION	DATE (YR-MO-DA)	APPROVED
A	Add "Changes in accordance with NOR 5962-R115-92."	92-01-27	M. A. Frye
B	Add software data protection. Increase data retention to 20 years, minimum. Add device types 08 through 16. Remove tests t_{DHWL}, t_{WHDX}, and ESDS requirements from drawing.	93-07-21	M. A. Frye

THE ORIGINAL FIRST PAGE OF THIS DRAWING HAS BEEN REPLACED.

REV																			
SHEET																			
REV	B	B	B	B	B	B	B	B	B										
SHEET	15	16	17	18	19	20	21	22	23										

REV STATUS OF SHEETS	REV	B	B	B	B	B	B	B	B	B	B	B	B	B	B
	SHEET	1	2	3	4	5	6	7	8	9	10	11	12	13	14

PMIC N/A

STANDARDIZED MILITARY DRAWING

THIS DRAWING IS AVAILABLE FOR USE BY ALL DEPARTMENTS AND AGENCIES OF THE DEPARTMENT OF DEFENSE

AMSC N/A

PREPARED BY
Kenneth Rice

CHECKED BY
Ray Monnin

APPROVED BY
Michael A. Frye

DRAWING APPROVAL DATE
88-08-29

REVISION LEVEL
B

DEFENSE ELECTRONICS SUPPLY CENTER
DAYTON, OHIO 45444

MICROCIRCUIT, MEMORY, DIGITAL, CMOS 32K X 8 EEPROM, MONOLITHIC SILICON

SIZE	CAGE CODE	5962-88525
A	67268	

SHEET 1 OF 23

DESC FORM 193
JUL 91

5962-E176-93

1. SCOPE

1.1 Scope. This drawing describes device requirements for class B microcircuits in accordance with 1.2.1 of MIL-STD-883, "Provisions for the use of MIL-STD-883 in conjunction with compliant non-JAN devices".

1.2 Part or Identifying Number (PIN). The complete PIN shall be as shown in the following example:

1.2.1 Device type(s). The device type(s) shall identify the circuit function as follows:

Device type	Generic number	Circuit function	Access time	Write speed	Write mode	End of Write Indicator	Endurance	Software data protect
01	See 6.6	(32K X 8 EEPROM)	350 ns	10 ms	byte/page	$\overline{\text{DATA}}$ polling	10,000 cycles	No
02			300 ns	10 ms	byte/page	$\overline{\text{DATA}}$ polling	10,000 cycles	No
03			250 ns	10 ms	byte/page	$\overline{\text{DATA}}$ polling	10,000 cycles	No
04			200 ns	10 ms	byte/page	$\overline{\text{DATA}}$ polling	10,000 cycles	No
05			250 ns	10 ms	byte/page	$\overline{\text{DATA}}$ polling	100,000 cycles	No
06			150 ns	10 ms	byte/page	$\overline{\text{DATA}}$ polling	10,000 cycles	No
07			150 ns	3 ms	byte/page	$\overline{\text{DATA}}$ polling	10,000 cycles	No
08			150 ns	10 ms	byte/page	$\overline{\text{DATA}}$ polling	100,000 cycles	No
09			350 ns	10 ms	byte/page	$\overline{\text{DATA}}$ polling	10,000 cycles	Yes
10			300 ns	10 ms	byte/page	$\overline{\text{DATA}}$ polling	10,000 cycles	Yes
11			250 ns	10 ms	byte/page	$\overline{\text{DATA}}$ polling	10,000 cycles	Yes
12			200 ns	10 ms	byte/page	$\overline{\text{DATA}}$ polling	10,000 cycles	Yes
13			250 ns	10 ms	byte/page	$\overline{\text{DATA}}$ polling	100,000 cycles	Yes
14			150 ns	10 ms	byte/page	$\overline{\text{DATA}}$ polling	10,000 cycles	Yes
15			150 ns	3 ms	byte/page	$\overline{\text{DATA}}$ polling	10,000 cycles	Yes
16			150 ns	10 ms	byte/page	DATA polling	100,000 cycles	Yes

1.2.2 Case outline(s). The case outline(s) shall be as designated in MIL-STD-1835 and as follows:

Outline letter	Descriptive designator	Terminals	Package style
U	See figure 1	28	Grid array
X	GDIPI-T28 or CDIP2-T28	28	Dual-in-line
Y	CQCC1-N32	32	Rectangular leadless chip carrier
Z	CDFP4-F28	28	Flat package

1.2.3 Lead finish. The lead finish shall be as specified in MIL-M-38510. Finish letter "X" shall not be marked on the microcircuit or its packaging. The "X" designation is for use in specifications when lead finishes A, B, and C are considered acceptable and interchangeable without preference.

1.3 Absolute maximum ratings. 1/

Supply voltage range (V_{CC})	-0.3 V dc to +6.25 V dc
Storage temperature range	-65°C to +150°C
Maximum power dissipation (P_D)	1.0 W
Lead temperature (soldering, 10 seconds)	+300°C
Junction temperature (T_J) 2/	+175°C
Thermal resistance, junction-to-case (Θ_{JC})	See MIL-STD-1835
Input voltage range (V_{IL}, V_{IH})	-0.3 V dc to +6.25 V dc
Data retention	20 years (minimum)
Endurance:	
Types 01-04, 06, 07, 09-12, 14, 15	10,000 cycles/byte (minimum)
Types 05, 08, 13 ,16	100,000 cycles/byte (minimum)
Chip clear voltage (V_H)	15.0 V dc

1.4 Recommended operating conditions. 1/

Supply voltage range (V_{CC})	+4.5 V dc to +5.5 V dc
Case operating temperature range (T_C)	-55°C to +125°C
Input voltage, low range (V_{IL})	-0.1 V dc to +0.8 V dc
Input voltage, high range (V_{IH})	+2.0 V dc to V_{CC} +0.3 V dc

2. APPLICABLE DOCUMENTS

2.1 Government specification, standards, and bulletin. Unless otherwise specified, the following specification, standards, and bulletin of the issue listed in that issue of the Department of Defense Index of Specifications and Standards specified in the solicitation, form a part of this drawing to the extent specified herein.

SPECIFICATION

MILITARY

MIL-M-38510 - Microcircuits, General Specification for.

STANDARDS

MILITARY

MIL-STD-883 - Test Methods and Procedures for Microelectronics.
MIL-STD-1835 - Microcircuit Case Outlines.

BULLETIN

MILITARY

MIL-BUL-103 - List of Standardized Military Drawings (SMD's).

(Copies of the specification, standards, and bulletin required by manufacturers in connection with specific acquisition functions should be obtained from the contracting activity or as directed by the contracting activity.)

2.2 Order of precedence. In the event of a conflict between the text of this drawing and the references cited herein, the text of this drawing shall take precedence.

3. REQUIREMENTS

3.1 Item requirements. The individual item requirements shall be in accordance with 1.2.1 of MIL-STD-883, "Provisions for the use of MIL-STD-883 in conjunction with compliant non-JAN devices" and as specified herein.

3.2 Design, construction, and physical dimensions. The design, construction, and physical dimensions shall be as specified in MIL-M-38510 and herein.

3.2.1 Case outline(s). The case outline(s) shall be in accordance with 1.2.2 herein and on figure 1.

3.2.2 Terminal connections. The terminal connections shall be as specified on figure 2.

3.2.2.1 Truth table (unprogrammed or erased devices). The truth table for unprogrammed devices shall be as specified on figure 3.

3.2.2.2 Programmed devices. The requirements for supplying programmed devices are not part of this drawing.

3.3 Electrical performance characteristics. Unless otherwise specified herein, the electrical performance characteristics are as specified in table I and shall apply over the full case operating temperature range.

1/ All voltages are referenced to V_{SS} (ground).
2/ Maximum junction temperature shall not be exceeded except for allowable short duration burn-in screening conditions in accordance with method 5004 of MIL-STD-883.

TABLE I. Electrical performance characteristics.

Test	Symbol	Conditions $-55°C \le T_C \le +125°C$, $V_{SS} = 0$ V, $4.5\ V \le V_{CC} \le 5.5$ V unless otherwise specified 1/	Group A subgroups	Device types	Limits		Unit
					Min	Max	
Supply current (active)	I_{CC1}	$\overline{CE} = \overline{OE} = V_{IL}$, $\overline{WE} = V_{IH}$ all I/O's = 0 mA, Inputs = V_{CC} = 5.5 V, f = $1/t_{AVAV}$ (minimum)	1,2,3	All		80	mA
Supply current (TTL standby)	I_{CC2}	$\overline{CE} = V_{IH}$, $\overline{OE} = V_{IL}$ all I/O's = 0 mA Inputs = V_{CC} -0.3 V	1,2,3	All		3	mA
Supply current (CMOS standby)	I_{CC3}	$\overline{CE} = V_{CC}$ -0.3 V all I/O's = 0 mA, Inputs = V_{IL} to V_{CC} -0.3 V	1,2,3	All		350	µA
Input leakage (high)	I_{IH}	V_{IN} = 5.5 V	1,2,3	All	-10	10	µA
Input leakage (low)	I_{IL}	V_{IN} = 0.1 V	1,2,3	All	-10	10	µA
Output leakage (high)	I_{OHZ} 2/	V_{OUT} = 5.5 V, $\overline{CE} = V_{IH}$	1,2,3	All	-10	10	µA
Output leakage (low)	I_{OLZ} 2/	V_{OUT} = 0.1 V, $\overline{CE} = V_{IH}$	1,2,3	All	-10	10	µA
Input voltage low	V_{IL}		1,2,3	All	-0.1	0.8	V
Input voltage high	V_{IH}		1,2,3	All	2.0	V_{CC} + 0.3V	V
Output voltage low	V_{OL}	I_{OL} = 2.1 mA, V_{IH} = 2.0 V, V_{CC} = 4.5 V, V_{IL} = 0.8 V	1,2,3	All		0.45	V
Output voltage high	V_{OH}	I_{OH} = -400 µA, V_{IH} = 2.0 V, V_{CC} = 4.5 V, V_{IL} = 0.8 V	1,2,3	All	2.4		V
$\overline{OE}$ high leakage (chip erase)	I_{OE}	V_H = 13 V	1,2,3	All	-10	100	µA

See footnotes at end of table.

TABLE I. Electrical performance characteristics - Continued.

Test	Symbol	Conditions $-55°C \le T_C \le +125°C$, $V_{SS} = 0$ V, $4.5\ V \le V_{CC} \le 5.5$ V unless otherwise specified 1/	Group A subgroups	Device types	Limits		Unit
					Min	Max	
Input capacitance	C_I 3/ 4/	$V_{IN} = 0$ V, $V_{CC} = 5.0$ V, $T_A = +25°C$, $f = 1$ MHz, See 4.3.1c	4	All		10	pF
Output capacitance	C_O 3/ 4/	$V_{OUT} = 0$ V, $V_{CC} = 5.0$ V, $T_A = +25°C$, $f = 1$ MHz, See 4.3.1c	4	All		10	pF
Read cycle time	t_{AVAV} 5/	See figure 4	9,10,11	01,09	350		ns
				02,10	300		
				03,05,11,13	250		
				04,12	200		
				06-08,14-16	150		
Address access time	t_{AVQV} 5/		9,10,11	01,09		350	ns
				02,10		300	
				03,05,11,13		250	
				04,12		200	
				06-08,14-16		150	
Chip enable access time	t_{ELQV} 5/		9,10,11	01,09		350	ns
				02,10		300	
				03,05,11,13		250	
				04,12		200	
				06-08,14-16		150	
Output enable access time	t_{OLQV} 5/		9,10,11	01-03,05 09-11,13		100	ns
				04,06,07,08 12,14,15,16		80	
Chip enable to output in low Z	t_{ELQX} 4/ 5/		9,10,11	All	10		ns
Chip disable to output in high Z	t_{EHQZ} 4/ 5/		9,10,11	01,02,09,10		80	ns
				03-08,11-16		60	
Output enable to output in low Z	t_{OLQX} 4/ 5/		9,10,11	All	10		ns
Output disable to output in high Z	t_{OHQZ} 4/ 5/		9,10,11	01,02,09,10		80	ns
				03-08,11-16		60	
Output hold from address change	t_{AXQX} 4/ 5/		9,10,11	All	0		ns

See footnotes at end of table.

TABLE I. Electrical performance characteristics - Continued.

Test	Symbol	Conditions $-55°C \le T_C \le +125°C$, $V_{SS} = 0$ V, $4.5\ V \le V_{CC} \le 5.5$ V unless otherwise specified 1/	Group A subgroups	Device types	Limits		Unit
					Min	Max	
Write cycle time	t_{WHWL1} t_{EHEL1} 5/	See figure 5 or 7 as applicable	9,10,11	01-06, 08-14, 16		10	ms
				07,15		3	
Address set-up time	t_{AVEL} 5/ t_{AVWL}	See figures 5, 6, or 7 as applicable	9,10,11	All	20		ns
Address hold time	t_{ELAX} 5/ t_{WLAX}		9,10,11	All	150		ns
Write set-up time	t_{WLEL} 5/ t_{ELWL}		9,10,11	All	0		ns
Write hold time	t_{EHWH} 5/ t_{WHEH}		9,10,11	All	0		ns
$\overline{OE}$ set-up time	t_{OHEL} t_{OHWL} 5/		9,10,11	All	20		ns
$\overline{OE}$ hold time	t_{EHOL} t_{WHOL} 5/		9,10,11	All	20		ns
$\overline{WE}$ pulse width	t_{ELEH} t_{WLWH} 5/ 6/		9,10,11	All	.150	1	µs
Data set-up time	t_{DVEH} t_{DVWH} 5/		9,10,11	All	50		ns
Delay to next write	t_{DVWL} 4/ t_{DVEL} 5/		9,10,11	All		10	µs
Data hold time	t_{EHDX} t_{WHDX} 5/		9,10,11	All	10		ns
Byte load cycle	t_{WHWL2} 5/ 6/	See figure 5 or 7 as applicable	9,10,11	All	.20	149	µs

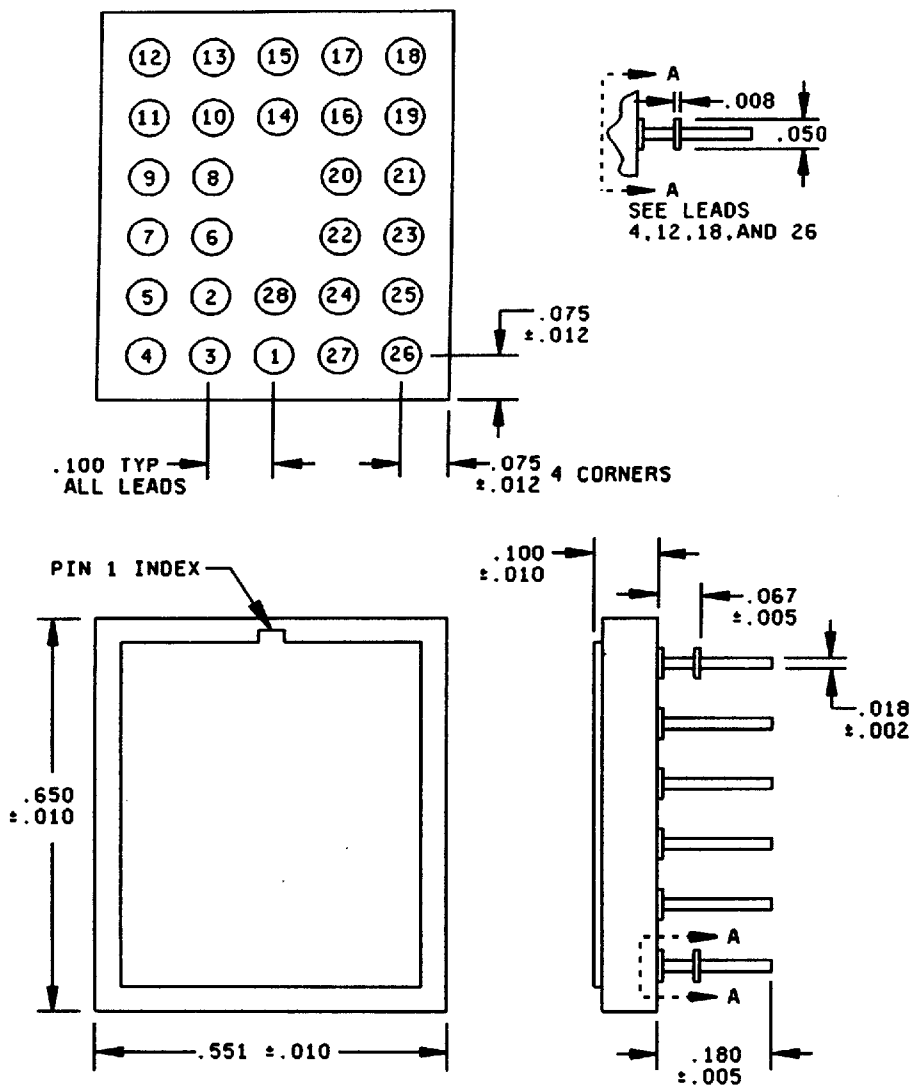
See footnotes at end of table.

TABLE I. Electrical performance characteristics - Continued.

Test	Symbol	Conditions $-55°C \le T_C \le +125°C$, $V_{SS} = 0$ V, $4.5\ V \le V_{CC} \le 5.5$ V unless otherwise specified 1/	Group A subgroups	Device types	Limits		Unit
					Min	Max	
Last byte loaded to data polling	t_{WHEL} t_{EHEL} 5/	See figure 5 or 6 as applicable	9,10,11	All		650	µs
$\overline{CE}$ setup time	t_{ELWL} 5/	See figure 8	9,10,11	All	5		µs
Output set-up time	t_{OVHWL} 5/		9,10,11	All	5		µs
$\overline{CE}$ hold time	t_{WHEH} 5/		9,10,11	All	5		µs
$\overline{OE}$ hold time	t_{WHOH} 5/		9,10,11	All	5		µs
High voltage	V_H 5/		9,10,11	All	12	13	V
Chip erase	t_{WLWH2} 5/		9,10,11	All		210	ms
$\overline{WE}$ pulse width for chip erase	t_{WLWH1} 5/		9,10,11	All	10		ms

1/ DC and read mode.
2/ Connect all address inputs and $\overline{OE}$ to V_{IH} and measure I_{OLZ} and I_{OHZ} with the output under test connected to V_{OUT}.
3/ All pins not being tested are to be open.
4/ Tested initially and after any design or process changes that affect that parameter, and therefore shall be guaranteed to the limits specified in table I.
5/ Tested by application of specified timing signals and conditions, including:
Equivalent ac test conditions:
Devices: All.
Output load: 1 TTL gate and C_L = 100 pF (minimum) or equivalent circuit.
Input rise and fall times ≤ 10 ns.
Input pulse levels: 0.4 V and 2.4 V.
Timing measurements reference levels:
Inputs: 1 V and 2 V.
Outputs: 0.8 V and 2 V.
6/ During a page write operation the cycle time defined by t_{WLWH} and t_{WHWL2} shall not be less than 1 µs.

Case U



NOTES:
1. Dimensions are in inches.
2. Metric equivalents are given for general information only.

Inches	mm
.002	0.05
.005	0.13
.008	0.20
.010	0.25
.012	0.30
.050	1.27
.067	1.70
.075	1.90
.100	2.54
.180	4.57
.551	14.00
.650	16.51

FIGURE 1. Case outline.

Device types	All	
Case outlines	U, X, Z	Y
Terminal numbers	Terminal symbols	
1	A_{14}	NC
2	A_{12}	A_{14}
3	A_7	A_{12}
4	A_6	A_7
5	A_5	A_6
6	A_4	A_5
7	A_3	A_4
8	A_2	A_3
9	A_1	A_2
10	A_0	A_1
11	I/O_0	A_0
12	I/O_1	NC
13	I/O_2	I/O_0
14	V_{SS}	I/O_1
15	I/O_3	I/O_2
16	I/O_4	V_{SS}
17	I/O_5	NC
18	I/O_6	I/O_3
19	I/O_7	I/O_4
20	$\overline{CE}$	I/O_5
21	A_{10}	I/O_6
22	$\overline{OE}$	I/O_7
23	A_{11}	$\overline{CE}$
24	A_9	A_{10}
25	A_8	$\overline{OE}$
26	A_{13}	NC
27	$\overline{WE}$	A_{11}
28	V_{CC}	A_9
29	---	A_8
30	---	A_{13}
31	---	$\overline{WE}$
32	---	V_{CC}

FIGURE 2. Terminal connections.

Mode	$\overline{CE}$	$\overline{OE}$	$\overline{WE}$	I/O	Device type
Read	V_{IL}	V_{IL}	V_{IH}	D_{OUT}	All
Standby	V_{IH}	X	X	High Z	All
Chip clear	V_{IL}	V_H	V_{IL}	$D_{IN} = V_{IH}$	All
Byte write	V_{IL}	V_{IH}	V_{IL}	Data in	All
Write inhibit	X	V_{IL}	X	High Z/D out	All
Write inhibit	X	X	V_{IH}	High Z/D out	All

X = Don't care state.

FIGURE 3. Truth table for unprogrammed devices.

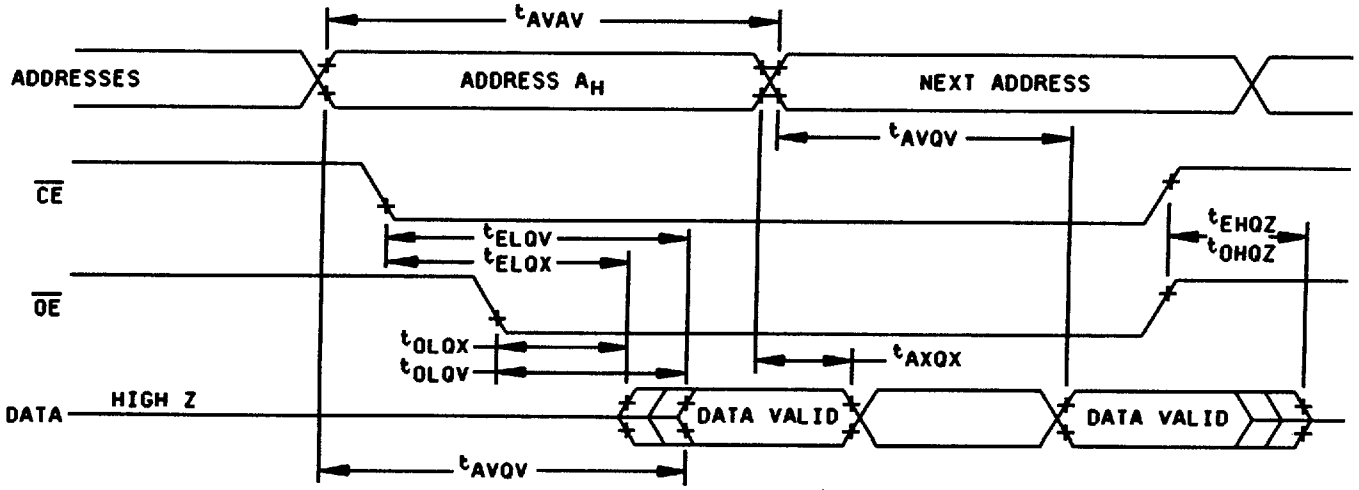


FIGURE 4. Read cycle timing waveform.

STANDARDIZED MILITARY DRAWING DEFENSE ELECTRONICS SUPPLY CENTER DAYTON, OHIO 45444	SIZE A		5962-88525
		REVISION LEVEL B	SHEET 11

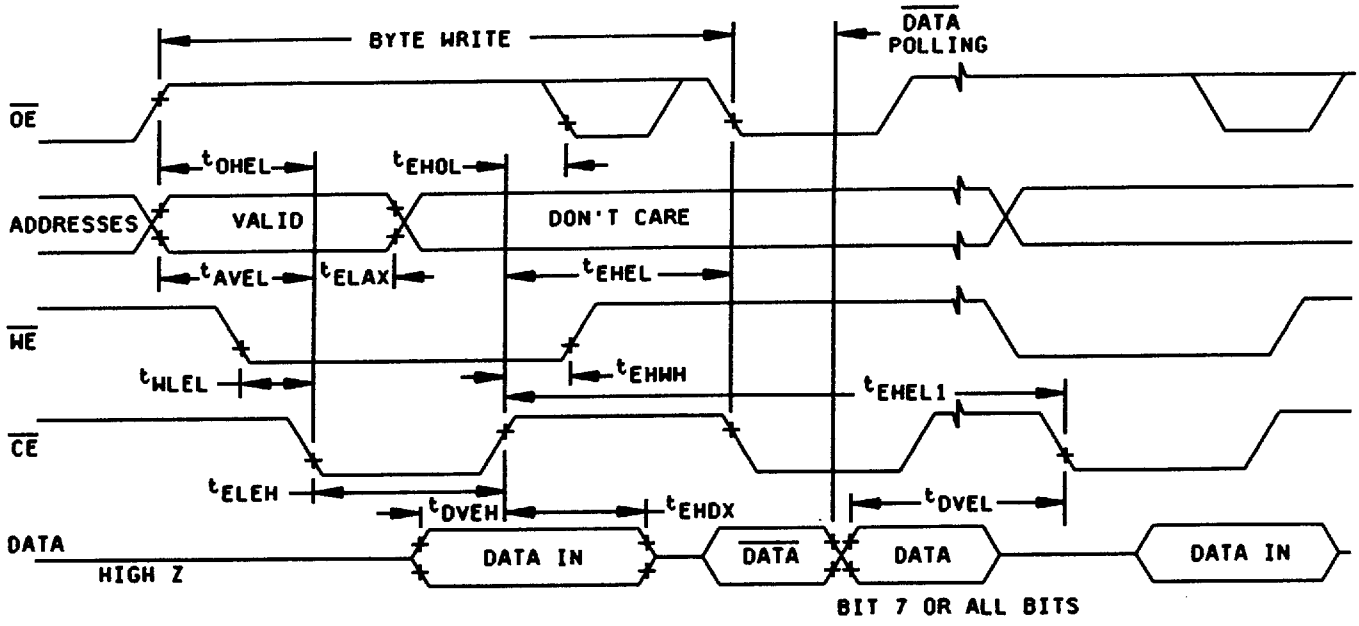


FIGURE 5. $\overline{CE}$ controlled byte write programming waveform.

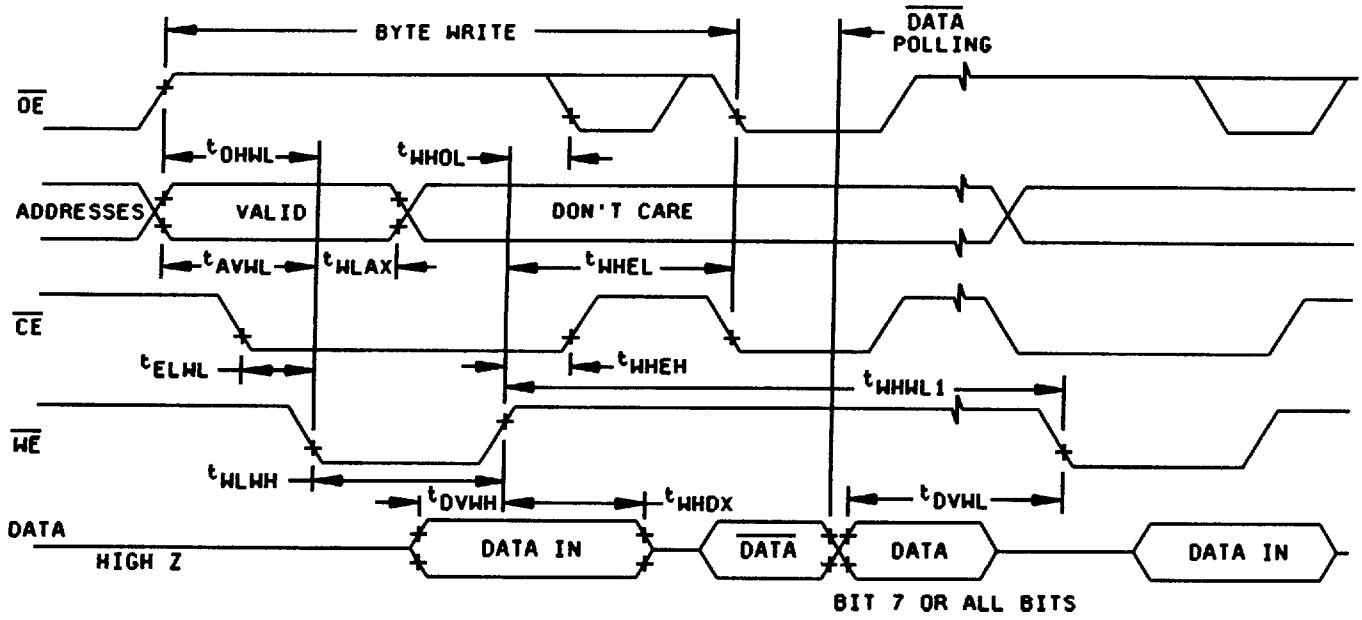


FIGURE 6. $\overline{WE}$ controlled byte write programming waveform.

STANDARDIZED MILITARY DRAWING DEFENSE ELECTRONICS SUPPLY CENTER DAYTON, OHIO 45444	SIZE A		5962-88525
		REVISION LEVEL B	SHEET 13

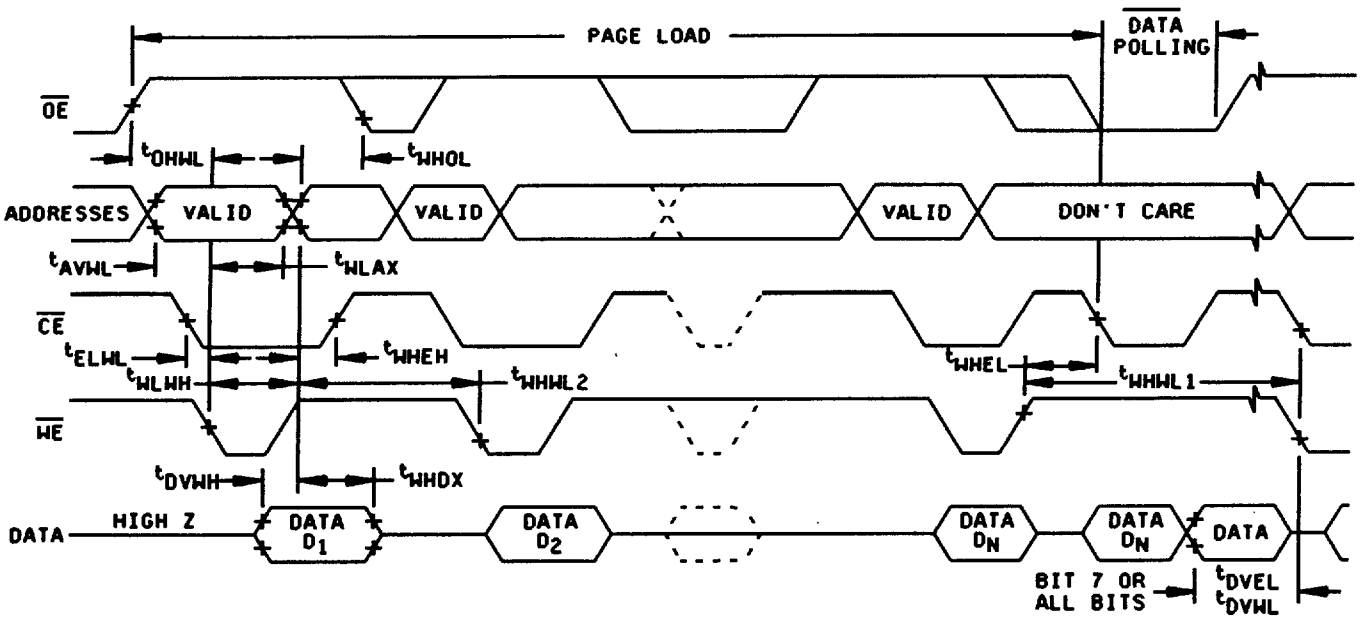


FIGURE 7. Page write programming waveform.

STANDARDIZED MILITARY DRAWING DEFENSE ELECTRONICS SUPPLY CENTER DAYTON, OHIO 45444	SIZE A		5962-88525
		REVISION LEVEL B	SHEET 14

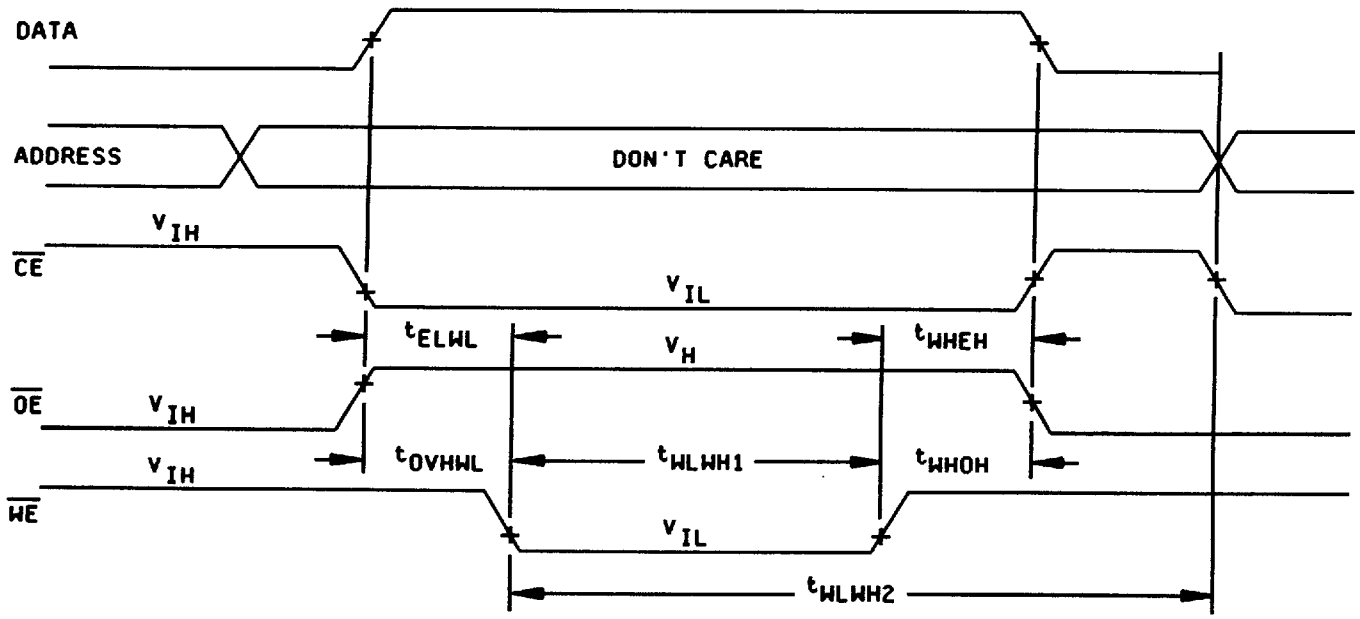
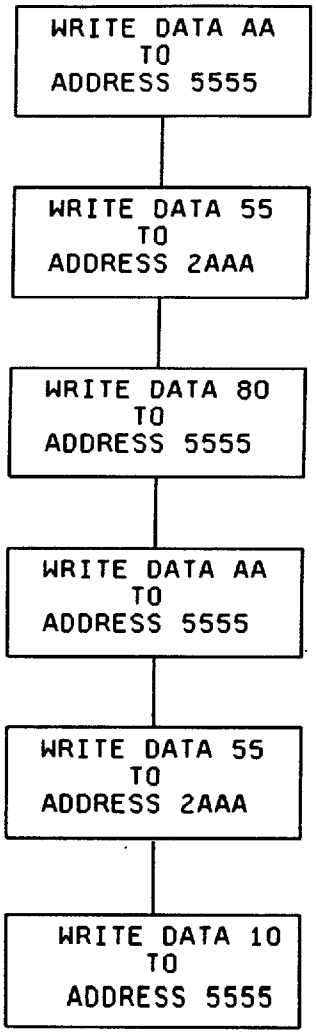
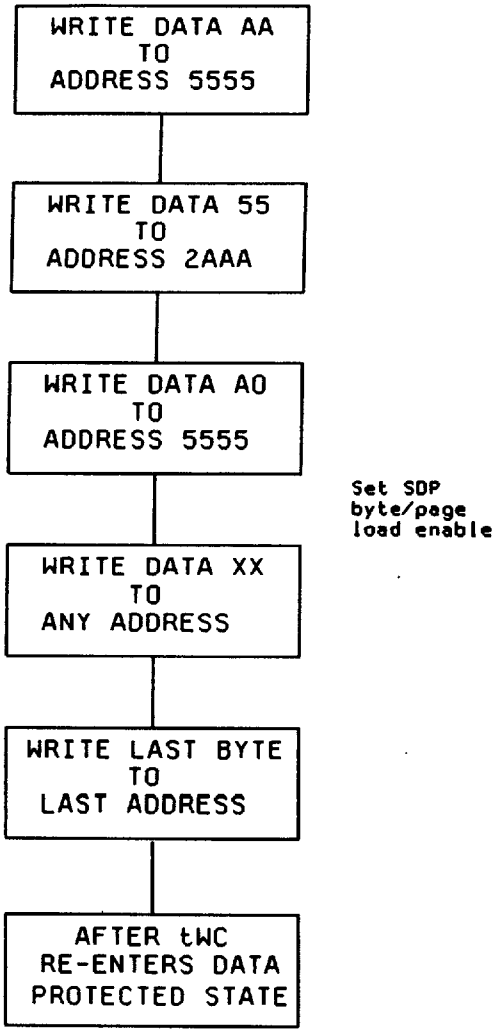


FIGURE 8. Timer chip clear waveform.



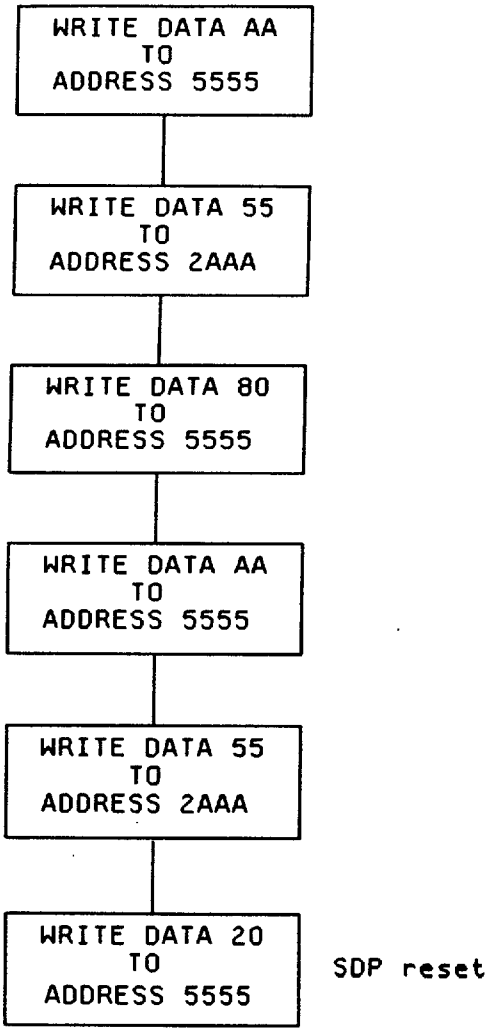
NOTES:
1. Software chip clear timings are referenced to $\overline{WE}$ or $\overline{CE}$ inputs, whichever is last to go low, and the $\overline{WE}$ or $\overline{CE}$ inputs, whichever is first to go high.
2. The command sequence must conform to the page write timing.

FIGURE 9. Software chip clear algorithm (device types 09-16).



NOTES:
1. Software data protection timings are referenced to the $\overline{WE}$ or $\overline{CE}$ inputs, whichever is last to go low, and the $\overline{WE}$ or $\overline{CE}$ inputs, whichever is first to go high.
2. The command sequence and subsequent data must conform to page write timing.

FIGURE 10. Set software data protect algorithm (device types 09-16).



NOTES:
1. Reset software data protection timings are referenced to the $\overline{WE}$ or $\overline{CE}$ inputs, whichever is last to go low, and the $\overline{WE}$ or $\overline{CE}$ inputs, whichever is first to go high.
2. The command sequence and subsequent data must conform to page write timing.

FIGURE 11. Reset software data protect algorithm(device types 09-16).

3.4 Electrical test requirements. The electrical test requirements shall be the subgroups specified in table II. The electrical tests for each subgroup are described in table I.

3.5 Marking. Marking shall be in accordance with MIL-STD-883 (see 3.1 herein). The part shall be marked with the PIN listed in 1.2 herein. In addition, the manufacturer's PIN may also be marked as listed in MIL-BUL-103 (see 6.6 herein).

3.6 Certificate of compliance. A certificate of compliance shall be required from a manufacturer in order to be listed as an approved source of supply in MIL-BUL-103 (see 6.6 herein). The certificate of compliance submitted to DESC-EC prior to listing as an approved source of supply shall affirm that the manufacturer's product meets the requirements of MIL-STD-883 (see 3.1 herein) and the requirements herein.

3.7 Certificate of conformance. A certificate of conformance as required in MIL-STD-883 (see 3.1 herein) shall be provided with each lot of microcircuits delivered to this drawing.

3.8 Notification of change. Notification of change to DESC-EC shall be required in accordance with MIL-STD-883 (see 3.1 herein).

3.9 Verification and review. DESC, DESC's agent, and the acquiring activity retain the option to review the manufacturer's facility and applicable required documentation. Offshore documentation shall be made available onshore at the option of the reviewer.

3.10 Processing EEPROMS. All testing requirements and quality assurance provisions herein shall be satisfied by the manufacturer prior to delivery.

3.10.1 Erasure of EEPROMS. When specified, devices shall be erased in accordance with the procedures and characteristics specified in 4.4.3. Devices shall be shipped in the erased (logic "1's) and verified state unless otherwise specified.

3.10.2 Programmability of EEPROMS. When specified, devices shall be programmed to the specified pattern using the procedures and characteristics specified in 4.4.2. Software data protect procedures shall be as specified in 4.4.5.

3.10.3 Verification of erasure or programmability of EEPROMS. When specified, devices shall be verified as either programmed to the specified pattern or erased. As a minimum, verification shall consist of reading the device per the procedures and characteristics specified in 4.4.4. Any bit that does not verify to be in the proper state shall constitute a device failure, and shall be removed from the lot.

4. QUALITY ASSURANCE PROVISIONS

4.1 Sampling and inspection. Sampling and inspection procedures shall be in accordance with section 4 of MIL-M-38510 to the extent specified in MIL-STD-883 (see 3.1 herein).

4.2 Screening. Screening shall be in accordance with method 5004 of MIL-STD-883, and shall be conducted on all devices prior to quality conformance inspection. The following additional criteria shall apply:

a. Burn-in test, method 1015 of MIL-STD-883.

(1) Test condition D or F. The test circuit shall be maintained by the manufacturer under document revision level control and shall be made available to the preparing or acquiring activity upon request. The test circuit shall specify the inputs, outputs, biases, and power dissipation, as applicable, in accordance with the intent specified in test method 1015 of MIL-STD-883.

(2) T_A = +125°C, minimum.

(3) Devices shall be burned-in containing a checkerboard pattern or equivalent.

b. Interim and final electrical test parameters shall be as specified in table II herein, except interim electrical parameter tests prior to burn-in are optional at the discretion of the manufacturer.

c. An endurance/data retention test prior to burn-in, in accordance with method 1033 of MIL-STD-883, shall be included as part of the screening procedure with the following conditions:

(1) Cycling may be block, byte, or page at equipment room ambient temperature and shall cycle all bytes for a minimum of 10,000 cycles for devices 01-04, 06,07, 09-12, 14,15 and a minimum of 50,000 cycles for device 05,08,13, and 16.

(2) After cycling, perform a high temperature unbiased bake for 72 hours at +150°C (minimum). The storage time may be accelerated by using higher temperature in accordance with the Arrhenius Relationship:

$$A_F = e^{-\frac{E_A}{K}\left[\frac{1}{T_1}-\frac{1}{T_2}\right]}$$

A_F = acceleration factor (unitless quantity) = t_1/t_2
T = temperature in Kelvin (i.e., t_1+ 273)
t_1 = time (hrs) at temperature T_1
t_2 = time (hrs) at temperature T_2
K = Boltzmanns constant = 8.62 x 10^{-5}eV/°K using an apparent activation energy (E_A) of 0.6 eV.

The maximum storage temperature shall not exceed +200°C for packaged devices or +300°C for unassembled devices.

(3) Read the data retention pattern and test using subgroups 1, 7, and 9 (minimum, e.g., high temperature equivalent subgroups 2, 8A, and 10 may be used) after cycling and bake, prior to burn-in. Devices having bits not in the proper state after storage shall constitute a device failure.

4.3 Quality conformance inspection. Quality conformance inspection shall be in accordance with method 5005 of MIL-STD-883 including groups A, B, C, and D inspections. The following additional criteria shall apply.

4.3.1 Group A inspection.

a. Tests shall be as specified in table II herein.

b. Subgroups 5 and 6 in table I, method 5005 of MIL-STD-883 shall be omitted.

c. Subgroup 4 (C_I and C_O measurements) shall be measured only for the initial test and after process or design changes which may affect input capacitance.

d. Subgroups 7 and 8 shall include verification of the truth table.

4.3.2 Group C inspections. Group C inspection shall be in accordance with table III of method 5005 of MIL-STD-883 and as follows:

a. End-point electrical parameters shall be as specified in table II herein.

b. All devices requiring end-point electrical testing shall be programmed with a checkerboard or equivalent alternating bit pattern.

c. Steady-state life test conditions, method 1005 of MIL-STD-883.

(1) Test condition D or F using the circuit submitted with the certificate of compliance (see 3.6 herein).

(2) T_A = +125°C, minimum.

(3) Test duration: 1,000 hours, except as permitted by method 1005 of MIL-STD-883.

d. An endurance test, in accordance with method 1033 of MIL-STD-883, shall be added to group C1 inspection prior to performing the steady-state life test (see 4.3.2c) and extended data retention (see 4.3.2e).

Cycling may be block, byte, or page from devices passing group A after the completion of the requirements of 4.2 herein. Initially, two groups of devices shall be formed, cell 1 and cell 2.

The following conditions shall be met:

(1) Cell 1 shall be cycled at -55°C and cell 2 shall be cycled at +125°C for a minimum of 10,000 cycles for device types 01-04,06,07,09-12,14,15 and 100,000 cycles for device types 05,08,13, and 16.

(2) Perform group A subgroups 1, 7, and 9 after cycling. Form two new cells (cells 3 and 4) for steady-state life and extended data retention. Cell 3 for steady-state life test consists of one-half of the devices from cell 1 and one-half of the devices from cell 2. Cell 4 for extended data retention consists of the remaining devices from cells 1 and 2.

(3) The sample plans for cell 1, cell 2, cell 3, and cell 4 shall individually be the same as for group C1, as specified in method 5005 of MIL-STD-883.

e. Extended data retention shall consist of:

(1) All devices shall be programmed with a charge on all memory cells in each device, such that the cell will read opposite the state that the cell would read in its equilibrium state (e.g., worst case pattern, see 4.2a(3)).

(2) Unbiased bake for 1000 hours (minimum) at +150°C (minimum). The unbiased bake time may be accelerated by using higher temperature in accordance with the Arrhenius Relationship:

$$A_F = e^{-\frac{E_A}{K}\left[\frac{1}{T_1}-\frac{1}{T_2}\right]}$$

A_F = acceleration factor (unitless quantity) = t_1/t_2
T = temperature in Kelvin (i.e., t_1 + 273)
t_1 = time (hrs) at temperature T_1
t_2 = time (hrs) at temperature T_2
K = Boltzmanns constant = 8.62×10^{-5} eV/°K using an apparent activation energy (E_A) of 0.6 eV.

The maximum storage temperature shall not exceed +200°C for packaged devices or +300°C for unassembled devices.

(3) Read the pattern after bake and perform endpoint electrical tests for table II herein for group C.

4.3.3 Groups D inspections. Group D inspection shall be in accordance with table IV of method 5005 of MIL-STD-883 and as follows:

a. End-point electrical parameters shall be as specified in table II herein.

b. All devices requiring end-point electrical testing shall be programmed with a checkerboard or equivalent alternating bit pattern.

TABLE II. Electrical test requirements.

MIL-STD-883 test requirements	Subgroups (in accordance with method 5005, table I)
Interim electrical parameters (method 5004)	1,7,9, or 2,8 (+125°C),10
Final electrical test parameters (method 5004)	1*,2,3,7*,8,9,10,11
Group A test requirements (method 5005)	1,2,3,4**,7,8,9,10,11
Groups C and D end-point electrical parameters (method 5005)	1,2,3,7,8,9,10,11

1. (*) Indicates PDA applies to subgroups 1 and 7.
2. Any or all subgroups may be combined when using multifunction testers.
3. Subgroup 7 and 8 shall consist of writing and reading the data pattern specified in accordance with the limits of table I subgroups 9, 10, and 11.
4. For all electrical tests, the device shall be programmed to the data pattern specified.
5. (**) Indicates that subgroup 4 will only be performed during initial qualification and after design or process changes (see 4.3.1c).

4.4 Methods of inspection. Methods of inspection shall be as specified in the appropriate tables of method 5005 of MIL-STD-883 and as follows.

4.4.1 Voltage and current. All voltages given are referenced to the microcircuit V_{SS} terminal. Currents given are conventional current and positive when flowing into the referenced terminal.

4.4.2 Programming procedure. The following procedure shall be followed when programming (Write) is performed. The waveforms and timing relationships shown on figure 5 (in accordance with appropriate device type) and the conditions specified in table I shall be adhered to. Information is introduced by selectively programming a TTL low or TTL high on each I/O of the address desired. Functionality shall be verified at all temperatures (group A subgroups 7 and 8) by programming all bytes of each device and verifying the pattern used.

4.4.3 Erasing procedure. There are two forms of erasure, chip and byte, whereby all bits or the address selected will be erased to a TTL high.

a. Chip erase is performed in accordance with the waveforms and timing relationships shown on figure 8 (in accordance with appropriate device type) and the conditions specified in table I.

b. Byte erase is performed in accordance with the waveforms and timing relationships shown on figures 5, 6, and 7 (in accordance with appropriate device type) and the conditions specified in table I.

4.4.4 Read mode operation. The waveforms and timing relationships shown on figure 4 and the conditions specified in table I shall be applied when reading the device. Pattern verification utilizes the read mode.

4.4.5 Software data protection. Device types 09-16 software data protection offers a method of preventing inadvertent writes (see figure 9). The instructions, waveforms, and timing relationships shown on figures 4, 5, 6, 7, 10, and 11, and the conditions specified in table I shall apply (see 3.10.2).

4.4.5.1 Set software data protection. Device types 09-16 are placed in protected state by writing a series of instructions (see figure 10) to the device. Once protected, writing to the device may only be performed by executing the same sequence of instructions appended with either a byte write operation or page write operation. The waveforms and timing relationships shown on figures 5, 6, and 7 and the test conditions and limits specified in table I shall apply.

4.4.5.2 Reset software data protection. Device types 09-16 protection feature is reset by writing a series of instructions (see figure 11) to the device. The waveforms and timing relationships shown on figures 5, 6, and 7 and the test conditions and limits specified in table I shall apply.

5. PACKAGING

5.1 Packaging requirements. The requirements for packaging shall be in accordance with MIL-M-38510.

6. NOTES

6.1 Intended use. Microcircuits conforming to this drawing are intended for use when military specifications do not exist and qualified military devices that will perform the required function are not available for original equipment manufacturer application. When a military specification exists and the product covered by this drawing has been qualified for listing on QPL-38510, the device specified herein will be inactivated and will not be used for new design. The QPL-38510 product shall be the preferred item for all applications.

6.2 Replaceability. Microcircuits covered by this drawing will replace the same generic device covered by a contractor-prepared specification or drawing.

6.3 Configuration control of SMD's. All proposed changes to existing SMD's will be coordinated with the users of record for the individual documents. This coordination will be accomplished in accordance with MIL-STD-481 using DD Form 1693, Engineering Change Proposal (Short Form).

6.4 Record of users. Military and industrial users shall inform Defense Electronics Supply Center when a system application requires configuration control and the applicable SMD. DESC will maintain a record of users and this list will be used for coordination and distribution of changes to the drawings. Users of drawings covering microelectronics devices (FSC 5962) should contact DESC-EC, telephone (513) 296-6047.

6.5 Comments. Comments on this drawing should be directed to DESC-EC, Dayton, Ohio 45444, or telephone (513) 296-5377.

6.6 Approved sources of supply. Approved sources of supply are listed in MIL-BUL-103. The vendors listed in MIL-BUL-103 have agreed to this drawing and a certificate of compliance (see 3.6 herein) has been submitted to and accepted by DESC-EC.