REVISIONS

LTR	DESCRIPTION	DATE (YR-MO-DA)	APPROVED

REV																																						
SHEET																																						
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REV STATUS OF SHEETS	REV														
	SHEET	1	2	3	4	5	6	7	8	9	10	11	12	13	14

PMIC N/A	PREPARED BY	DEFENSE ELECTRONICS SUPPLY CENTER DAYTON, OHIO 45444

STANDARDIZED MILITARY DRAWING

CHECKED BY

APPROVED BY

THIS DRAWING IS AVAILABLE FOR USE BY ALL DEPARTMENTS AND AGENCIES OF THE DEPARTMENT OF DEFENSE

AMSC N/A

DRAWING APPROVAL DATE
30 MAY 1989

REVISION LEVEL

MICROCIRCUITS, LINEAR, CMOS, 8-BIT, MICROPROCESSOR COMPATIBLE, A/D CONVERTER WITH TRACK/HOLD, MONOLITHIC SILICON

SIZE	CAGE CODE	
A	67268	5962-88650

SHEET	1

1. SCOPE

1.1 <u>Scope</u>. This drawing describes device requirements for class B microcircuits in accordance with 1.2.1 of MIL-STD-883, "Provisions for the use of MIL-STD-883 in conjunction with compliant non-JAN devices".

1.2 <u>Part number</u>. The complete part number shall be as shown in the following example:

5962-88650	01	R	X
Drawing number	Device type (1.2.1)	Case outline (1.2.2)	Lead finish per MIL-M-38510

1.2.1 <u>Device types</u>. The device types shall identify the circuit function as follows:

Device type	Generic number	Circuit function	Total unadjusted error
01	AD7820U	CMOS 8-bit ADC with T/H	±0.5 LSB
02	AD7820T	CMOS 8-bit ADC with T/H	±1.0 LSB

1.2.2 <u>Case outlines</u>. The case outlines shall be as designated in appendix C of MIL-M-38510, and as follows:

Outline letter	Case outline
R	D-8 (20-lead, 1.060" x .310" x .200"), dual-in-line package
2	C-2 (20-terminal, .358" x .358" x .100"), square chip carrier package

1.3 <u>Absolute maximum ratings</u>. 1/

Supply voltage to ground (V_{DD}) $- - - - - - - - - -$	0 V dc to +7.0 V dc
Digital input voltage $- - - - - - - - - - - - - -$	-0.3 V dc to V_{DD}
Digital output voltage $- - - - - - - - - - - - -$	-0.3 V dc to V_{DD}
Positive reference voltage $- - - - - - - - - - -$	V_{REF-} to V_{DD}
Negative reference voltage $- - - - - - - - - - -$	0 V dc to V_{REF+}
Input voltage (V_{IN}) $- - - - - - - - - - - - -$	-0.3 V dc to V_{DD}
Storage temperature range $- - - - - - - - - - - -$	-65°C to +150°C
Lead temperature (soldering, 10 seconds) $- - - - - -$	+300°C
Power dissipation (P_D) $- - - - - - - - - - - - -$	450 mW 2/
Thermal resistance, junction-to-case (θ_{JC}):	
Cases R and 2 $- - - - - - - - - - - - - - - - - - - -$	See MIL-M-38510, appendix C
Thermal resistance, junction-to-ambient (θ_{JA}):	
Cases R and 2 $- - - - - - - - - - - - - - - - - - - -$	120°C/W
Junction temperature (T_J) $- - - - - - - - - - - - -$	+150°C

1.4 <u>Recommended operating conditions</u>.

Supply voltage range (V_{DD}) $- - - - - - - - - - - -$	+4.75 V dc to +5.25 V dc
Positive reference voltage (V_{REF+}) $- - - - - - - -$	+5.0 V dc
Negative reference voltage (V_{REF-}) $- - - - - - - -$	0 V dc
Ground potential (GND) $- - - - - - - - - - - - - -$	0 V dc
Ambient operating temperature range (T_A) $- - - - - -$	-55°C to +125°C

1/ All voltages are with respect to ground.
2/ Derate above T_A = +75°C at 6.0 mW/°C.

<table>
<tr>
<td rowspan="2">STANDARDIZED
MILITARY DRAWING</td>
<td>SIZE</td>
<td rowspan="2"></td>
<td rowspan="2">5962-88650</td>
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<tr>
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<tr>
<td>DEFENSE ELECTRONICS SUPPLY CENTER
DAYTON, OHIO 45444</td>
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<td>REVISION LEVEL</td>
<td>SHEET
2</td>
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2. APPLICABLE DOCUMENTS

2.1 Government specification and standard. Unless otherwise specified, the following specification and standard, of the issue listed in that issue of the Department of Defense Index of Specifications and Standards specified in the solicitation, form a part of this drawing to the extent specified herein.

SPECIFICATION

  MILITARY

    MIL-M-38510 - Microcircuits, General Specification for.

STANDARD

  MILITARY

    MIL-STD-883 - Test Methods and Procedures for Microelectronics.

(Copies of the specification and standard required by manufacturers in connection with specific acquisition functions should be obtained from the contracting activity or as directed by the contracting activity.)

2.2 Order of precedence. In the event of a conflict between the text of this drawing and the references cited herein, the text of this drawing shall take precedence.

3. REQUIREMENTS

3.1 Item requirements. The individual item requirements shall be in accordance with 1.2.1 of MIL-STD-883, "Provisions for the use of MIL-STD-883 in conjunction with compliant non-JAN devices" and as specified herein.

3.2 Design, construction, and physical dimensions. The design, construction, and physical dimensions shall be as specified in MIL-M-38510 and herein.

3.2.1 Terminal connections. The terminal connections shall be as specified on figure 1.

3.2.2 Case outlines. The case outlines shall be in accordance with 1.2.2 herein.

3.3 Electrical performance characteristics. Unless otherwise specified, the electrical performance characteristics are as specified in table I and apply over the full ambient operating temperature range.

3.4 Marking. Marking shall be in accordance with MIL-STD-883 (see 3.1 herein). The part shall be marked with the part number listed in 1.2 herein. In addition, the manufacturer's part number may also be marked as listed in 6.4 herein.

3.5 Certificate of compliance. A certificate of compliance shall be required from a manufacturer in order to be listed as an approved source of supply in 6.4. The certificate of compliance submitted to DESC-ECS prior to listing as an approved source of supply shall state that the manufacturer's product meets the requirements of MIL-STD-883 (see 3.1 herein) and the requirements herein.

3.6 Certificate of conformance. A certificate of conformance as required in MIL-STD-883 (see 3.1 herein) shall be provided with each lot of microcircuits delivered to this drawing.

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TABLE I. Electrical performance characteristics.

Test	Symbol	Conditions 1/ 2/ $-55°C \leq T_A \leq +125°C$ unless otherwise specified	Group A subgroups	Device types	Limits Min	Limits Max	Unit
Resolution	RES	This is the minimum resolution for which no missing codes are guaranteed.	1, 2, 3	All	8.0		LSB
Total unadjusted error	TUE	3/	1	01		±1	
			2, 3, 12			±0.5	
			1, 2, 3	02		±1	LSB
Analog input leakage current	I_{IN}		1, 2, 3	All		±3.0	μA
Analog input capacitance	C_{IA}	See 4.3.1c, $T_A = +25°C$	4	All		60	pF
Reference input resistance	R_{IN}		1, 2, 3	All	1.0	4.0	kΩ
Digital input high level voltage	V_{IH}	$\overline{CS}$, $\overline{WR}$, and $\overline{RD}$ inputs (Pin 7)	1, 2, 3	All	2.4		V
		Mode input			3.5		
Digital input low level voltage	V_{IL}	$\overline{CS}$, $\overline{WR}$, and $\overline{RD}$ inputs (Pin 7)	1, 2, 3	All		0.8	V
		Mode input				1.5	
Digital input high current	I_{IH}	$\overline{CS}$ and $\overline{RD}$ inputs	1, 2, 3	All		±1.0	μA
		$\overline{WR}$ input				±3.0	
		Mode input (Pin 7)				±200	

See footnotes at end of table.

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TABLE I. Electrical performance characteristics - Continued.

Test	Symbol	Conditions 1/ 2/ $-55°C \leq T_A \leq +125°C$ unless otherwise specified	Group A subgroups	Device types	Limits		Unit
					Min	Max	
Digital input low current	I_{IL}	$\overline{CS}$, $\overline{WR}$, $\overline{RD}$, and mode inputs (Pin 7)	1, 2, 3	All		-1.0	µA
Digital input capacitance	C_{ID}	$\overline{CS}$, $\overline{WR}$, $\overline{RD}$, and mode inputs, See 4.3.1c, T_A = +25°C	4	All		8.0	pF
Digital output high level voltage	V_{OH}	DB_0 - DB_7, $\overline{OFL}$, and $\overline{INT}$ outputs, I_{SOURCE} = 360 µA	1, 2, 3	All	4.0		V
Digital output low level voltage	V_{OL}	DB_0 - DB_7, $\overline{OFL}$, and $\overline{INT}$ outputs, I_{SINK} = 1.6 mA	1, 2, 3	All		0.4	V
Floating state leakage current	I_{OUT}	DB_0 - DB_7	1, 2, 3	All		±3.0	µA
Digital output capacitance	C_{OUT}	See 4.3.1c, T_A = +25°C	4	All		8.0	pF
Supply current from V_{DD}	I_{DD}	$\overline{CS}$ = $\overline{RD}$ = 0 V	1, 2, 3	All		20.0	mA
Power supply sensitivity	PSS	V_{DD} = 5.0 V ±5%	1, 2, 3	All		±.25	LSB
$\overline{CS}$ to $\overline{RD}/\overline{WR}$ setup time	t_{CSS}	6/ 7/	9,10,11	All	0		ns
$\overline{CS}$ to $\overline{RD}/\overline{WR}$ hold time	t_{CSH}	6/ 7/	9,10,11	All	0		ns
$\overline{CS}$ to RDY delay	t_{RDY}	C_L = 50 pF, pull-up resistor = 2.0 kΩ	9	All		70	ns
		6/ 7/	10, 11			100	
Conversion time ($\overline{RD}$ mode)	t_{CRD}	See figure 3. 7/	9	All		1.6	µs
			10, 11			2.5	

See footnotes at end of table.

TABLE I. Electrical performance characteristics - Continued.

Test	Symbol	Conditions 1/ 2/ -55°C $\leq$ T$_A$ $\leq$ +125°C unless otherwise specified	Group A subgroups	Device types	Limits Min	Limits Max	Unit
Data access time (RD mode)	t$_{ACCO}$	4/ 7/	9	All		1.62	ns
			10, 11			2.55	
RD to INT delay (RD mode)	t$_{INTH}$	C$_L$ = 50 pF 7/	9	All		175	ns
			10, 11			225	
Data hold time	t$_{DH}$	5/ 6/ 7/	9	All		60	ns
			10, 11			100	
Delay time between conversion	tp	6/ 7/	9	All	500		ns
			10, 11		600		
Write pulse width	t$_{WR}$	6/	9,10,11	All	0.6	50	µs
Delay time between WR and RD pulses	t$_{RD}$	6/	9	All	600		ns
			10, 11		700		
Data access time (WR/RD mode)	t$_{ACC1}$	4/ 6/	9	All		160	ns
			10, 11			250	
RD to INT delay	t$_{R1}$	6/	9	All		140	ns
			10, 11			225	

See footnotes at end of table.
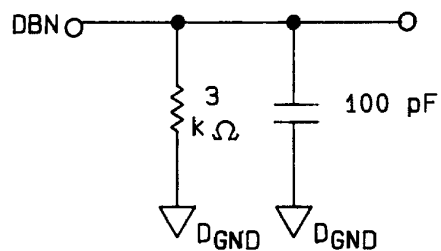
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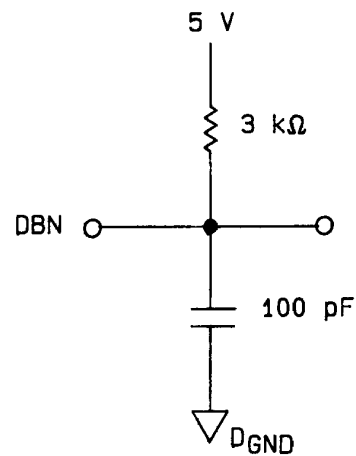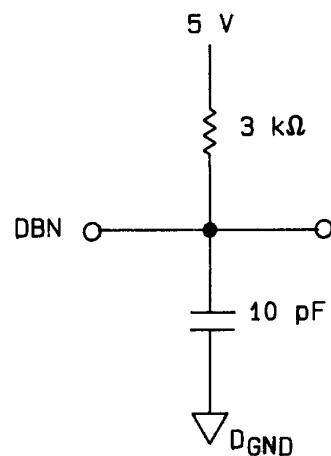DESC FORM 193A
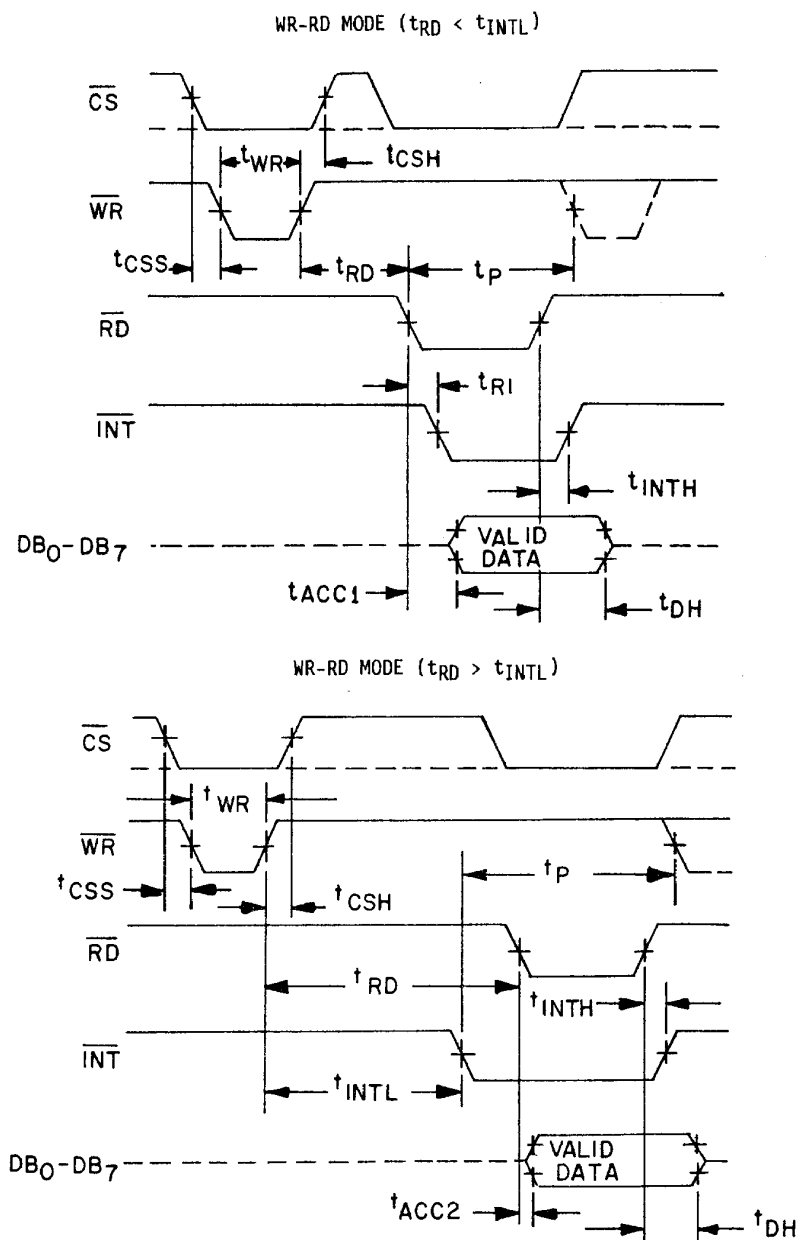SEP 87

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TABLE I. Electrical performance characteristics - Continued.

Test	Symbol	Conditions 1/ 2/ $-55°C \leq T_A \leq +125°C$ unless otherwise specified	Group A subgroups	Device types	Limits		Unit
					Min	Max	
$\overline{WR}$ to $\overline{INT}$ delay	t_{INTL}	$C_L = 50$ pF 6/	9	All		1.0	µs
			10, 11			1.7	
Data access time ($\overline{WR}/\overline{RD}$ mode)	t_{ACC2}	4/ 6/	9	All		70	ns
			10, 11			110	
$\overline{WR}$ to $\overline{INT}$ delay (Stand alone operation)	t_{IHWR}	$C_L = 50$ pF 6/	9	All		100	ns
			10, 11			150	
Data access time after $\overline{INT}$ (Stand alone operation)	t_{ID}	6/	9	All		50	ns
			10, 11			75	

1/ $V_{DD} = +5.0$ V; $V_{REF}(+) = +5.0$ V; $V_{REF}(-) = GND = 0$ V unless otherwise specified. Specifications apply for $\overline{RD}$ mode (Pin 7 = 0 V).

2/ All input control signals are specified with $t_r = t_f = 20$ ns (10 percent to 90 percent of +5.0 V) and timed from a voltage level of 1.6 V.

3/ Includes gain error, offset error and linearity error.

4/ Measured with load circuits of figure 2 and defined as the time required for an output to cross 0.8 V to 2.4 V.

5/ Defined as the time required for the data lines to change 0.5 V when loaded with the circuits of figure 2 and is measured only for the initial test and after process or design changes which may affect T_{DH}.

6/ Refer to timing diagrams of figure 3. These parameters, if not tested, shall be guaranteed to the limits specified in table I.

7/ Refer to timing diagram of figure 3 ($\overline{RD}$ mode). These parameters are tested to subgroup 9 under group A test requirements.

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Device types	All
Case outlines	R and 2
Terminal number	Terminal symbol
1	V_{IN}
2	$DB_0(LSB)$
3	DB_1
4	DB_2
5	DB_3
6	$\overline{WR}/RDY$
7	Mode
8	$\overline{RD}$
9	$\overline{INT}$
10	GND
11	V_{REF-}
12	V_{REF+}
13	CS
14	DB_4
15	DB_5
16	DB_6
17	$DB_7(MSB)$
18	$\overline{OFL}$
19	NC
20	V_{DD}

FIGURE 1.   Terminal connections.

LOAD CIRCUITS FOR DATA ACCESS TIME

HIGH-Z TO V_{OH}

HIGH-Z TO V_{OL}

LOAD CIRCUITS FOR DATA HOLD TIME

V_{OH} TO HIGH-Z
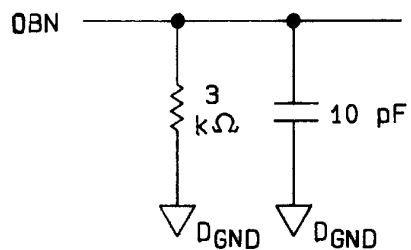
V_{OL} TO HIGH-Z

FIGURE 2. Output load circuits.

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WR-RD MODE ($t_{RD} < t_{INTL}$)

$\overline{CS}$

t_{WR} t_{CSH}

$\overline{WR}$

t_{CSS} t_{RD} t_P

$\overline{RD}$

t_{RI}

$\overline{INT}$

t_{INTH}

$DB_0 - DB_7$ VALID DATA

t_{ACC1} t_{DH}

WR-RD MODE ($t_{RD} > t_{INTL}$)

$\overline{CS}$

t_{WR}

$\overline{WR}$

t_{CSS} t_{CSH} t_P

$\overline{RD}$

t_{RD} t_{INTH}

$\overline{INT}$

t_{INTL}

$DB_0 - DB_7$ VALID DATA

t_{ACC2} t_{DH}

FIGURE 3. Mode timing waveforms.

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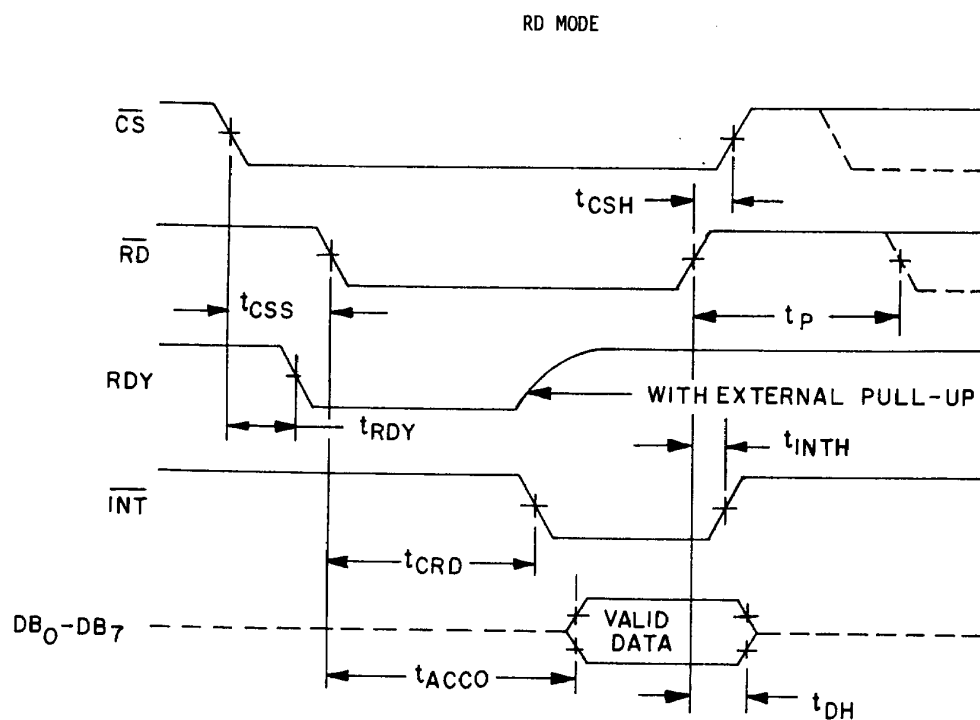
RD MODE

WR-RD MODE STAND-ALONE OPERATION, $\overline{CS} = \overline{RD} = 0$
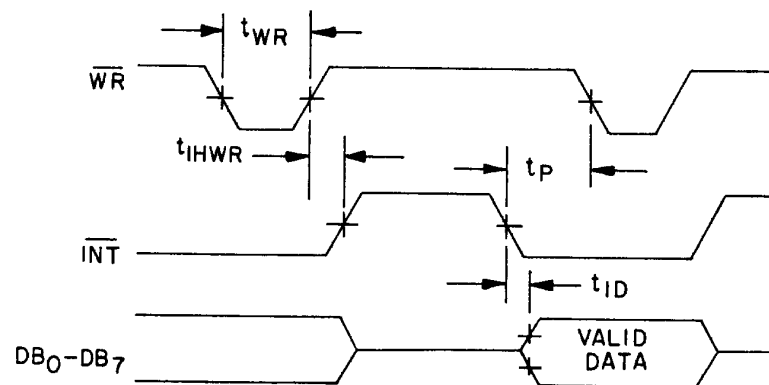
FIGURE 3. Mode timing waveforms - Continued.

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3.7 Notification of change. Notification of change to DESC-ECS shall be required in accordance with MIL-STD-883 (see 3.1 herein).

3.8 Verification and review. DESC, DESC's agent, and the acquiring activity retain the option to review the manufacturer's facility and applicable required documentation. Offshore documentation shall be made available onshore at the option of the reviewer.

4. QUALITY ASSURANCE PROVISIONS

4.1 Sampling and inspection. Sampling and inspection procedures shall be in accordance with section 4 of MIL-M-38510 to the extent specified in MIL-STD-883 (see 3.1 herein).

4.2 Screening. Screening shall be in accordance with method 5004 of MIL-STD-883, and shall be conducted on all devices prior to quality conformance inspection. The following additional criteria shall apply:

    a. Burn-in test, method 1015 of MIL-STD-883.

        (1) Test condition A, B, C, or D using the circuit submitted with the certificate of compliance (see 3.5 herein).

        (2) T_A = +125°C, minimum.

    b. Interim and final electrical test parameters shall be as specified in table II herein, except interim electrical parameter tests prior to burn-in are optional at the discretion of the manufacturer.

4.3 Quality conformance inspection. Quality conformance inspection shall be in accordance with method 5005 of MIL-STD-883 including groups A, B, C, and D inspections. The following additional criteria shall apply.

4.3.1 Group A inspection.

    a. Tests shall be as specified in table II herein.

    b. Subgroups 5, 6, 7, and 8 in table I, method 5005 of MIL-STD-883 shall be omitted.

    c. Subgroup 4 (C_{IA}, C_{ID}, and C_{OUT} measurements) shall be measured only for the initial test and after process or design changes which may affect capacitance.

    d. Subgroup 12 test is used for grading and part selection at T_A = +25°C and is not included in PDA calculations.

4.3.2 Groups C and D inspections.

    a. End-point electrical parameters shall be as specified in table II herein.

    b. Steady-state life, test method 1005 of MIL-STD-883 conditions.

        (1) Test condition A, B, C, or D using the circuit submitted with the certificate of compliance (see 3.5 herein).

        (2) T_A = +125°C, minimum.

        (3) Test duration: 1,000 hours, except as permitted by method 1005 of MIL-STD-883.

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TABLE II. Electrical test requirements.

MIL-STD-883 test requirements	Subgroups (per method 5005, table I)
Interim electrical parameters (method 5004)	1
Final electrical test parameters (method 5004)	1*, 2, 3, 12
Group A test requirements (method 5005)	1, 2, 3, 4, 9, 10**, 11**, 12
Groups C and D end-point electrical parameters (method 5005)	1

* PDA applies to subgroup 1.
** Subgroups 10 and 11 if not tested, are guaranteed to the limits specified in table I.

5. PACKAGING

5.1 Packaging requirements. The requirements for packaging shall be in accordance with MIL-M-38510.

6. NOTES

6.1 Intended use. Microcircuits conforming to this drawing are intended for use when military specifications do not exist and qualified military devices that will perform the required function are not available for OEM application. When a military specification exists and the product covered by this drawing has been qualified for listing on QPL-38510, the device specified herein will be inactivated and will not be used for new design. The QPL-38510 product shall be the preferred item for all applications.

6.2 Replaceability. Microcircuits covered by this drawing will replace the same generic device covered by a contractor-prepared specification or drawing.

6.3 Comments. Comments on this drawing should be directed to DESC-ECS, Dayton, Ohio 45444, or telephone 513-296-5375.

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6.4 Approved source of supply. An approved source of supply is listed herein. Additional sources will be added as they become available. The vendor listed herein has agreed to this drawing and a certificate of compliance (see 3.5 herein) has been submitted to DESC-ECS.

Military drawing part number	Vendor CAGE number	Vendor similar part number 1/	Replacement military specification part number
5962-8865001RX 5962-88650012X	24355 24355	AD7820UQ/883B AD7820UE/883B	M38510/14601BRX M38510/14601B2X
5962-8865002RX 5962-88650022X	24355 24355	AD7820TQ/883B AD7820TE/883B	M38510/14602BRX M38510/14602B2X

1/ Caution. Do not use this number for item acquisition. Items acquired to this number may not satisfy the performance requirements of this drawing.

Vendor CAGE
number

24355

Vendor name
and address

Analog Devices
1 Technology Way
Norwood, MA 02062

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