

REVISIONS			
LTR	DESCRIPTION	DATE (YR-MO-DA)	APPROVED
A	Add footnote 5 to section 1.4. Add footnote 3 to table I. Add vendor CAGE number 34335, 6Y440. Add device type 06. Editorial changes throughout.	92-11-13	M. A. Frye
B	Changes in accordance with NOR 5962-R108-94	94-01-21	M. A. Frye
C	Changes in accordance with NOR 5962-R070-95	95-02-14	M. A. Frye
D	Updated boilerplate. Add device type 07. Add vendor CAGE number 0HGZ7.	97-02-25	Ray Monnin

THE ORIGINAL FIRST PAGE OF THIS DRAWING HAS BEEN REPLACED.

REV																														
SHEET																														
REV	D	D	D	D	D	D	D	D																						
SHEET	15	16	17	18	19	20	21	22																						
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				SHEET		1	2	3	4	5	6	7	8	9	10	11	12	13	14											
PMIC N/A				PREPARED BY Rick Officer					DEFENSE SUPPLY CENTER COLUMBUS COLUMBUS, OHIO 42316-5000																					
STANDARD MICROCIRCUIT DRAWING THIS DRAWING IS AVAILABLE FOR USE BY ALL DEPARTMENTS AND AGENCIES OF THE DEPARTMENT OF DEFENSE AMSC N/A				CHECKED BY Ray Monnin																										
				APPROVED BY Michael Frye																										
				DRAWING APPROVAL DATE 89-02-10																										
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										SIZE A	CAGE CODE 67268	5962-88669																		
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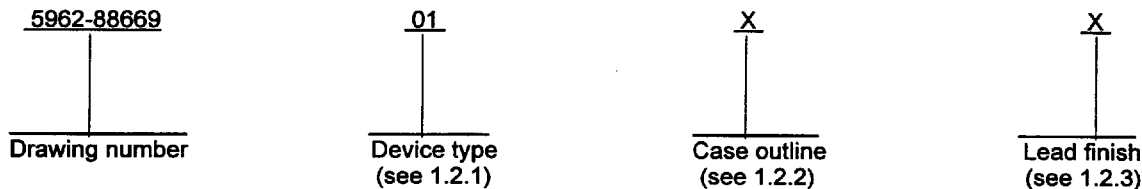
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1. SCOPE

1.1 Scope. This drawing describes device requirements for MIL-STD-883 compliant, non-JAN class level B microcircuits in accordance with MIL-PRF-38535, appendix A.

1.2 Part or Identifying Number (PIN). The complete PIN shall be as shown in the following example:



1.2.1 Device type(s). The device type(s) shall identify the circuit function as follows:

Device type	Generic number	Circuit function	Access time
01	See 6.6	2048 X 9 FIFO	80 ns
02	See 6.6	2048 X 9 FIFO	65 ns
03	See 6.6	2048 X 9 FIFO	50 ns
04	See 6.6	2048 X 9 FIFO	40 ns
05	See 6.6	2048 X 9 FIFO	30 ns
06	See 6.6	2048 X 9 FIFO	20 ns
07	See 6.6	2048 X 9 FIFO	25 ns

1.2.2 Case outlines. The case outlines shall be as designated in MIL-STD-1835 and as follows:

Outline letter	Descriptive designator	Terminals	Package style
X	GDIP1-T28 or CDIP2-T28	28	Dual-in-line package
Y	CDIP3-T28 or GDIP4-T28	28	Dual-in-line package
Z	CQCC1-N32	32	Rectangular leadless chip carrier
U	GDIP2-F28	28	Flat package

1.3 Absolute maximum ratings.

Supply voltage range	-0.5 V dc to +7.0 V dc
DC voltage applied to outputs in high-Z state	-0.5 V dc to +7.0 V dc
DC input voltage range	-0.5 V dc to +7.0 V dc <u>1/</u>
DC output current	20 mA
Maximum power dissipation <u>2/</u>	1.0 W
Lead temperature (soldering, 10 seconds)	+260°C
Thermal resistance, junction-to-case (Θ_{JC}):	See MIL-STD-1835
Junction temperature (T_J) <u>3/</u>	+150°C
Storage temperature range	-65°C to +150°C
Temperature under bias	-55°C to +125°C

1/ 1.5 V undershoots are allowed for 10 ns once per cycle.

2/ Must withstand the added P_D due to short circuit test; e.g., I_{OS} .

3/ Maximum junction temperature may be increased to +175°C during burn-in and steady-state life.

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1.4 Recommended operating conditions.

Supply voltage range (V_{CC})	+4.5 V dc to +5.5 V dc
Ground voltage (GND)	0 V dc
Input high voltage (V_{IH})	2.2 V dc minimum 4/
Input low voltage (V_{IL})	0.8 V dc maximum
Case operating temperature range (T_C)	-55°C to +125°C

2. APPLICABLE DOCUMENTS

2.1 Government specification, standards, and handbooks. The following specification, standards, and handbooks form a part of this drawing to the extent specified herein. Unless otherwise specified, the issues of these documents are those listed in the issue of the Department of Defense Index of Specifications and Standards (DoDISS) and supplement thereto, cited in the solicitation.

SPECIFICATION

MILITARY

MIL-PRF-38535 - Integrated Circuits Manufacturing, General Specification for.

STANDARD

MILITARY

MIL-STD-883 - Test Methods and Procedures for Microelectronics.
MIL-STD-973 - Configuration Management.
MIL-STD-1835 - Microcircuit Case Outlines.

HANDBOOKS

MILITARY

MIL-HDBK-103 - List of Standard Microcircuit Drawings (SMD's).
MIL-HDBK-780 - Standard Microcircuit Drawings.

(Unless otherwise indicated, copies of the specification, standards, and handbooks are available from the Standardization Document Order Desk, 700 Robbins Avenue, Building 4D, Philadelphia, PA 19111-5094.)

2.2 Order of precedence. In the event of a conflict between the text of this drawing and the references cited herein, the text of this drawing shall take precedence. Nothing in this document, however, supersedes applicable laws and regulations unless a specific exemption has been obtained.

3. REQUIREMENTS

3.1 Item requirements. The individual item requirements shall be in accordance with MIL-PRF-38535, appendix A for non-JAN class level B devices and as specified herein. Product built to this drawing that is produced by a Qualified Manufacturer Listing (QML) certified and qualified manufacturer or a manufacturer who has been granted transitional certification to MIL-PRF-38535 may be processed as QML product in accordance with the manufacturers approved program plan and qualifying activity approval in accordance with MIL-PRF-38535. This QML flow as documented in the Quality Management (QM) plan may make modifications to the requirements herein. These modifications shall not affect form, fit, or function of the device. These modifications shall not affect the PIN as described herein. A "Q" or "QML" certification mark in accordance with MIL-PRF-38535 is required to identify when the QML flow option is used.

3.2 Design, construction, and physical dimensions. The design, construction, and physical dimensions shall be as specified in MIL-PRF-38535, appendix A and herein.

3.2.1 Case outline(s). The case outline(s) shall be in accordance with 1.2.2 herein.

3.2.2 Terminal connections. The terminal connections shall be as specified on figure 1.

4/ V_{IH} is 2.2 V minimum for all input pins except XT, which is 3.5 V minimum.

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TABLE I. Electrical performance characteristics.

Test	Symbol	Conditions 1/ -55°C ≤ T _C ≤ +125°C 4.5 V ≤ V _{CC} ≤ 5.5 V unless otherwise specified	Group A subgroups	Device types	Limits		Unit
					Min	Max	
Output high voltage	V _{OH}	V _{CC} = 4.5 V, I _{OH} = -2.0 mA, V _{IN} = V _{IL} , V _{IH}	1, 2, 3	All	2.4		V
Output low voltage	V _{OL}	V _{CC} = 4.5 V, I _{OL} = 8.0 mA, V _{IN} = V _{IL} , V _{IH}	1, 2, 3	All		0.4	V
Input high voltage	V _{IH} 2/ 3/		1, 2, 3	All	2.2		V
Input low voltage	V _{IL} 2/		1, 2, 3	All	4/ -0.5	0.8	V
Input leakage current	I _{IX}	V _{IN} = 5.5 V to GND	1, 2, 3	All	-10	10	μA
Output leakage current	I _{OZ}	V _{CC} = 5.5 V, V _{OUT} = 5.5 V and GND	1, 2, 3	All	-10	10	μA
Operating supply current	I _{CC}	V _{CC} = 5.5 V, I _{OUT} = 0 mA f = 1/t _{BC} W, R, D ₀ - D ₈ pins are toggling between 0 V and 3 V FF, XO/HF = 0 mA Q ₀ - Q ₈ = 0 mA MR, FL/RT = 3.0 V	1, 2, 3	All		150	mA
Standby current	I _{SB1}	V _{CC} = 5.5 V, I _{OUT} = 0 mA All inputs = V _{IH} FF, XO/HF = 0 mA Q ₀ - Q ₈ = 0 mA	1, 2, 3	All		30	mA
Power down current	I _{SB2}	V _{CC} = 5.5 V, I _{OUT} = 0 mA All inputs = V _{CC} - 0.2 V FF, XO/HF = 0 mA Q ₀ - Q ₈ = 0 mA	1, 2, 3	All		25	mA
Input capacitance	C _{IN}	V _{IN} = 0 V, V _{CC} = 5.0 V T _A = +25°C, f = 1 MHz (See 4.3.1c)	4	All		8	pF
Output capacitance	C _{OUT}	V _O = 0 V, V _{CC} = 5.0 V T _A = +25°C, f = 1 MHz (See 4.3.1c)	4	All		12	pF

See footnotes at end of table.

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TABLE I. Electrical performance characteristics - Continued.

Test	Symbol	Conditions 1/ $-55^{\circ}\text{C} \leq T_C \leq +125^{\circ}\text{C}$ $4.5\text{ V} \leq V_{CC} \leq 5.5\text{ V}$ unless otherwise specified	Group A subgroups	Device types	Limits		Unit
					Min	Max	
Read cycle time	t_{RC}		9, 10, 11	01	100		ns
				02	80		
				03	65		
				04	50		
				05	40		
				06	30		
				07	35		
Access time	t_A		9, 10, 11	01		80	ns
				02		65	
				03		50	
				04		40	
				05		30	
				06		20	
				07		25	
Read recovery time	t_{RR}		9, 10, 11	01	20		ns
				02,03	15		
				04 - 07	10		
Read pulse width	t_{PR}		9, 10, 11	01	80		ns
				02	65		
				03	50		
				04	40		
				05	30		
				06	20		
				07	25		
Read low to low-Z	$\frac{5/6}{t_{LZR}}$		9, 10, 11	All	3		ns
Read high to data valid	t_{DVR}		9, 10, 11	01 - 06	3		ns
				07	5		

See footnotes at end of table.

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TABLE I. Electrical performance characteristics - Continued.

Test	Symbol	Conditions 1/ $-55^{\circ}\text{C} \leq T_C \leq +125^{\circ}\text{C}$ $4.5\text{ V} \leq V_{CC} \leq 5.5\text{ V}$ unless otherwise specified	Group A subgroups	Device types	Limits		Unit
					Min	Max	
Read high to high-Z	5/6/ t_{HZR}		9, 10, 11	01,02,03		30	ns
				04		25	
				05		20	
				06		15	
				07		18	
Write cycle time	t_{WC}		9, 10, 11	01	100		ns
				02	80		
				03	65		
				04	50		
				05	40		
				06	30		
				07	35		
Write pulse width	t_{PW}		9, 10, 11	01	80		ns
				02	65		
				03	50		
				04	40		
				05	30		
				06	20		
				07	25		
Write high to low-Z	5/6/ t_{HWZ}		9, 10, 11	01 - 04	10		ns
				05 - 07	5		
Write recovery time	t_{WR}		9, 10, 11	01	20		ns
				02,03	15		
				04 - 07	10		
Data setup time	t_{SD}		9, 10, 11	01	40		ns
				02,03	30		
				04	20		
				05	18		
				06	12		
				07	15		

See footnotes at end of table.

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TABLE I. Electrical performance characteristics - Continued.

Test	Symbol	Conditions 1/ -55°C ≤ T _C ≤ +125°C 4.5 V ≤ V _{CC} ≤ 5.5 V unless otherwise specified	Group A subgroups	Device types	Limits		Unit
					Min	Max	
Data hold time	t _{HD}		9, 10, 11	01,02	10		ns
				03	5		
				04 - 07	0		
Master reset cycle time	t _{MRSC}		9, 10, 11	01	100		ns
				02	80		
				03	65		
				04	50		
				05	40		
				06	30		
				07	35		
Master reset pulse width	t _{PMR}		9, 10, 11	01	80		ns
				02	65		
				03	50		
				04	40		
				05	30		
				06	20		
				07	25		
Master reset recovery time	t _{RMR}		9, 10, 11	01	20		ns
				02,03	15		
				04 - 07	10		
Read high to master reset high	t _{RPW}		9, 10, 11	01	80		ns
				02	65		
				03	50		
				04	40		
				05	30		
				06	20		
				07	25		

See footnotes at end of table.

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TABLE I. Electrical performance characteristics - Continued.

Test	Symbol	Conditions 1/ -55°C ≤ T _C ≤ +125°C 4.5 V ≤ V _{CC} ≤ 5.5 V unless otherwise specified	Group A subgroups	Device types	Limits		Unit
					Min	Max	
Write high to master reset high	t _{WPW}		9, 10, 11	01	80		ns
				02	65		
				03	50		
				04	40		
				05	30		
				06	20		
				07	25		
Retransmit cycle time	t _{RTC}		9, 10, 11	01	100		ns
				02	80		
				03	65		
				04	50		
				05	40		
				06	45		
				07	35		
Retransmit pulse width	t _{PRT}		9, 10, 11	01	80		ns
				02	65		
				03	50		
				04	40		
				05	30		
				06	35		
				07	25		
Retransmit recovery time	t _{RTR}		9, 10, 11	01	20		ns
				02,03	15		
				04 - 07	10		
Master reset to empty flag low	t _{EFL}		9, 10, 11	01		100	ns
				02		80	
				03		65	
				04		50	
				05		40	
				06		30	
				07		35	

See footnotes at end of table.

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TABLE I. Electrical performance characteristics - Continued.

Test	Symbol	Conditions 1/ $-55^{\circ}\text{C} \leq T_C \leq +125^{\circ}\text{C}$ $4.5\text{ V} \leq V_{CC} \leq 5.5\text{ V}$ unless otherwise specified	Group A subgroups	Device types	Limits		Unit
					Min	Max	
Master reset to half-full flag high	t_{HFH}		9, 10, 11	01		100	ns
				02		80	
				03		65	
				04		50	
				05		40	
				06		30	
				07		35	
Master reset to full flag high	t_{FFH}		9, 10, 11	01		100	ns
				02		80	
				03		65	
				04		50	
				05		40	
				06		30	
				07		35	
Read low to empty flag low	t_{REF}		9, 10, 11	01,02		60	ns
				03		45	
				04		35	
				05		30	
				06		28	
				07		25	
Read high to full flag high	t_{RFF}		9, 10, 11	01,02		60	ns
				03		45	
				04		35	
				05		30	
				06		28	
				07		25	
Write high to empty flag high	t_{WEF}		9, 10, 11	01,02		60	ns
				03		45	
				04		35	
				05		30	
				06		28	
				07		25	

See footnotes at end of table.

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TABLE I. Electrical performance characteristics - Continued.

Test	Symbol	Conditions 1/ $-55^{\circ}\text{C} \leq T_C \leq +125^{\circ}\text{C}$ $4.5\text{ V} \leq V_{CC} \leq 5.5\text{ V}$ unless otherwise specified	Group A subgroups	Device types	Limits		Unit
					Min	Max	
Write low to full flag low	t_{WFF}		9, 10, 11	01,02		60	ns
				03		45	
				04		35	
				05		30	
				06		28	
				07		25	
Write low to half-full flag low	t_{WHF}		9, 10, 11	01		100	ns
				02		80	
				03		65	
				04		50	
				05		40	
				06		30	
				07		25	
Read high to half-full flag high	t_{RHF}		9, 10, 11	01		100	ns
				02		80	
				03		65	
				04		50	
				05		40	
				06		30	
				07		25	
Effective read from write high	$\frac{4}{t_{RAE}}$		9, 10, 11	01		60	ns
				02		60	
				03		45	
				04		35	
				05		30	
				06		20	
				07		25	

See footnotes at end of table.

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TABLE I. Electrical performance characteristics - Continued.

Test	Symbol	Conditions 1/ -55°C ≤ T _C ≤ +125°C 4.5 V ≤ V _{CC} ≤ 5.5 V unless otherwise specified	Group A subgroups	Device types	Limits		Unit
					Min	Max	
Effective read pulse width after empty flag high	t _{RPE}		9, 10, 11	01	80		ns
				02	65		
				03	50		
				04	40		
				05	30		
				06	20		
				07	25		
Effective write from read high	4/ t _{WAF}		9, 10, 11	01		60	ns
				02		60	
				03		45	
				04		35	
				05		30	
				06		20	
				07		25	
Effective write pulse width after full flag high	t _{WPF}		9, 10, 11	01	80		ns
				02	65		
				03	50		
				04	40		
				05	30		
				06	20		
				07	25		
Expansion out low delay from clock	t _{XOL} 5/		9, 10, 11	01		80	ns
				02		65	
				03		50	
				04		40	
				05		30	
				06		20	
				07		25	

See footnotes at end of table.

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TABLE I. Electrical performance characteristics - Continued.

Test	Symbol	Conditions 1/ $-55^{\circ}\text{C} \leq T_C \leq +125^{\circ}\text{C}$ $4.5\text{ V} \leq V_{CC} \leq 5.5\text{ V}$ unless otherwise specified	Group A subgroups	Device types	Limits		Unit
					Min	Max	
Expansion out high delay from clock	t_{XOH} 5/		9, 10, 11	01		80	ns
				02		65	
				03		50	
				04		40	
				05		30	
				06		20	
				07		25	

1/ AC tests are performed with input rise and fall times of 5 ns or less, timing reference levels of 1.5 V, input pulse levels of 0 to 3.0 V, and the output load circuit, unless otherwise specified. See figures 4 and 5.

2/ These are absolute values with respect to device ground and all overshoots due to system or tester noise are included.

3/ V_{IH} is 2.2 V minimum for all input pins except $\overline{XI}$, which is 3.5 V minimum.

4/ May not be tested, but shall be guaranteed to the limits specified in table I herein.

5/ Tested initially and after any design or process changes that affect that parameter, and therefore shall be guaranteed to the limits specified in table I.

6/ Transition is measured at steady-state high level -500 mV or steady-state low level +500 mV on the output from the 1.5 V level on the input.

3.2.3 Truth tables. The truth tables shall be as specified on figure 2.

3.2.4 Die overcoat. Polyimide and silicone coatings are allowable as an overcoat on the die for alpha particle protection provided that each coated microcircuit inspection lot (reference appendix A of MIL-PRF-38535, 30.1.3.8) shall be subjected to and pass the internal moisture content test, (test method 1018 of MIL-STD-883), the frequency of the internal water vapor testing may not be decreased unless approved by the preparing activity.

3.3 Electrical performance characteristics. Unless otherwise specified herein, the electrical performance characteristics are as specified in table I and shall apply over the full case operating temperature range.

3.4 Electrical test requirements. The electrical test requirements shall be the subgroups specified in table II. The electrical tests for each subgroup are described in table I.

3.5 Marking. Marking shall be in accordance with MIL-PRF-38535, appendix A. The part shall be marked with the PIN listed in 1.2 herein. In addition, the manufacturer's PIN may also be marked as listed in MIL-HDBK-103 (see 6.6 herein). For packages where marking of the entire SMD PIN number is not feasible due to space limitations, the manufacturer has the option of not marking the "5962-" on the device.

3.6 Certificate of compliance. A certificate of compliance shall be required from a manufacturer in order to be listed as an approved source of supply in MIL-HDBK-103 (see 6.6 herein). The certificate of compliance submitted to DSCC-VA prior to listing as an approved source of supply shall affirm that the manufacturer's product meets the requirements of MIL-PRF-38535, appendix A and the requirements herein.

3.7 Certificate of conformance. A certificate of conformance as required in MIL-PRF-38535, appendix A shall be provided with each lot of microcircuits delivered to this drawing.

3.8 Notification of change. Notification of change to DSCC-VA shall be required in accordance with MIL-PRF-38535, appendix A.

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Device types	01-07	
Case outlines	X, Y, and U	Z
Terminal number	Terminal symbol	Terminal symbol
1	$\overline{W}$	NC
2	D ₈	$\overline{W}$
3	D ₃	D ₈
4	D ₂	D ₃
5	D ₁	D ₂
6	D ₀	D ₁
7	$\overline{XI}$	D ₀
8	$\overline{FF}$	$\overline{XI}$
9	Q ₀	$\overline{FF}$
10	Q ₁	Q ₀
11	Q ₂	Q ₁
12	Q ₃	NC
13	Q ₈	Q ₂
14	GND	Q ₃
15	R	Q ₈
16	Q ₄	GND
17	Q ₅	NC
18	Q ₆	R
19	Q ₇	Q ₄
20	$\overline{XO/HF}$	Q ₅
21	$\overline{EE}$	Q ₆
22	MR	Q ₇
23	$\overline{FL/RT}$	$\overline{XO/HF}$
24	D ₇	$\overline{EE}$
25	D ₆	MR
26	D ₅	$\overline{FL/RT}$
27	D ₄	NC
28	V _{CC}	D ₇
29	---	D ₆
30	---	D ₅
31	---	D ₄
32	---	V _{CC}

NC = no connection

FIGURE 1. Terminal connections.

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Reset and retransmit
Single device configuration/width expansion mode

Mode	Inputs			Internal status		Outputs		
	$\overline{MR}$	$\overline{RT}$	$\overline{XI}$	Read pointer	Write pointer	$\overline{EF}$	$\overline{FF}$	$\overline{HF}$
Reset	0	X	0	Location zero	Location zero	0	1	1
Retransmit	1	0	0	Location zero	Unchanged	X	X	X
Read/write	1	1	0	Increment	Increment (see note 2)	X	X	X

Reset and first load truth table
Depth expansion/compound expansion mode

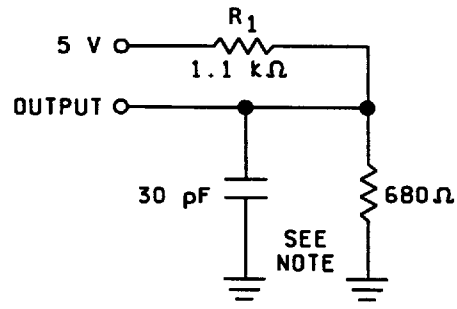
Mode	Inputs		Internal status			Outputs	
	$\overline{MR}$	$\overline{FL}$	$\overline{XI}$	Read pointer	Write pointer	$\overline{EF}$	$\overline{FF}$
Reset first device	0	0	(see note 3)	Location zero	Location zero	0	1
Reset all other devices	0	1	(see note 3)	Location zero	Location zero	0	X
Read/write	1	X	(see note 3)	X	X	X	X

NOTES:

1. $\overline{MR}$ = Reset input, $\overline{FL}/\overline{RT}$ = First load/retransmit $\overline{EF}$ = Empty flag output, $\overline{FF}$ = Full flag output, $\overline{XI}$ = Expansion input, and $\overline{HF}$ = Half-full flag output
2. Pointer will increment if flag is high.
3. $\overline{XI}$ is connected to $\overline{XO}$ of previous device.

FIGURE 2. Truth tables.

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NOTE: 30 pF includes scope and jig capacitance.

FIGURE 3. Output load circuit.

Asynchronous read and write diagram

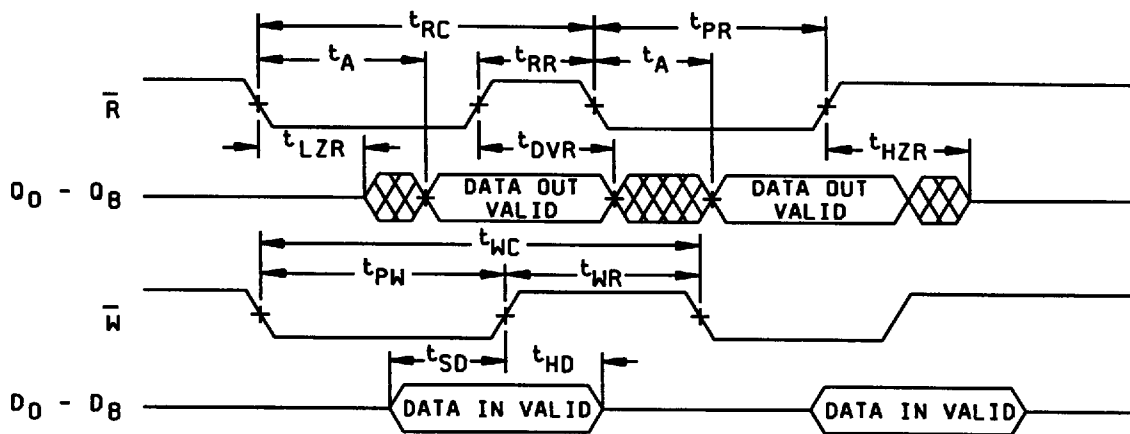


FIGURE 4. Timing waveforms.

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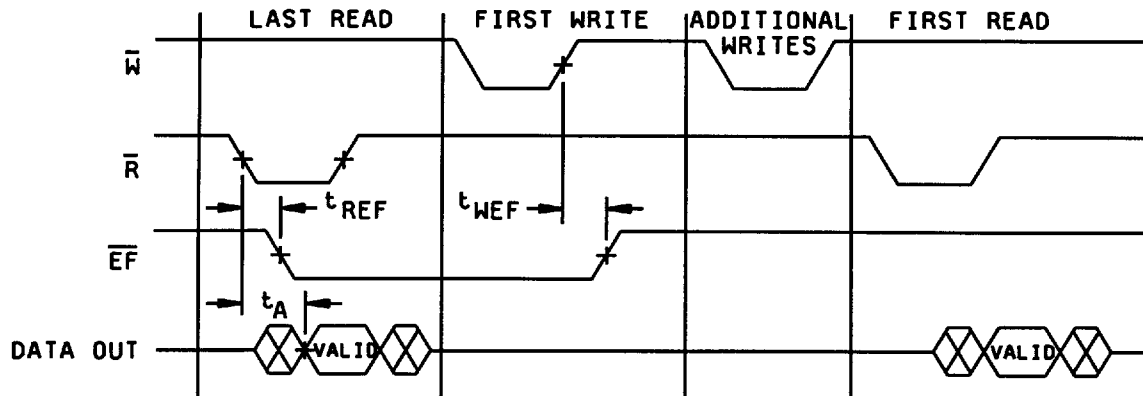
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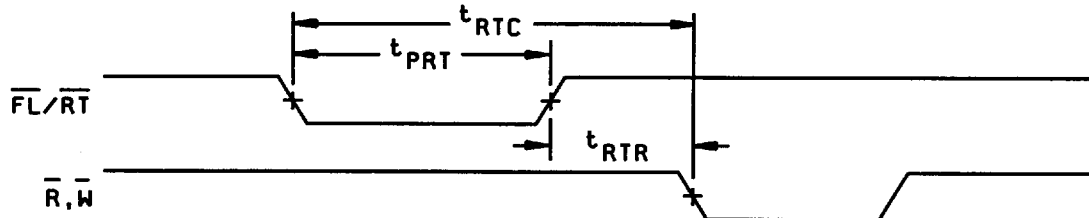
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Last read to first write empty flag timing diagram



Retransmit timing diagram

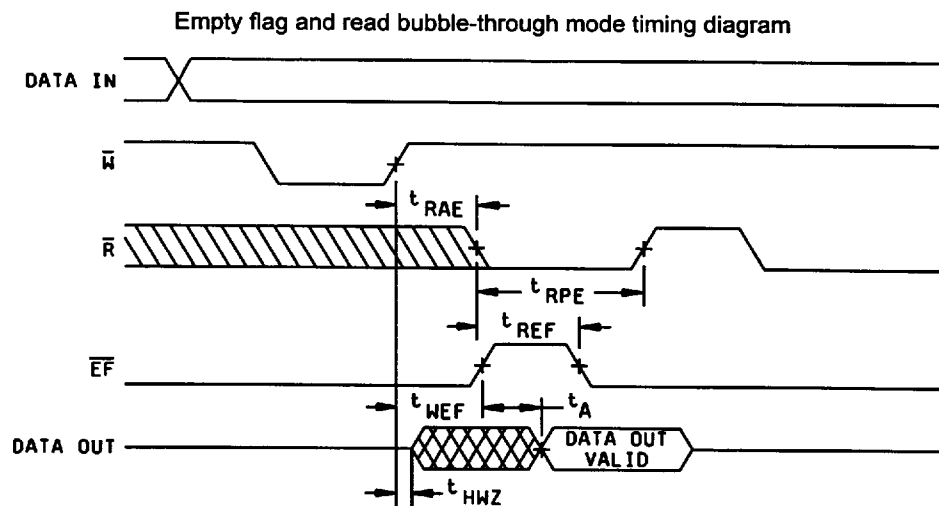


NOTES:

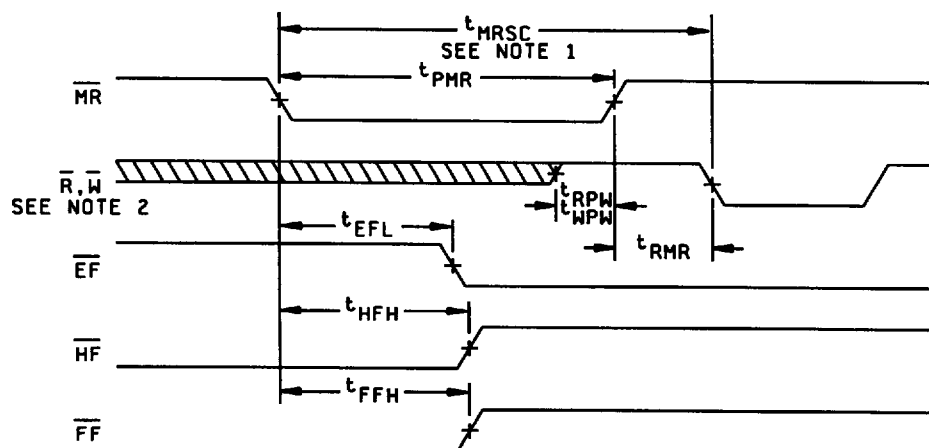
1. $t_{RTC} = t_{RT} + t_{RTR}$
2. $\overline{EF}$, $\overline{HF}$ and $\overline{FF}$ may change state during retransmit as a result of the offset of the read and write pointers, but flags will be valid at t_{RTC} .

FIGURE 4. Timing waveforms - Continued.

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Master reset timing diagram



NOTES:

1. $t_{MRSC} = t_{PMR} + t_{RMR}$
2. $\overline{W}$ and $\overline{R} = V_{IH}$ around the rising edge of $\overline{MR}$.

FIGURE 4. Timing waveforms - Continued.

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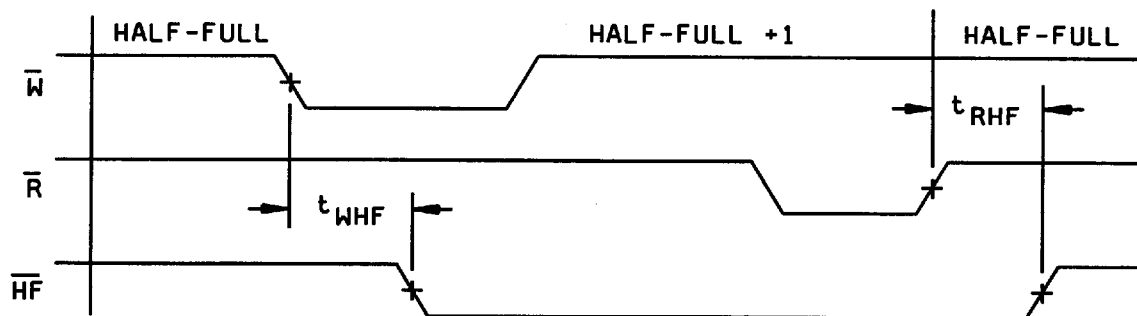
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Half-full flag timing diagram



Last write to first read full flag timing diagram

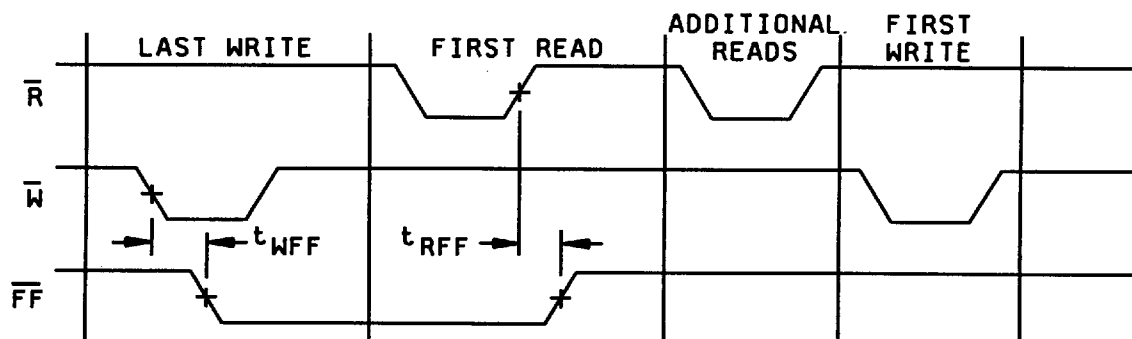


FIGURE 4. Timing waveforms - Continued.

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Full flag and write bubble-through mode timing diagram

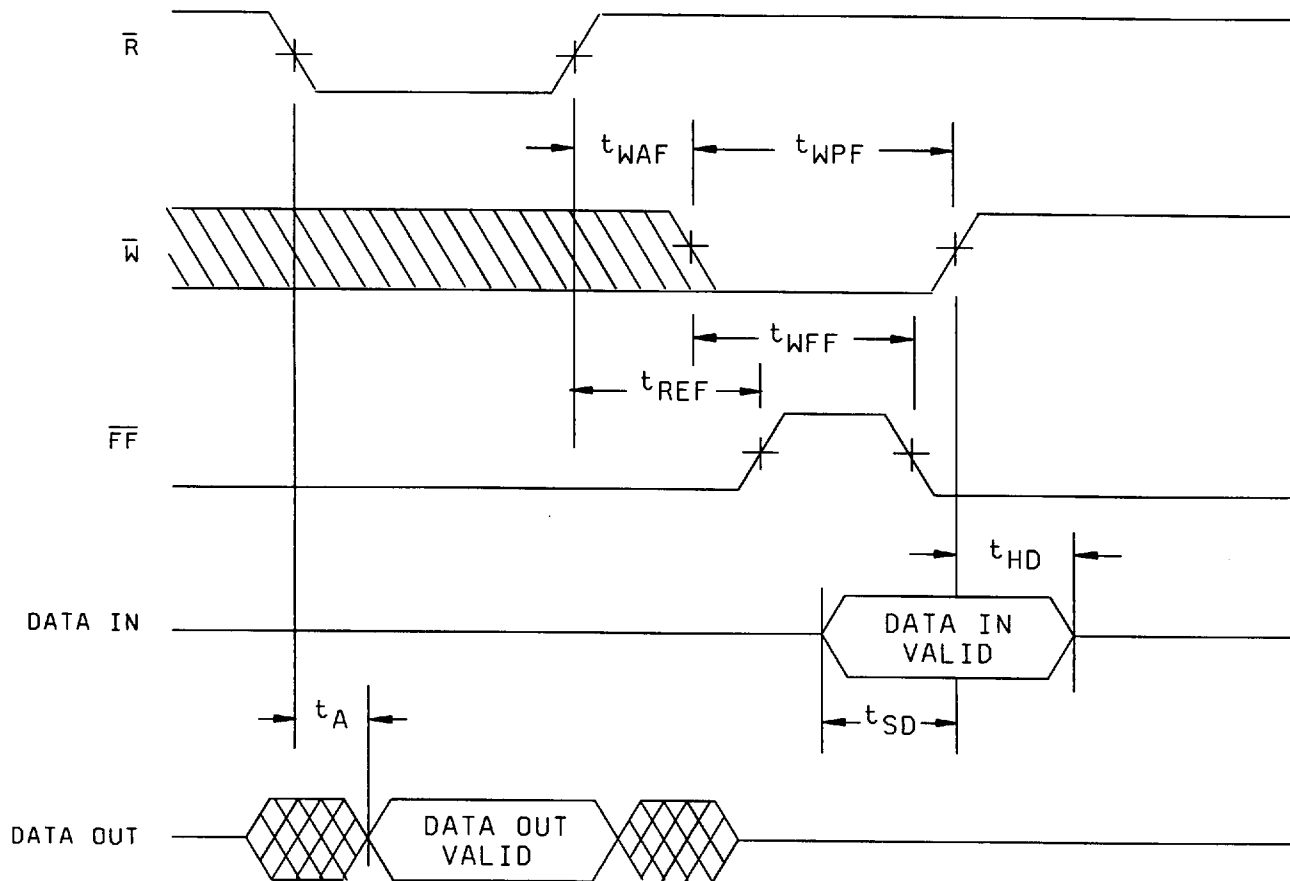


FIGURE 4. Timing waveforms - Continued.

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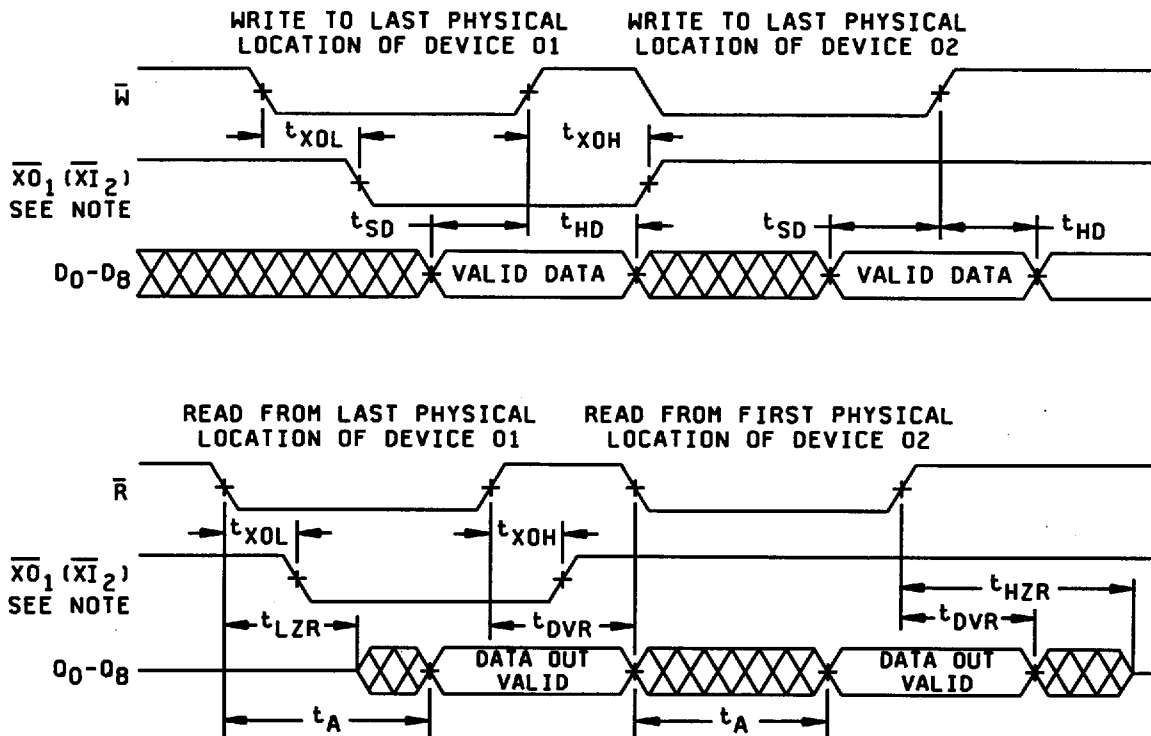
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Expansion timing diagrams



NOTE: Expansion out of device 1 ($\bar{XO}_1$) is connected to expansion in of device 2 ($\bar{XI}_2$).

FIGURE 4. Timing waveforms - Continued.

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3.9 Verification and review. DSCC, DSCC's agent, and the acquiring activity retain the option to review the manufacturer's facility and applicable required documentation. Offshore documentation shall be made available onshore at the option of the reviewer.

4. QUALITY ASSURANCE PROVISIONS

4.1 Sampling and inspection. Sampling and inspection procedures shall be in accordance with MIL-PRF-38535, appendix A.

4.2 Screening. Screening shall be in accordance with method 5004 of MIL-STD-883, and shall be conducted on all devices prior to quality conformance inspection. The following additional criteria shall apply:

a. Burn-in test, method 1015 of MIL-STD-883.

(1) Test condition C or D. The test circuit shall be maintained by the manufacturer under document revision level control and shall be made available to the preparing or acquiring activity upon request. The test circuit shall specify the inputs, outputs, biases, and power dissipation, as applicable, in accordance with the intent specified in test method 1015 of MIL-STD-883.

(2) $T_A = +125^\circ\text{C}$, minimum.

b. Interim and final electrical test parameters shall be as specified in table II herein, except interim electrical parameter tests prior to burn-in are optional at the discretion of the manufacturer.

4.3 Quality conformance inspection. Quality conformance inspection shall be in accordance with method 5005 of MIL-STD-883 including groups A, B, C, and D inspections. The following additional criteria shall apply.

4.3.1 Group A inspection.

a. Tests shall be as specified in table II herein.

b. Subgroups 5 and 6 in table I, method 5005 of MIL-STD-883 shall be omitted.

c. Subgroup 4 (C_{IN} and C_{OUT} measurement) shall be measured only for the initial test and after process or design changes which may affect input capacitance.

d. Subgroups 7 and 8 shall include verification of the truth table.

4.3.2 Groups C and D inspections.

a. End-point electrical parameters shall be as specified in table II herein.

b. Steady-state life test conditions, method 1005 of MIL-STD-883.

(1) Test condition C or D. The test circuit shall be maintained by the manufacturer under document revision level control and shall be made available to the preparing or acquiring activity upon request. The test circuit shall specify the inputs, outputs, biases, and power dissipation, as applicable, in accordance with the intent specified in test method 1005 of MIL-STD-883.

(2) $T_A = +125^\circ\text{C}$, minimum.

(3) Test duration: 1,000 hours, except as permitted by method 1005 of MIL-STD-883.

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TABLE II. Electrical test requirements.

MIL-STD-883 test requirements	Subgroups (per method 5005, table I)
Interim electrical parameters (method 5004)	---
Final electrical test parameters (method 5004)	1*,2,3,7*,8, 9,10,11
Group A test requirements (method 5005)	1,2,3,4**,7,8, 9,10,11
Groups C and D end-point electrical parameters (method 5005)	2,3,7,8

* PDA applies to subgroups 1 and 7.

** Indicates subgroup 4 will only be performed during initial qualification and after any design or process changes that may affect capacitance (see 4.3.1c).

5. PACKAGING

5.1 Packaging requirements. The requirements for packaging shall be in accordance with MIL-PRF-38535, appendix A.

6. NOTES

6.1 Intended use. Microcircuits conforming to this drawing are intended for use for Government microcircuit applications (original equipment), design applications, and logistics purposes.

6.2 Replaceability. Microcircuits covered by this drawing will replace the same generic device covered by a contractor-prepared specification or drawing.

6.3 Configuration control of SMD's. All proposed changes to existing SMD's will be coordinated with the users of record for the individual documents. This coordination will be accomplished in accordance with MIL-STD-973 using DD Form 1692, Engineering Change Proposal (Short Form).

6.4 Record of users. Military and industrial users shall inform Defense Supply Center Columbus when a system application requires configuration control and the applicable SMD. DSCC will maintain a record of users and this list will be used for coordination and distribution of changes to the drawings. Users of drawings covering microelectronics devices (FSC 5962) should contact DSCC-VA, telephone (614) 692-0525.

6.5 Comments. Comments on this drawing should be directed to DSCC-VA, Columbus, Ohio 43216-5000, or telephone (614) 692-0674.

6.6 Approved sources of supply. Approved sources of supply are listed in MIL-HDBK-103. The vendors listed in MIL-HDBK-103 have agreed to this drawing and a certificate of compliance (see 3.6 herein) has been submitted to and accepted by DSCC-VA.

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STANDARD MICROCIRCUIT DRAWING SOURCE APPROVAL BULLETIN

DATE: 97-02-25

Approved sources of supply for SMD 5962-88669 are listed below for immediate acquisition only and shall be added to MIL-HDBK-103 during the next revision. MIL-HDBK-103 will be revised to include the addition or deletion of sources. The vendors listed below have agreed to this drawing and a certificate of compliance has been submitted to and accepted by DSCC-VA. This bulletin is superseded by the next dated revision of MIL-HDBK-103.

Standard microcircuit drawing PIN	Vendor CAGE number	Vendor similar PIN <u>1</u> /
5962-8866901XX	61772 0HGZ7	IDT7203S80DB MM1I-67203L-50/883
5962-8866901ZX	0HGZ7 61772	MM4J-67203L-50/883 IDT7203S80LB
5962-8866901UX	61772	IDT7203S80EB
5962-8866902XX	61772 0HGZ7 65786	IDT7203S65DB MM1I-67203L-50/883 CY7C428-65DMB
5962-8866902YX	65786	CY7C429-65DMB
5962-8866902ZX	61772 0HGZ7 65786	IDT7203S65LB MM4J-67203L-50/883 CY7C429-65LMB
5962-8866902UX	61772 2/	IDT7203S65EB CY7C429-65KMB
5962-8866903XX	2/ 2/ 61772 0HGZ7 65786	AM7203A-50/BXA MT52C9020CW-50883C IDT7203S50DB MM1I-67203L-50/883 CY7C428-50DMB
5962-8866903YX	2/ 65786	MT52C9020C-50883C CY7C429-50DMB
5962-8866903ZX	2/ 2/ 61772 0HGZ7 65787	AM7203A-50/BUA MT52C9020EC-50883C IDT7203S50LB MM4J-67203L-50/883 CY7C429-50LMB
5962-8866903UX	2/ 61772 2/	MT52C9020F-50883C IDT7203S50EB CY7C429-50KMB
5962-8866904XX	2/ 61772 0HGZ7 65786	MT52C9020CW-40883C IDT7203S40DB MM1I-67203L-40/883 CY7C428-40DMB
5962-8866904YX	2/ 65786	MT52C9020C-40883C CY7C429-40DMB
5962-8866904ZX	2/ 61772 0HGZ7 65786	MT52C9020EC-40883C IDT7203S40LB MM4J-67203L-40/883 CY7C429-40LMB
5962-8866904UX	2/ 61772 2/	MT52C9020F-40883C IDT7203S40EB CY7C429-40KMB
5962-8866905XX	2/ 2/ 61772 0HGZ7 65786	AM7203A-30/BXA MT52C9020CW-30883C IDT7203S30DB MM1I-67203L-30/883 CY7C428-30DMB
5962-8866905YX	2/	MT52C9020C-30883C
5962-8866905YX	65786	CY7C429-30DMB

See footnote at end of list.

Standard microcircuit drawing PIN	Vendor CAGE number	Vendor similar PIN 1/
5962-8866905ZX	2/ 2/ 61772 0HGZ7 65786	AM7203A-30/BUA MT52C9020EC-30883C IDT7203S30LB MM4J-67203L-30/883 CY7C429-30LMB
5962-8866905UX	2/ 2/ 2/	MT52C9020F-30883C IDT7203S30XEB CY7C429-30KMB
5962-8866906XX	2/ 2/ 61772	AM7203A-20/BXA MT52C9020CW-20883C IDT7203S20DB
5962-8866906YX	61772 2/	IDT7203S20TDB MT52C9020C-20883C
5962-8866906ZX	2/ 2/ 61772	AM7203A-20/BUA MT52C9020EC-20883C IDT7203S20LB
5962-8866906UX	2/ 2/ 2/	AM7203A-20/BYA MT52C9020F-20883C IDT7203S20XEB
5962-8866907XX	65786	CY7C428-25DMB
5962-8866907YX	65786	CY7C429-25DMB
5962-8866907ZX	65786	CY7C429-25LMB

- 1/ Caution. Do not use this number for item acquisition. Items acquired to this number may not satisfy the performance requirements of this drawing.
- 2/ No longer available from an approved source.

<u>Vendor CAGE number</u>	<u>Vendor name and address</u>
61772	Integrated Device Technology, Incorporated 3236 Scott Boulevard Santa Clara, CA 95054
65786	Cypress Semiconductor 3901 North First Street San Jose, CA 95134
0HGZ7	Matra-Harris Semiconductor 2895 Northwestern Parkway Santa Clara, CA 94086

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