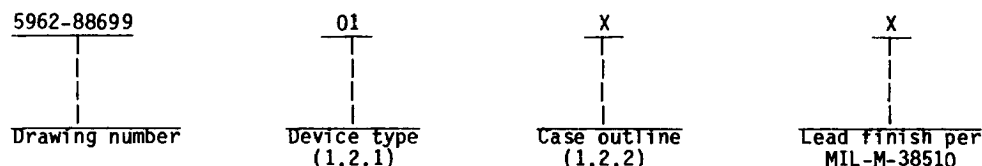


**DISTRIBUTION STATEMENT A.** Approved for public release; distribution is unlimited.

## 1. SCOPE

1.1 Scope. This drawing describes device requirements for class B microcircuits in accordance with 1.2.1 of MIL-STD-883, "Provisions for the use of MIL-STD-883 in conjunction with compliant non-JAN devices".

1.2 Part number. The complete part number shall be as shown in the following example:



1.2.1 Device type. The device type shall identify the circuit function as follows:

| Device type | Generic number | Circuit function  |
|-------------|----------------|---|
| 01          | HI-516         | 16-channel/differential 8-channel CMOS analog multiplexer |

1.2.2 Case outlines. The case outlines shall be as designated in appendix C of MIL-M-38510, and as follows:

| Outline letter | Case outline  |
|----------------|---|
| X              | D-10 (28-lead, 1.490" x .610" x .232"), dual-in-line package          |
| 3              | C-4 (28-terminal, .460" x .460" x .100"), square chip carrier package |

1.3 Absolute maximum ratings.

|  |                             |
|--|-----------------------------|
| Voltage between +V <sub>CC</sub> and -V <sub>CC</sub>            | 33 V dc                     |
| Voltage between +V <sub>CC</sub> and ground                      | 16.5 V dc                   |
| Voltage between -V <sub>CC</sub> and ground                      | 16.5 V dc                   |
| Analog input voltage:  |                             |
| +V <sub>S</sub>  | +V <sub>CC</sub> + 2.0 V dc |
| -V <sub>S</sub>  | -V <sub>CC</sub> - 2.0 V dc |
| Digital input voltage, TTL (V <sub>DD</sub> /LLS = GND or open): |                             |
| +V <sub>A</sub>  | +6.0 V dc                   |
| -V <sub>A</sub>  | -6.0 V dc                   |
| +A <sub>3</sub> /SDS   | +V <sub>CC</sub> + 2.0 V dc |
| -A <sub>3</sub> /SDS   | -V <sub>CC</sub> - 2.0 V dc |
| Digital input voltage, CMOS (V <sub>DD</sub> /LLS = +15 V):      |                             |
| +V <sub>A</sub>  | +V <sub>CC</sub> + 2.0 V dc |
| -V <sub>A</sub>  | -2.0 V dc                   |
| Storage temperature range  | -65°C to +150°C             |
| Maximum power dissipation (P <sub>D</sub> ):                     |                             |
| Case X   | 2.0 W 1/                    |
| Case 3   | 1.23 W 2/                   |
| Lead temperature (soldering, 10 seconds)                         | +275°C                      |
| Thermal resistance, junction-to-case (θ <sub>JC</sub> ):         |                             |
| Cases X and 3  | See MIL-M-38510, appendix C |
| Thermal resistance, junction-to-ambient (θ <sub>JA</sub> ):      |                             |
| Case X   | 50°C/W                      |
| Case 3   | 81°C/W                      |
| Junction temperature (T <sub>J</sub> )                           | +175°C                      |

1/ Derate linearly above T<sub>A</sub> = +75°C at 20.0 mW/°C.

2/ Derate linearly above T<sub>A</sub> = +75°C at 12.3 mW/°C.

|   |                  |                |            |
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#### 1.4 Recommended operating conditions.

|   |           |   |
|---|-----------|---|
| Supply voltage ( $\pm V_{CC}$ )               | - - - - - | $\pm 15$ V dc                               |
| Analog input voltage ( $V_S$ )                | - - - - - | $\pm V_{CC}$                                |
| Input logic low voltage range ( $V_{AL}$ )    | - - - - - | 0 V dc to 0.8 V dc                          |
| Input logic high voltage range ( $V_{AH}$ )   | - - - - - | 2.4 V dc to $+V_{CC}$                       |
| Ambient operating temperature range ( $T_A$ ) | - - - - - | $-55^\circ\text{C}$ to $+125^\circ\text{C}$ |

#### 2. APPLICABLE DOCUMENTS

2.1 Government specification and standard. Unless otherwise specified, the following specification and standard, of the issue listed in that issue of the Department of Defense Index of Specifications and Standards specified in the solicitation, form a part of this drawing to the extent specified herein.

##### SPECIFICATION

###### MILITARY

MIL-M-38510 - Microcircuits, General Specification for.

##### STANDARD

###### MILITARY

MIL-STD-883 - Test Methods and Procedures for Microelectronics.

(Copies of the specification and standard required by manufacturers in connection with specific acquisition functions should be obtained from the contracting activity or as directed by the contracting activity.)

2.2 Order of precedence. In the event of a conflict between the text of this drawing and the references cited herein, the text of this drawing shall take precedence.

#### 3. REQUIREMENTS

3.1 Item requirements. The individual item requirements shall be in accordance with 1.2.1 of MIL-STD-883, "Provisions for the use of MIL-STD-883 in conjunction with compliant non-JAN devices" and as specified herein.

3.2 Design, construction, and physical dimensions. The design, construction, and physical dimensions shall be as specified in MIL-M-38510 and herein.

3.2.1 Terminal connections. The terminal connections shall be as specified on figure 1.

3.2.2 Truth table. The truth table shall be as specified on figure 2.

3.2.3 Functional diagram. The functional diagram shall be as specified on figure 3.

3.2.4 Case outlines. The case outlines shall be in accordance with 1.2.2 herein.

3.3 Electrical performance characteristics. Unless otherwise specified, the electrical performance characteristics are as specified in table I and apply over the full ambient operating temperature range.

3.4 Marking. Marking shall be in accordance with MIL-STD-883 (see 3.1 herein). The part shall be marked with the part number listed in 1.2 herein. In addition, the manufacturer's part number may also be marked as listed in 6.4 herein.

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TABLE I. Electrical performance characteristics.

| Test  | Symbol               | Conditions<br>$-55^{\circ}\text{C} \leq T_A \leq +125^{\circ}\text{C}$ 1/   | Group A<br>subgroups | Limits |      | Unit          |
|---|----------------------|---|----------------------|--------|------|---------------|
|   |                      |   |                      | Min    | Max  |               |
| Input leakage current   | $I_{IH}$             | Measure inputs sequentially,<br>All unused inputs = GND   | 1, 2, 3              | -1.0   | 1.0  | $\mu\text{A}$ |
|   | $I_{IL}$             | Measure inputs sequentially,<br>All unused inputs = +5.0 V  | 1, 2, 3              | -25    | 25   | $\mu\text{A}$ |
| Leakage current into<br>the source terminal<br>of an "OFF" switch | $+I_{S(\text{OFF})}$ | $V_S = +10\text{ V}$ , $V_D = -10\text{ V}$ ,<br>$V_{EN} = 0.8\text{ V}$ ,<br>All unused inputs = -10 V                                   | 1, 2, 3              | -50    | +50  | nA            |
|   | $-I_{S(\text{OFF})}$ | $V_S = -10\text{ V}$ , $V_D = +10\text{ V}$ ,<br>$V_{EN} = 0.8\text{ V}$ ,<br>All unused inputs = +10 V                                   | 1, 2, 3              | -50    | +50  | nA            |
| Leakage current into<br>the drain terminal<br>of an "OFF" switch  | $+I_{D(\text{OFF})}$ | $V_D = +10\text{ V}$ , $V_{EN} = 0.8\text{ V}$ ,<br>$V_S = -10\text{ V}$ ,<br>All unused inputs = -10 V                                   | 1, 2, 3              | -100   | +100 | nA            |
|   | $-I_{D(\text{OFF})}$ | $V_D = -10\text{ V}$ , $V_{EN} = 0.8\text{ V}$ ,<br>$V_S = +10\text{ V}$ ,<br>All unused inputs = +10 V                                   | 1, 2, 3              | -100   | +100 | nA            |
| Leakage current from<br>an "ON" driver into<br>the switch (drain) | $+I_{D(\text{ON})}$  | $V_S = V_D = +10\text{ V}$ ,<br>All unused inputs = -10 V   | 1, 2, 3              | -100   | +100 | nA            |
|   | $-I_{D(\text{ON})}$  | $V_S = V_D = -10\text{ V}$ ,<br>All unused inputs = +10 V   | 1, 2, 3              | -100   | +100 | nA            |
| Positive supply current   | $+I_{CC}$            | $V_S = 0\text{ V}$ , $V_D = \text{open}$ ,<br>$V_{EN} = 2.4\text{ V}$ , sequence all<br>address combinations,<br>record highest $+I_{CC}$ | 1, 2, 3              |        | +25  | mA            |

See footnotes at end of table.

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TABLE I. Electrical performance characteristics - Continued.

| Test                               | Symbol                | Conditions<br>$-55^{\circ}\text{C} \leq T_A \leq +125^{\circ}\text{C}$ 1/   | Group A<br>subgroups | Limits |      | Unit     |
|------------------------------------|-----------------------|---|----------------------|--------|------|----------|
|                                    |                       |   |                      | Min    | Max  |          |
| Negative supply current            | $-I_{CC}$             | $V_S = 0\text{ V}$ , $V_D = \text{open}$ ,<br>$V_{EN} = 2.4\text{ V}$ , sequence all<br>address combinations,<br>record highest $-I_{CC}$ | 1, 2, 3              | -25    |      | mA       |
| Standby positive supply<br>current | $+I_{SBY}$            | $V_A = 0.8\text{ V}$ , $V_{EN} = 0.8\text{ V}$ ,<br>$V_S = 0\text{ V}$ , $V_D = \text{open}$  | 1, 2, 3              |        | +25  | mA       |
| Standby negative supply<br>current | $-I_{SBY}$            |   | 1, 2, 3              | -25    |      | mA       |
| Switch "ON" resistance             | $+R_{DS1}$            | $V_S = +10\text{ V}$ , $I_D = -100\text{ }\mu\text{A}$  | 1                    |        | 750  | $\Omega$ |
|                                    |                       |   | 2, 3                 |        | 1000 | $\Omega$ |
|                                    | $-R_{DS1}$            | $V_S = -10\text{ V}$ , $I_D = +100\text{ }\mu\text{A}$  | 1                    |        | 750  | $\Omega$ |
|                                    |                       |   | 2, 3                 |        | 1000 | $\Omega$ |
| Logic level voltage                | $V_{AL}(\text{TTL})$  | $V_{DD}/\text{LLS} = \text{GND}$  | 1, 2, 3              |        | 0.8  | V        |
|                                    | $V_{AH}(\text{TTL})$  |   | 1, 2, 3              | 2.4    |      | V        |
|                                    | $V_{AL}(\text{CMOS})$ | $V_{DD}/\text{LLS} = +15\text{ V}$  | 1, 2, 3              |        | 4.5  | V        |
|                                    | $V_{AH}(\text{CMOS})$ |   | 1, 2, 3              | 10.5   |      | V        |

See footnotes at end of table.

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TABLE I. Electrical performance characteristics - Continued.

| Test                                  | Symbol        | Conditions<br>$-55^{\circ}\text{C} \leq T_A \leq +125^{\circ}\text{C}$ 1/  | Group A<br>subgroups | Limits |     | Unit |
|---------------------------------------|---------------|--|----------------------|--------|-----|------|
|                                       |               |  |                      | Min    | Max |      |
| Address input capacitance             | $C_A$         | $+V_{CC} = -V_{CC} = 0\text{ V}$ , $f = 1.0\text{ MHz}$<br>$T_A = +25^{\circ}\text{C}$   | 4                    |        | 10  | pF   |
| Output switch capacitance             | $C_{OS}$      | See 4.3.1c   | 4                    |        | 25  | pF   |
| Input switch capacitance              | $C_{IS}$      |  | 4                    |        | 10  | pF   |
| Charge transfer error 2/              | $V_{CTE}$     | $V_S = \text{GND}$ , $V_{EN} = 0\text{ to }5.0\text{ V}$ ,<br>$C_L = 100\text{ pF}$ , $f = 500\text{ kHz}$<br>$T_A = +25^{\circ}\text{C}$                          | 4                    |        | 20  | mV   |
| Off channel isolation 2/              | $V_{ISO}$     | $V_{EN} = 0.8\text{ V}$ , $R_L = 1.0\text{ k}\Omega$ ,<br>$C_L = 40\text{ pF}$ , $V_S = 3.0\text{ V rms}$ ,<br>$f = 500\text{ kHz}$<br>$T_A = +25^{\circ}\text{C}$ | 4                    | -55    |     | dB   |
| Break-before-make time delay          | $t_d$         | $R_L = 800\Omega$ , $C_L = 12.5\text{ pF}$ ,<br>See figure 4   | 9                    | 10     |     | ns   |
|                                       |               |  | 10                   | 2.0    |     | ns   |
|                                       |               |  | 11 2/                | 2.0    |     | ns   |
| Propagation delay time, enable to I/O | $t_{ON(EN)}$  |  | 9                    |        | 175 | ns   |
|                                       |               |  | 10, 11               |        | 225 | ns   |
|                                       | $t_{OFF(EN)}$ |  | 9                    |        | 175 | ns   |
|                                       |               |  | 10, 11               |        | 225 | ns   |

See footnotes at end of table.

|   |                  |                |            |
|---|------------------|----------------|------------|
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TABLE I. Electrical performance characteristics - Continued.

| Test  | Symbol         | Conditions<br>-55°C ≤ T <sub>A</sub> ≤ +125°C 1/                  | Group A<br>subgroups | Limits |     | Unit |
|---|----------------|---|----------------------|--------|-----|------|
|   |                |   |                      | Min    | Max |      |
| Propagation delay time,<br>address inputs to I/O<br>channel | t <sub>A</sub> | R <sub>L</sub> = 10 MΩ, C <sub>L</sub> = 12.5 pF,<br>See figure 4 | 9                    |        | 175 | ns   |
|   |                |   | 10, 11               |        | 225 | ns   |
| Functional test   |                | See 4.3.1d  | 7, 8                 |        |     |      |

1/ +V<sub>CC</sub> = +15 V, -V<sub>CC</sub> = -15 V, V<sub>EN</sub> = 2.4 V, V<sub>DD</sub>/LLS = GND, V<sub>AH</sub> = 2.4 V and V<sub>AL</sub> = 0.8 V, unless otherwise specified.

2/ Guaranteed, but not tested to the limits specified in table I.

3.5 Certificate of compliance. A certificate of compliance shall be required from a manufacturer in order to be listed as an approved source of supply in 6.4. The certificate of compliance submitted to DESC-ECS prior to listing as an approved source of supply shall state that the manufacturer's product meets the requirements of MIL-STD-883 (see 3.1 herein) and the requirements herein.

3.6 Certificate of conformance. A certificate of conformance as required in MIL-STD-883 (see 3.1 herein) shall be provided with each lot of microcircuits delivered to this drawing.

3.7 Notification of change. Notification of change to DESC-ECS shall be required in accordance with MIL-STD-883 (see 3.1 herein).

3.8 Verification and review. DESC, DESC's agent, and the acquiring activity retain the option to review the manufacturer's facility and applicable required documentation. Offshore documentation shall be made available onshore at the option of the reviewer.

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|                 |                      |
|-----------------|----------------------|
| Device type     | 01                   |
| Case outlines   | X and 3              |
| Terminal number | Terminal connection  |
| 1               | +VCC                 |
| 2               | OUT B                |
| 3               | No connection        |
| 4               | IN 16/8B             |
| 5               | IN 15/7B             |
| 6               | IN 14/6B             |
| 7               | IN 13/5B             |
| 8               | IN 12/4B             |
| 9               | IN 11/3B             |
| 10              | IN 10/2B             |
| 11              | IN 9/1B              |
| 12              | GND                  |
| 13              | V <sub>DD</sub> /LLS |
| 14              | A <sub>3</sub> /SDS  |
| 15              | A <sub>2</sub>       |
| 16              | A <sub>1</sub>       |
| 17              | A <sub>0</sub>       |
| 18              | Enable               |
| 19              | IN 1/1A              |
| 20              | IN 2/2A              |
| 21              | IN 3/3A              |
| 22              | IN 4/4A              |
| 23              | IN 5/5A              |
| 24              | IN 6/6A              |
| 25              | IN 7/7A              |
| 26              | IN 8/8A              |
| 27              | -VCC                 |
| 28              | OUT A                |

FIGURE 1. Terminal connections.

|   |                  |                |            |
|---|------------------|----------------|------------|
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16-channel multiplexer operation. 1/ 2/

| Use A <sub>3</sub> as digital address input |                |                |                |                | On channel to |       |
|---|----------------|----------------|----------------|----------------|---------------|-------|
| Enable                                      | A <sub>3</sub> | A <sub>2</sub> | A <sub>1</sub> | A <sub>0</sub> | OUT A         | OUT B |
| L   | X              | X              | X              | X              | None          | None  |
| H   | L              | L              | L              | L              | 1A            | None  |
| H   | L              | L              | L              | H              | 2A            | None  |
| H   | L              | L              | H              | L              | 3A            | None  |
| H   | L              | L              | H              | H              | 4A            | None  |
| H   | L              | H              | L              | L              | 5A            | None  |
| H   | L              | H              | L              | H              | 6A            | None  |
| H   | L              | H              | H              | L              | 7A            | None  |
| H   | L              | H              | H              | H              | 8A            | None  |
| H   | H              | L              | L              | L              | None          | 1B    |
| H   | H              | L              | L              | H              | None          | 2B    |
| H   | H              | L              | H              | L              | None          | 3B    |
| H   | H              | L              | H              | H              | None          | 4B    |
| H   | H              | H              | L              | L              | None          | 5B    |
| H   | H              | H              | L              | H              | None          | 6B    |
| H   | H              | H              | H              | L              | None          | 7B    |
| H   | H              | H              | H              | H              | None          | 8B    |

See footnotes at end of table.

FIGURE 2. Truth table.

|   |                  |                |            |
|---|------------------|----------------|------------|
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Differential 8-channel multiplexer operation. 2/ 3/

| A <sub>3</sub> connected to -V <sub>CC</sub> |                |                |                | On channel to |       |
|--|----------------|----------------|----------------|---------------|-------|
| Enable                                       | A <sub>2</sub> | A <sub>1</sub> | A <sub>0</sub> | OUT A         | OUT B |
| L  | X              | X              | X              | None          | None  |
| H  | L              | L              | L              | 1A            | 1B    |
| H  | L              | L              | H              | 2A            | 2B    |
| H  | L              | H              | L              | 3A            | 3B    |
| H  | L              | H              | H              | 4A            | 4B    |
| H  | H              | L              | L              | 5A            | 5B    |
| H  | H              | L              | H              | 6A            | 6B    |
| H  | H              | H              | L              | 7A            | 7B    |
| H  | H              | H              | H              | 8A            | 8B    |

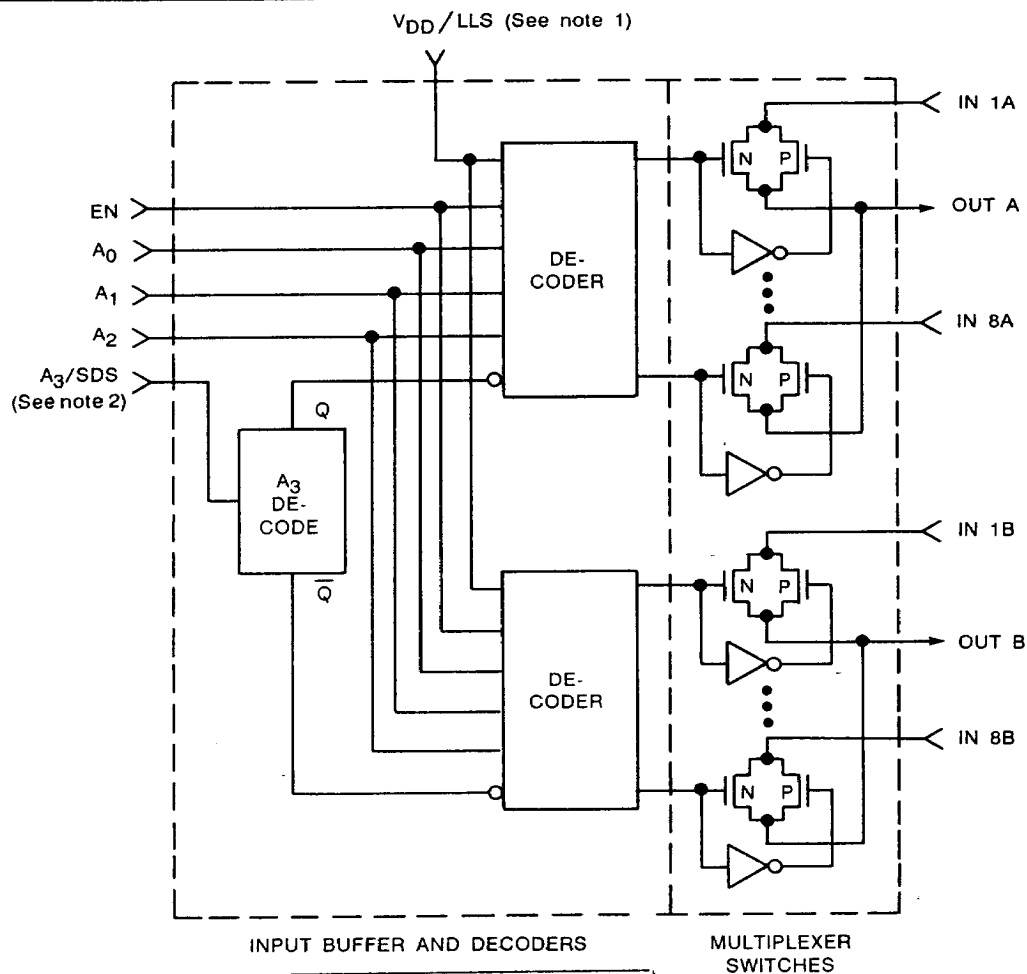
1/ For 16-channel operation, connect OUT A to OUT B.

2/ H = High logic level  
L = Low logic level  
X = Don't care

3/ For differential 8-channel operation, use the A<sub>3</sub> address pin to select the differential mode where A<sub>3</sub> = -V<sub>CC</sub> and OUT A is not connected to OUT B.

FIGURE 2. Truth table - Continued.

|   |                  |                |             |
|---|------------------|----------------|-------------|
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| A <sub>3</sub> decode |   |           |
|-----------------------|---|-----------|
| A <sub>3</sub>        | Q | $\bar{Q}$ |
| H                     | H | L         |
| L                     | L | H         |
| -V <sub>CC</sub>      | L | L         |

**NOTES:**

1. LLS = Logic level select. The circuit is TTL compatible when  $V_{DD}/LLS = GND$  or open, and CMOS compatible when  $V_{DD}/LLS = +15 V$ .
2. SDS = Single ended/differential select. Multiplexer is in differential mode when  $A_3/SDS = -V_{CC}$ .

FIGURE 3. Functional diagram.

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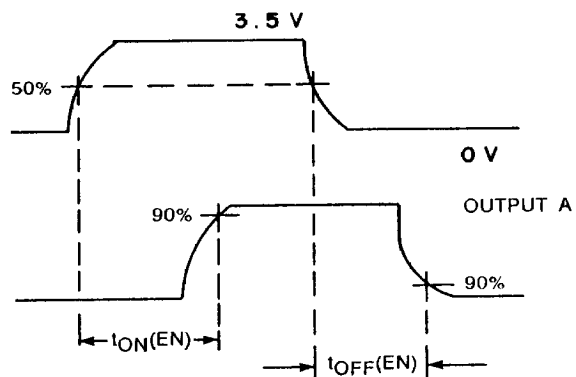
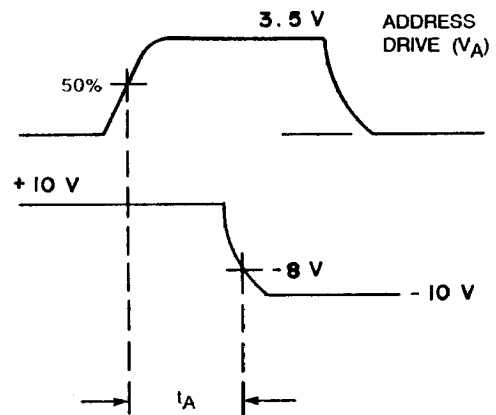
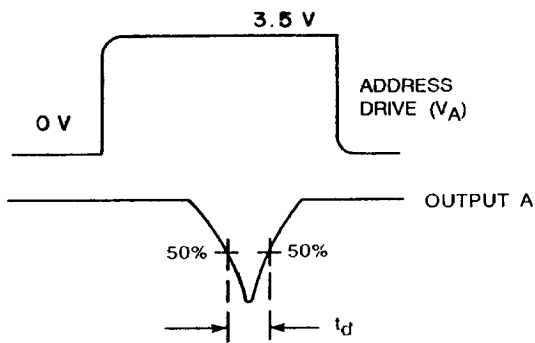


FIGURE 4. Switching waveforms.

|   |                         |  |                    |
|---|-------------------------|--|--------------------|
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#### 4. QUALITY ASSURANCE PROVISIONS

4.1 Sampling and inspection. Sampling and inspection procedures shall be in accordance with section 4 of MIL-M-38510 to the extent specified in MIL-STD-883 (see 3.1 herein).

4.2 Screening. Screening shall be in accordance with method 5004 of MIL-STD-883, and shall be conducted on all devices prior to quality conformance inspection. The following additional criteria shall apply:

a. Burn-in test, method 1015 of MIL-STD-883.

(1) Test condition A, B, C, or D using the circuit submitted with the certificate of compliance (see 3.5 herein).

(2)  $T_A = +125^{\circ}\text{C}$ , minimum.

b. Interim and final electrical test parameters shall be as specified in table II herein, except interim electrical parameter tests prior to burn-in are optional at the discretion of the manufacturer.

4.3 Quality conformance inspection. Quality conformance inspection shall be in accordance with method 5005 of MIL-STD-883 including groups A, B, C, and D inspections. The following additional criteria shall apply.

##### 4.3.1 Group A inspection.

a. Tests shall be as specified in table II herein.

b. Subgroups 5 and 6 in table I, method 5005 of MIL-STD-883 shall be omitted.

c. Subgroup 4 (capacitance measurement) shall be measured for initial qualification and after process or design changes which may affect capacitance. Sample size is fifteen devices, all input and output terminals tested, and no failures.

d. Subgroups 7 and 8 test sufficient to verify truth table.

##### 4.3.2 Groups C and D inspections.

a. End-point electrical parameters shall be as specified in table II herein.

b. Steady-state life test conditions, method 1005 of MIL-STD-883.

(1) Test condition A, B, C, or D using the circuit submitted with the certificate of compliance (see 3.5 herein).

(2)  $T_A = +125^{\circ}\text{C}$ , minimum.

(3) Test duration: 1,000 hours, except as permitted by method 1005 of MIL-STD-883.

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TABLE II. Electrical test requirements.

|  |  |
|--|--|
| MIL-STD-883 test requirements                                      | Subgroups<br>(per method<br>5005, table I) |
| Interim electrical parameters<br>(method 5004)                     | ---  |
| Final electrical test parameters<br>(method 5004)                  | 1*,2,3,7,8,<br>9,10,11                     |
| Group A test requirements<br>(method 5005)                         | 1,2,3,4**,7,8,<br>9,10,11                  |
| Groups C and D end-point<br>electrical parameters<br>(method 5005) | 1  |

\* PDA applies to subgroup 1.

\*\* See 4.3.1c.

## 5. PACKAGING

5.1 Packaging requirements. The requirements for packaging shall be in accordance with MIL-M-38510.

## 6. NOTES

6.1 Intended use. Microcircuits conforming to this drawing are intended for use when military specifications do not exist and qualified military devices that will perform the required function are not available for OEM application. When a military specification exists and the product covered by this drawing has been qualified for listing on QPL-38510, the device specified herein will be inactivated and will not be used for new design. The QPL-38510 product shall be the preferred item for all applications.

6.2 Replaceability. Microcircuits covered by this drawing will replace the same generic device covered by a contractor-prepared specification or drawing.

6.3 Comments. Comments on this drawing should be directed to DESC-ECS, Dayton, Ohio 45444, or telephone 513-296-5375.

|   |                  |                |             |
|---|------------------|----------------|-------------|
| <b>STANDARDIZED<br/>MILITARY DRAWING</b><br>DEFENSE ELECTRONICS SUPPLY CENTER<br>DAYTON, OHIO 45444 | SIZE<br><b>A</b> |                | 5962-88699  |
|   |                  | REVISION LEVEL | SHEET<br>14 |

6.4 Approved source of supply. An approved source of supply is listed herein. Additional sources will be added as they become available. The vendor listed herein has agreed to this drawing and a certificate of compliance (see 3.5 herein) has been submitted to DESC-ECS.

| Military drawing part number | Vendor CAGE number | Vendor similar part number <u>1/</u> |
|------------------------------|--------------------|--------------------------------------|
| 5962-8869901XX               | 34371              | HI1-516/883                          |
| 5962-88699013X               | 34371              | HI4-516/883                          |

1/ Caution. Do not use this number for item acquisition. Items acquired by this number may not satisfy the performance requirements of this drawing.

Vendor CAGE number

34371

Vendor name and address

Harris Semiconductor  
P.O. Box 883  
Melbourne, FL 32901

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