REVISIONS

LTR	DESCRIPTION	DATE (YR-MO-DA)	APPROVED
A	Change to vendor similar part number. Change to table I. Removed programming procedures for method A, programming waveforms, table III, and ESDS from the drawing. Removed final electrical test from table II. Added device type 04. Editorial changes throughout.	1990 FEB 26	M.A. Frye

REV																								
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REV STATUS OF SHEETS	REV	A	A	A	A	A	A	A				A	A	A	A	A								
	SHEET	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15								

PMIC N/A

STANDARDIZED MILITARY DRAWING

THIS DRAWING IS AVAILABLE FOR USE BY ALL DEPARTMENTS AND AGENCIES OF THE DEPARTMENT OF DEFENSE

AMSC N/A

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DRAWING APPROVAL DATE: 9 September 1988

REVISION LEVEL: A

DEFENSE ELECTRONICS SUPPLY CENTER
DAYTON, OHIO 45444

MICROCIRCUITS, DIGITAL, MEMORY, CMOS UV ERASABLE, PROGRAMMABLE LOGIC ARRAY, MONOLITHIC SILICON

SIZE	CAGE CODE	
A	67268	5962-88724

SHEET 1

DESC FORM 193
SEP 87

* U.S. GOVERNMENT PRINTING OFFICE: 1987 — 748-129/60911

5962-E1464

1. SCOPE

1.1 Scope. This drawing describes device requirements for class B microcircuits in accordance with 1.2.1 of MIL-STD-883, "Provisions for the use of MIL-STD-883 in conjunction with compliant non-JAN devices".

1.2 Part number. The complete part number shall be as shown in the following example:

5962-88724	01	K	X
Drawing number	Device type (1.2.1)	Case outline (1.2.2)	Lead finish per MIL-M-38510

1.2.1 Device types. The device types shall identify the circuit function as follows:

Device type	Generic number	Circuit function	t_{PD}
01	C22V10L	22-input 10-output AND-OR-logic array	25 ns
02	C22V10L	22-input 10-output AND-OR-logic array	30 ns
03	C22V10L	22-input 10-output AND-OR-logic array	40 ns
04	C22V10L	22-input 10-output AND-OR-logic array	20 ns

1.2.2 Case outlines. The case outlines shall be as designated in appendix C of MIL-M-38510, and as follows:

Outline letter	Case outline
K	F-6 (24-lead, .640" x .420" x .090"), flat package 1/
L	D-9 (24-lead, 1.280" x .310" x .200"), dual-in-line package 1/
3	C-4 (28-terminal .460" x .460" x .100"), square chip carrier package 1/

1.3 Absolute maximum ratings. 2/

Supply voltage range	-0.5 V dc to +7.0 V dc
Input voltage range	-2.0 V dc to +7.0 V dc 3/
Output voltage applied	-0.5 V dc to +7.0 V dc 3/
Output sink current	16 mA
Thermal resistance, junction-to-case (θ_{JC})	See MIL-M-38510, appendix C
Maximum power dissipation (P_D) 4/	1.2 W
Maximum junction temperature	+175°C
Lead temperature (soldering, 10 seconds maximum)	+300°C

1.4 Recommended operating conditions.

Supply voltage range (V_{CC})	4.5 V dc to 5.5 V dc
High level input voltage (V_{IH})	2.0 V dc minimum
Low level input voltage (V_{IL})	0.8 V dc maximum
Case operating temperature range (T_C)	-55°C to +125°C

1/ Lid shall be transparent to permit ultraviolet light erasure.
2/ All voltages referenced to V_{SS}.
3/ Minimum voltage is -0.6 V dc which may undershoot to -2.0 V dc for pulses of less than 20 ns. Maximum output pin voltage is V_{CC} +0.75 V dc which may overshoot to +7.0 V dc for pulses of less than 20 ns.
4/ Must withstand the added P_D due to short circuit test; e.g., I_{OS}.

2. APPLICABLE DOCUMENTS

2.1 Government specification, standard, and bulletin. Unless otherwise specified, the following specification, standard, and bulletin of the issue listed in that issue of the Department of Defense Index of Specifications and Standards specified in the solicitation, form a part of this drawing to the extent specified herein.

SPECIFICATION

MILITARY

MIL-M-38510 - Microcircuits, General Specification for.

STANDARD

MILITARY

MIL-STD-883 - Test Methods and Procedures for Microelectronics.

BULLETIN

MILITARY

MIL-BUL-103 - List of Standardized Military Drawings (SMD's).

(Copies of the specification, standard, and bulletin required by manufacturers in connection with specific acquisition functions should be obtained from the contracting activity or as directed by the contracting activity.)

2.2 Order of precedence. In the event of a conflict between the text of this drawing and the references cited herein, the text of this drawing shall take precedence.

3. REQUIREMENTS

3.1 Item requirements. The individual item requirements shall be in accordance with 1.2.1 of MIL-STD-883, "Provisions for the use of MIL-STD-883 in conjunction with compliant non-JAN devices" and as specified herein.

3.2 Design, construction, and physical dimensions. The design, construction, and physical dimensions shall be as specified in MIL-M-38510 and herein.

3.2.1 Terminal connections. The terminal connections shall be as specified on figure 1.

3.2.2 Truth table. The truth table shall be as specified on figure 2.

3.2.2.1 Unprogrammed devices. The truth table for unprogrammed devices for contracts involving no altered item drawing shall be as specified on figure 2. When required in group A, B, or C inspections (see 4.3), the devices shall be programmed by the manufacturer prior to test with a minimum of 50 percent of the total number of gates programmed or to any altered item drawing pattern which includes at least 25 percent of the total number of gates programmed.

3.2.2.2 Programmed devices. The requirements for supplying programmed devices are not part of this drawing.

3.2.3 Logic diagram. The logic diagram shall be as specified on figure 3.

3.2.4 Case outlines. The case outlines shall be in accordance with 1.2.2 herein.

TABLE I. Electrical performance characteristics.

Test	Symbol	Conditions 1/ V_{SS} = 0 V 4.5 V ≤ V_{CC} ≤ 5.5 V -55°C ≤ T_C ≤ +125°C unless otherwise specified	Group A subgroups	Device types	Limits		Unit
					Min	Max	
High level output voltage	V_{OH}	I_O = -2.0 mA	1, 2, 3	All	2.4		V
Low level output voltage	V_{OL}	I_O = 12.0 mA	1, 2, 3	All		0.5	V
High impedance output leakage current 2/	I_{OZ}	V_{CC} = 5.5 V and V_O = 5.5 V, V_O = GND	1, 2, 3	All	-10	10	µA
High level input current	I_{IH}	V_{IH} = 5.5 V	1, 2, 3	All		10	µA
		V_{IH} = 2.4 V	1, 2, 3	All		10	µA
Low level input current	I_{IL}	V_{IL} = 0.4 V	1, 2, 3	All		-10	µA
		V_{IL} = GND	1, 2, 3	All		-10	µA
Supply current	I_{CC}	V_{CC} = 5.5 V	1, 2, 3	All		15	mA
Output short circuit current 3/	I_{OS}	V_{CC} = 5.5 V	1, 2, 3	All	-30	-90	mA
Input capacitance	C_I 4/5/	V_I = 0 V, V_{CC} = 5.0 V T_A = +25°C, f = 1 MHz (see 4.3.1c)	4	All		6	pF
Output capacitance	C_O 4/5/	V_I = 0 V, V_{CC} = 5.0 V T_A = +25°C, f = 1 MHz (see 4.3.1c)	4	All		12	pF
Input or feedback to nonregistered output	t_{PD}	V_{CC} = 4.5 V, C_L = 50 pF See figure 4, circuit B and figure 5	9, 10, 11	01		25	ns
				02		30	
				03		40	
				04		20	

See footnotes at end of table.

TABLE I. Electrical performance characteristics - Continued.

Test	Symbol	Conditions 1/ V_{SS} = 0 V, 4.5 V ≤ V_{CC} ≤ 5.5 V, -55°C ≤ T_C ≤ +125°C unless otherwise specified	Group A subgroups	Device types	Limits Min	Limits Max	Unit
Clock to output	t_{CO}	V_{CC} = 4.5 V, C_L = 50 pF See figure 4, circuit B and figure 5	9, 10, 11	01		15	ns
				02		20	
				03		25	
				04		15	
Input to output enable	t_{EA}	V_{CC} = 4.5 V, C_L = 5 pF See figure 4, circuit A and figure 5	9, 10, 11	01		25	ns
				02		30	
				03		40	
				04		20	
Input to output disable	t_{ER}		9, 10, 11	01		25	ns
				02		30	
				03		40	
				04		20	
Clock pulse width 4/6/	t_W	V_{CC} = 4.5 V, C_L = 50 pF See figure 4, circuit B and figure 5	9, 10, 11	01	15		ns
				02	20		
				03	27		
				04	12		
Clock period	t_P		9, 10, 11	01	33		ns
				02	40		
				03	55		
				04	25		
Setup time 4/6/	t_S		9, 10, 11	01	18		ns
				02	20		
				03	30		
				04	17		

See footnotes at end of table.

TABLE I. Electrical performance characteristics - Continued.

Test	Symbol	Conditions 1/ V_{SS} = 0 V, 4.5 V ≤ V_{CC} ≤ 5.5 V, -55°C ≤ T_C ≤ +125°C unless otherwise specified	Group A subgroups	Device types	Limits Min	Limits Max	Unit
Hold time 4/6/	t_H	V_{CC} = 4.5 V, C_L = 50 pF See figure 4, circuit B and figure 5	9, 10, 11	All	0		ns
Maximum clock frequency 4/6/	f_{MAX}		9, 10, 11	01	30		MHz
				02	25		
				03	18		
				04	40		
Asynchronous reset pulse width	t_{AW}		9, 10, 11	01	25		ns
				02	30		
				03	40		
				04	20		
Asynchronous reset recovery time	t_{AR}		9, 10, 11	01	25		ns
				02	30		
				03	40		
				04	20		
Asynchronous reset to registered output reset	t_{AP}		9, 10, 11	01		25	ns
				02		30	
				03		40	
				04		22	

1/ All voltages are referenced to ground.
2/ I/O terminal leakage is the worst case of I_{IX} or I_{OZ}.
3/ Only one output shorted at a time.
4/ Tested initially and after any design or process changes that affect that parameter, and therefore shall be guaranteed to the limits specified in table I.
5/ All pins not being tested are to be open.
6/ Test applies only to registered outputs.

3.3 Electrical performance characteristics. Unless otherwise specified, the electrical performance characteristics are as specified in table I and shall apply over the full case operating temperature range.

3.4 Electrical test requirements. The electrical test requirements shall be the subgroups specified in table II. The electrical test for each subgroup are described in table I.

Device types	01 through 04	
Case outlines	L and K	3
Terminal number	Terminal symbol	
1	CK/I	NC
2	I	CK/I
3	I	I
4	I	I
5	I	I
6	I	I
7	I	I
8	I	NC
9	I	I
10	I	I
11	I	I
12	GND	I
13	I	I
14	I/O	GND
15	I/O	NC
16	I/O	I
17	I/O	I/O
18	I/O	I/O
19	I/O	I/O
20	I/O	I/O
21	I/O	I/O
22	I/O	NC
23	I/O	I/O
24	V_{CC}	I/O
25	---	I/O
26	---	I/O
27	---	I/O
28	---	V_{CC}

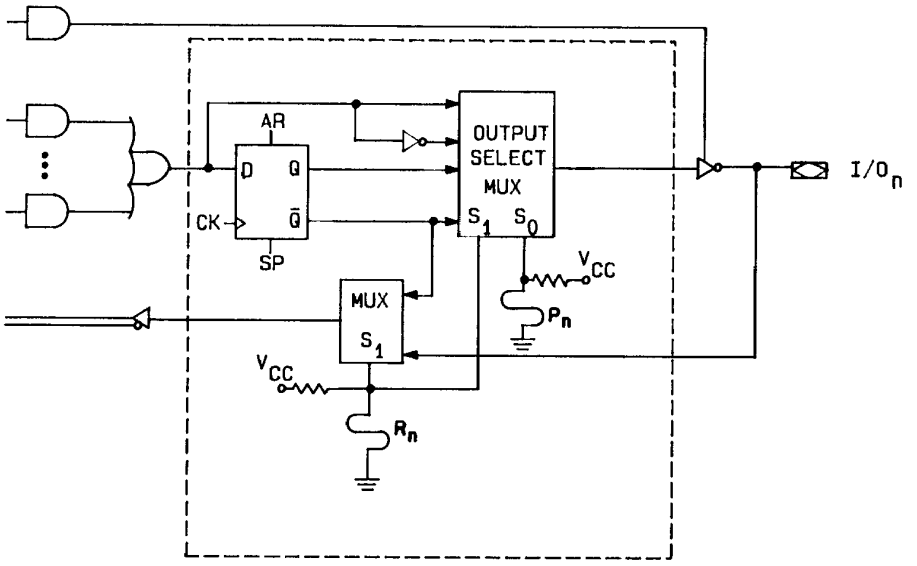
FIGURE 1. Terminal connections.

Truth table																					
Input pins												Output pins									
CK/I	I	I	I	I	I	I	I	I	I	I	I	I/O	I/O	I/O	I/O	I/O	I/O	I/O	I/O	I/O	I/O
X	X	X	X	X	X	X	X	X	X	X	X	Z	Z	Z	Z	Z	Z	Z	Z	Z	Z

NOTES:
1. Z = Three-state
2. X = Don't care

FIGURE 2. Truth table (unprogrammed).

OUTPUT LOGIC MACROCELL

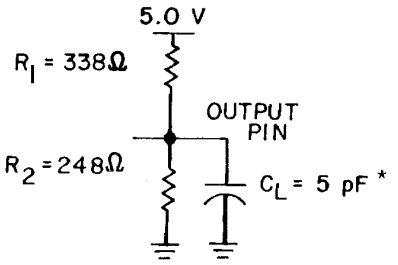


S_1	S_0	Output configuration
0	0	Registered/active low
0	1	Registered/active high
1	0	Combinatorial/active low
1	1	Combinatorial/active high

0 = Unblown fuse
1 = Blown fuse

FIGURE 3. Logic diagram (unprogrammed).

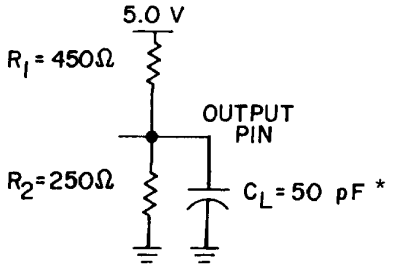
OUTPUT TEST LOAD



CIRCUIT A OR EQUIVALENT

* Including jig and scope (minimum value)

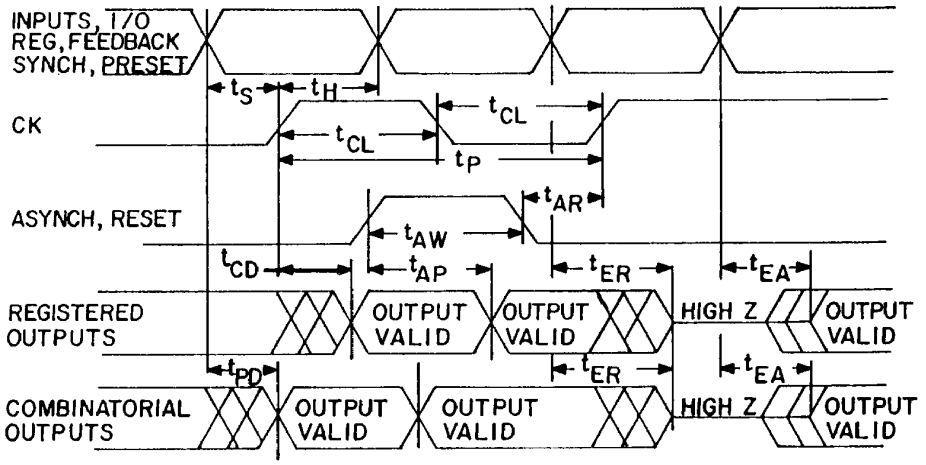
OUTPUT TEST LOAD



CIRCUIT B OR EQUIVALENT

* Including jig and scope (minimum value)

FIGURE 4. Output test circuit.



NOTE: Timing measurement reference is 1.5 V. Input ac driving levels are 0.0 V and 3.0 V unless otherwise specified.

FIGURE 5. Switching waveforms.

3.5 Marking. Marking shall be in accordance with MIL-STD-883 (see 3.1 herein). The part shall be marked with the part number listed in 1.2 herein. In addition, the manufacturer's part number may also be marked as listed in MIL-BUL-103 (see 6.6 herein).

3.6 Processing EPLDS. All testing requirements and quality assurance provisions herein shall be satisfied by the manufacturer prior to delivery.

3.6.1 Erasure of EPLDS. When specified, devices shall be erased in accordance with the procedures and characteristics specified in 4.4.

3.6.2 Programmability of EPLDS. When specified, devices shall be programmed to the specified pattern using the procedures and characteristics specified in 4.5.

3.6.3 Verification of erasure of programmability of EPLDS. When specified, devices shall be verified as either programmed to the specified pattern or erased. As a minimum, verification shall consist of performing a functional test (subgroup 7) to verify that all bits are in the proper state. Any bit that does not verify to be in the proper state shall constitute a device failure, and shall be removed from the lot.

3.7 Certificate of compliance. A certificate of compliance shall be required from a manufacturer in order to be listed as an approved source of supply in MIL-BUL-103 (see 6.6 herein). The certificate of compliance submitted to DESC-ECS prior to listing as an approved source of supply shall affirm that the manufacturer's product meets the requirements of MIL-STD-883 (see 3.1 herein) and the requirements herein.

3.8 Certificate of conformance. A certificate of conformance as required in MIL-STD-883 (see 3.1 herein) shall be provided with each lot of microcircuits delivered to this drawing.

3.9 Notification of change. Notification of change to DESC-ECS shall be required in accordance with MIL-STD-883 (see 3.1 herein).

3.10 Verification and review. DESC, DESC's agent, and the acquiring activity retain the option to review the manufacturer's facility and applicable required documentation. Offshore documentation shall be made available onshore at the option of the reviewer.

4. QUALITY ASSURANCE PROVISIONS

4.1 Sampling and inspection. Sampling and inspection procedures shall be in accordance with section 4 of MIL-M-38510 to the extent specified in MIL-STD-883 (see 3.1 herein).

4.2 Screening. Screening shall be in accordance with method 5004 of MIL-STD-883, and shall be conducted on all devices prior to quality conformance inspection. The following additional criteria shall apply:

a. Burn-in test, method 1015 of MIL-STD-883.

(1) Test condition C or D using the circuit submitted with the certificate of compliance (see 3.7 herein).

(2) T_A = +125°C, minimum.

b. Interim and final electrical test parameters shall be as specified in table II herein, except interim electrical parameter tests prior to burn-in are optional at the discretion of the manufacturer.

TABLE II. Electrical test requirements. 1/ 2/ 3/ 4/

MIL-STD-883 test requirements	Subgroups (per method 5005, table I)
Interim electrical parameters (method 5004)	1
Final electrical test parameters (method 5004)	1*,2,3,7*,8,9
Group A test requirements (method 5005)	1,2,3,4**,7, 8,9,10,11
Groups C and D end-point electrical parameters (method 5005)	2,3,7,8

1/ (*) indicates PDA applies to subgroups 1 and 7.
2/ Any or all subgroups may be combined when using high speed testers.
3/ Subgroups 7 and 8 functional tests shall verify that no fuses are blown for unprogrammed devices or that the altered item drawing pattern exists for programmed devices.
4/ (**) see 4.3.1c.

c. A data retention stress test shall be included as part of the screening procedure and shall consist of the following steps:

Margin test method A.

(1) Program greater than 95 percent of the bit locations, including the slowest programming cell. The remaining cells shall provide a worst case speed pattern.

(2) Bake, unbiased, for 72 hours at +140°C to screen for data retention lifetime.

(3) Perform a margin test using V_m = +5.8 V at +25°C using loose timing (i.e., t_{ACC} = 1 µs).

(4) Perform dynamic burn-in (see 4.2a).

(5) Margin at V_m = +5.8 V.

(6) Perform electrical tests (see 4.2).

(7) Erase (see 3.6.1), except devices submitted for groups A, B, C, and D testing.

(8) Verify erasure (see 3.6.3).

4.3 Quality conformance inspection. Quality conformance inspection shall be in accordance with method 5005 of MIL-STD-883 including groups A, B, C, and D inspections. The following additional criteria shall apply.

4.3.1 Group A inspection.

a. Tests shall be as specified in table II herein.

b. Subgroups 5 and 6 in table I, method 5005 of MIL-STD-883 shall be omitted.

c. Subgroup 4 (C_I and C_O measurements) shall be measured only for the initial qualification and after any process or design changes which may affect capacitance. Sample size is 15 devices with no failures, and all input and output terminals tested.

4.3.2 Groups C and D inspections.

a. End-point electrical parameters shall be as specified in table II herein.

b. Steady-state life test conditions, method 1005 of MIL-STD-883.

(1) Test condition C or D using the circuit submitted with the certificate of compliance (see 3.7 herein).

(2) T_A = +125°C, minimum.

(3) Test duration: 1,000 hours, except as permitted by method 1005 of MIL-STD-883.

4.4 Erasing procedures. The recommended erasure procedure is exposure to shortwave ultraviolet light which has a wavelength of 2537 angstroms (Å). The integrated dose (i.e., UV intensity x exposure time) for erasure should be a minimum of 15 Ws/cm^2. The erasure time with this dosage is approximately 15 to 20 minutes using an unltraviolet lamp with a 1200 $\mu W/cm^2$ power rating. The device should be placed within 1 inch of the lamp tubes during erasure. The maximum integrated dose the device can be exposed to without damage is 7258 Ws/cm^2 (1 week at 12000 $\mu W/cm^2$). Exposure of the device to high intensity UV light for long periods may cause permanent damage.

4.5 Programming procedures. The programming procedures shall be as specified by the device manufacture.

5. PACKAGING

5.1 Packaging requirements. The requirements for packaging shall be in accordance with MIL-M-38510.

6. NOTES

6.1 Intended use. Microcircuits conforming to this drawing are intended for use when military specifications do not exist and qualified military devices that will perform the required function are not available for OEM application. When a military specification exists and the product covered by this drawing has been qualified for listing on QPL-38510, the device specified herein will be inactivated and will not be used for new design. The QPL-38510 product shall be the preferred item for all applications.

6.2 Replaceability. Microcircuits covered by this drawing will replace the same generic device covered by a contractor-prepared specification or drawing.

6.3 Configuration control of SMD's. All proposed changes to existing SMD's will be coordinated with the users of record for the individual documents. This coordination will be accomplished in accordance with MIL-STD-481 using DD Form 1693, Engineering Change Proposal (Short Form).

6.4 Record of users. Military and industrial users shall inform the Defense Electronics Supply Center when a system application requires configuration control and the applicable SMD. DESC will maintain a record of users and this list will be used for coordination and distribution of changes to the drawings. Users of drawings covering microelectronic devices (FSC 5962) should contact DESC-ECS, telephone (513) 296-6022.

6.5 Comments. Comments on this drawing should be directed to DESC-ECS, Dayton, Ohio 45444, or telephone 513-296-5375.

6.6 Approved source of supply. An approved source of supply is listed in MIL-BUL-103. Additional sources will be added to MIL-BUL-103 as they become available. The vendor listed in MIL-BUL-103 has agreed to this drawing and a certificate of compliance (see 3.7 herein) has been submitted to and accepted by DESC-ECS. The approved sources of supply listed below are for information purposes only and are current only to the date of the last action of this document.

Military drawing part number	Vendor CAGE number	Vendor similar part number 1/
5962-8872401KX	1FN41	AT22V10L-25YM/883
5962-8872401LX	1FN41	AT22V10L-25DM/883
5962-88724013X	1FN41	AT22V10L-25LM/883
5962-8872402KX	1FN41	AT22V10L-30YM/883
5962-8872402LX	1FN41	AT22V10L-30DM/883
5962-88724023X	1FN41	AT22V10L-30LM/883
5962-8872403KX	1FN41	AT22V10L-40YM/883
5962-8872403LX	1FN41	AT22V10L-40DM/883
5962-88724033X	1FN41	AT22V10L-40LM/883
5962-8872404KX	1FN41	AT22V10L-20YM/883
5962-8872404LX	1FN41	AT22V10L-20DM/883
5962-88724043X	1FN41	AT22V10L-20LM/883

1/ Caution. Do not use this number for item acquisition. Items acquired to this number may not satisfy the performance requirements of this drawing.

Vendor CAGE number	Vendor name and address
1FN41	ATMEL Corporation 2095 Ringwood Avenue San Jose, CA 95131