REVISIONS			
LTR	DESCRIPTION	DATE (YR-MO-DA)	APPROVED

REV																									
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REV STATUS OF SHEETS	REV																								
	SHEET	1	2	3	4	5	6	7	8	9	10	11	12	13	14										

PMIC N/A

STANDARDIZED MILITARY DRAWING

THIS DRAWING IS AVAILABLE FOR USE BY ALL DEPARTMENTS AND AGENCIES OF THE DEPARTMENT OF DEFENSE

AMSC N/A

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APPROVED BY: [redacted]

DRAWING APPROVAL DATE: 26 APRIL 1989

REVISION LEVEL:

DEFENSE ELECTRONICS SUPPLY CENTER
DAYTON, OHIO 45444

MICROCIRCUIT, MEMORY, DIGITAL, CMOS, 2K X 8 BIT, ONE TIME PROGRAMMABLE PROM, MONOLITHIC SILICON

SIZE	CAGE CODE	5962-88734
A	67268	

SHEET 1 OF 14

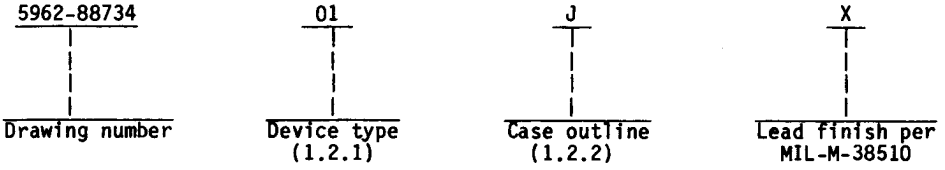
DESC FORM 193
SEP 87

* U.S. GOVERNMENT PRINTING OFFICE: 1987 — 748-129/60911

1. SCOPE

1.1 Scope. This drawing describes device requirements for class B microcircuits in accordance with 1.2.1 of MIL-STD-883, "Provisions for the use of MIL-STD-883 in conjunction with compliant non-JAN devices".

1.2 Part number. The complete part number shall be as shown in the following example:



1.2.1 Device types. The device types shall identify the circuit function as follows:

Device type	Generic number	Circuit function	Access time
01	See 6.4	2K x 8-bit PROM	55 ns
02	See 6.4	2K x 8-bit PROM	45 ns
03	See 6.4	2K x 8-bit PROM	35 ns
04	See 6.4	2K x 8-bit PROM	25 ns

1.2.2 Case outlines. The case outlines shall be as designated in appendix C of MIL-M-38510, and as follows:

Outline letter	Case outline
J	D-3 (24-lead, 1.290" x 0.610" x 0.225"), dual-in-line package
K	F-6 (24-lead, 0.640" x 0.420" x 0.090"), flat package
L	D-9 (24-lead, 1.280" x 0.310" x 0.200"), dual-in-line package
3	C-4 (28-terminal, 0.460" x 0.460" x 0.100"), square leadless chip carrier package

1.3 Absolute maximum ratings.

Supply voltage (V_{CC})	+4.5 V dc to +5.5 V dc
Storage temperature range	-65°C to +150°C
Voltages on any pin with respect to ground	-0.6 V dc to +7.0 V dc
V_{PP} with respect to ground	-0.6 V dc to +13.0 V dc
Power dissipation (P_D)	550 mW 1/
Lead temperature (soldering, 10 seconds)	+300°C
Thermal resistance, junction-to-case (θ_{JC})	See MIL-M-38510, appendix C

1.4 Recommended operating conditions.

Case operating temperature range (T_C)	-55°C to +125°C

1/ Must withstand the added P_D due to short-circuit test; e.g., I_{OS}.

2. APPLICABLE DOCUMENTS

2.1 Government specification and standard. Unless otherwise specified, the following specification and standard, of the issue listed in that issue of the Department of Defense Index of Specifications and Standards specified in the solicitation, form a part of this drawing to the extent specified herein.

SPECIFICATION

MILITARY

MIL-M-38510 - Microcircuits, General Specification for.

STANDARD

MILITARY

MIL-STD-883 - Test Methods and Procedures for Microelectronics.

(Copies of the specification and standard required by manufacturers in connection with specific acquisition functions should be obtained from the contracting activity or as directed by the contracting activity.)

2.2 Order of precedence. In the event of a conflict between the text of this drawing and the references cited herein, the text of this drawing shall take precedence.

3. REQUIREMENTS

3.1 Item requirements. The individual item requirements shall be in accordance with 1.2.1 of MIL-STD-883, "Provisions for the use of MIL-STD-883 in conjunction with compliant non-JAN devices" and as specified herein.

3.2 Design, construction, and physical dimensions. The design, construction, and physical dimensions shall be as specified in MIL-M-38510 and herein.

3.2.1 Terminal connections. The terminal connections shall be as specified on figure 1.

3.2.2 Truth tables. The truth tables shall be as specified on figure 2.

3.2.2.1 Unprogrammed or erased devices. The truth table for unprogrammed devices for contracts involving no altered item drawing shall be specified on figure 2 as applicable. When required in group A, B, or C (see 4.3), the devices shall be programmed by the manufacturer prior to test in a checkerboard pattern or equivalent with (a minimum of 50 percent of the total number of gates programmed) or to any altered item drawing pattern which includes at least 25 percent of the total number of gates programmed.

3.2.2.2 Programmed devices. The truth tables for programmed devices shall be as specified by an attached altered item drawing.

3.2.3 Case outlines. The case outlines shall be in accordance with 1.2.2 herein.

3.3 Electrical performance characteristics. Unless otherwise specified, the electrical performance characteristics are as specified in table I and shall apply over the full case operating temperature range.

TABLE I. Electrical performance characteristics.

Test	Symbol	Conditions $-55°C \le T_C \le +125°C$ $4.5\ V\ dc \le V_{CC} \le 5.5\ V\ dc$ unless otherwise specified	Group A subgroups	Device type	Limits		Unit
					Min	Max	
Input low voltage	V_{IL}	V_{CC} = 4.5 V and 5.5 V	1, 2, 3	All	-0.5 1/	0.8	V
Input high voltage	V_{IH}	V_{CC} = 4.5 V and 5.5 V	1, 2, 3	All	2.0	V_{CC} +0.5 1/	V
Output low voltage 2/	V_{OL}	I_{OL} = 16 mA, V_{CC} = 4.5 V V_{IL} = 0.8 V, V_{IH} = 2.0 V	1, 2, 3	All		0.45	V
Output high voltage 2/	V_{OH}	I_{OH} = -4 mA, V_{CC} = 4.5 V V_{IL} = 0.8 V, V_{IH} = 2.0 V	1, 2, 3	All	2.4		V
Output short-circuit current 1/	I_{OS}	V_{CC} = 5.5 V V_{OUT} = GND	1, 2, 3	All		200	mA
Input load current 3/	I_{L1}	V_{IN} = 5.5 V and GND	1, 2, 3	All		±10	µA
Output leakage	I_{LO}	V_{OUT} = 5.5 V and GND	1, 2, 3	All		±10	µA
Operating active current 4/	I_{CC}	$\overline{CS}_1 = V_{IL}$, V_{CC} = 5.5 V O_0 to O_7 = 0 mA $CS_2 = CS_3 = V_{IH}$ f = $1/t_{ACC}$	1, 2, 3	All		120	mA
Input capacitance	C_{IN}	V_{IN} = 0 V, see 4.3.1c	4	All		6	pF
Output capacitance	C_{OUT}	V_{OUT} = 0 V, see 4.3.1c	4	All		12	pF
Address to output delay 5/	t_{ACC}	$\overline{CS}_1 = V_{IL}$ $CS_2 = CS_3 = V_{IH}$	9, 10, 11	01		55	ns
				02		45	ns
				03		35	ns
				04		25	ns

See footnotes at end of table.

TABLE I. Electrical performance characteristics - Continued.

Test	Symbol	Conditions $-55°C \le T_C \le +125°C$ 4.5 V dc $\le V_{CC} \le$ 5.5 V dc unless otherwise specified	Group A subgroups	Device type	Limits		Unit
					Min	Max	
All chip selects to output delay 4/ 5/	t_{CS}	Either $\overline{CS}_1$, CS_2, or CS_3 6/	9, 10, 11	01, 02,03 04		30 25 20	ns ns
All chip selects high to output float 1/ 5/	t_{DF}	Either $\overline{CS}_1$, CS_2, or CS_3 6/	9, 10, 11	01,02 03 04		25 20	ns
Address to output hold 1/ 5/	t_{OH}	$\overline{CS}_1 = V_{IL}$ $CS_2 = CS_3 = V_{IH}$	9, 10, 11	All	0		ns

1/ May not be tested, but shall be guaranteed to the limits specified in table I.

2/ These are absolute voltages with respect to device ground pin and include all over shoots due to system and/or tester noise. Do not attempt to test these values without suitable equipment.

3/ Output shall be loaded in accordance with figure 4.

4/ The addresses, (A_0-A_{10} pins), are toggling between V_{IL} and V_{IH}.

5/ See figures 3 and 4.

6/ Worst case of output control signal lines $\overline{CS}_1$, CS_2, or CS_3.

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Device types	01 through 04	
Case outlines	J, K, L	3
Terminal number	Terminal symbol	
1	A_7	NC
2	A_6	A_7
3	A_5	A_6
4	A_4	A_5
5	A_3	A_4
6	A_2	A_3
7	A_1	A_2
8	A_0	A_1
9	O_0	A_0
10	O_1	NC
11	O_2	O_0
12	GND	O_1
13	O_3	O_2
14	O_4	GND
15	O_5	NC
16	O_6	O_3
17	O_7	O_4
18	CS_3	O_5
19	CS_2	O_6
20	$\overline{CS}_1/Vpp$	O_7
21	A_{10}	NC
22	A_9	CS_3
23	A_8	CS_2
24	V_{CC}	CS_1/Vpp
25	--	A_{10}
26	--	A_9
27	--	A_8
28	--	V_{CC}

FIGURE 1. Terminal connections.

Truth table A

	CS1/VPP	CS2	CS3	I/O pins
Programs	VPP	C	C	Data in
Read	VIL	VIH	VIH	Data out
Deselect	VIH	X	X	High - Z
Deselect	X	VIL	X	High - Z
Deselect	X	X	VIL	High - Z

FIGURE 2. Truth tables.

Truth table B

Pin functions					
Mode	Read or output disable	CS_3	CS_2	$\overline{CS_1}$	Outputs
	Other	$\overline{PGM}$	$\overline{VFY}$	V_{PP}	Outputs
Read 1/		V_{IH}	V_{IH}	V_{IL}	Data out
Output disable 1/, 2/		X	X	V_{IH}	High - Z
Output disable 1/, 2/		X	V_{IL}	X	High - Z
Output disable 1/, 2/		V_{IL}	X	X	High - Z
Program 1/		V_{ILP}	V_{IHP}	V_{PP}	Data in
Program verify 1/		V_{IHP}	V_{ILP}	V_{PP}	Data out
Program inhibit 1/		V_{IHP}	V_{IHP}	V_{PP}	High - Z
Intelligent program 1/		V_{ILP}	V_{IHP}	V_{PP}	Data in

NOTES:
1. During programming and verification, all unspecified pins to be at V_{ILP}.
2. X = Don't care but not to exceed V_{CC} plus 5%.
3. V_{PP} = 13.5 V ±0.5 V; V_{ILP} = 0.4 V maximum; V_{IHP} = 3.0 V minimum.

FIGURE 2. Truth tables - Continued.

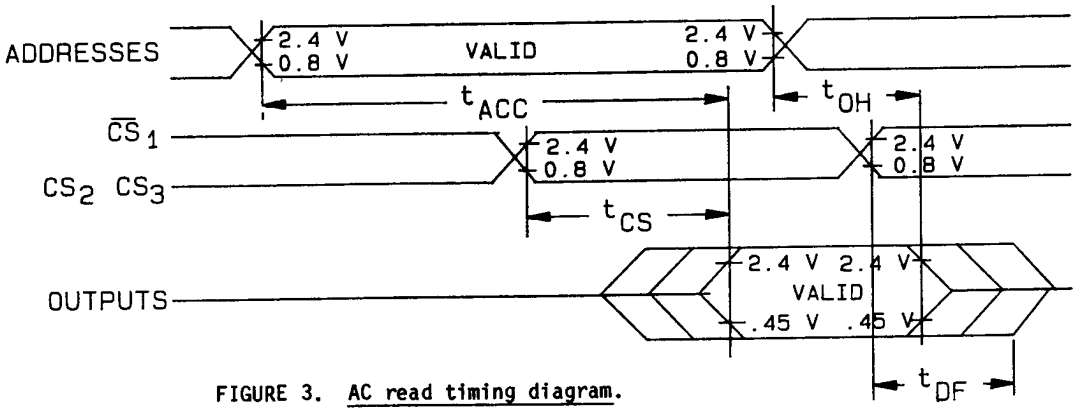
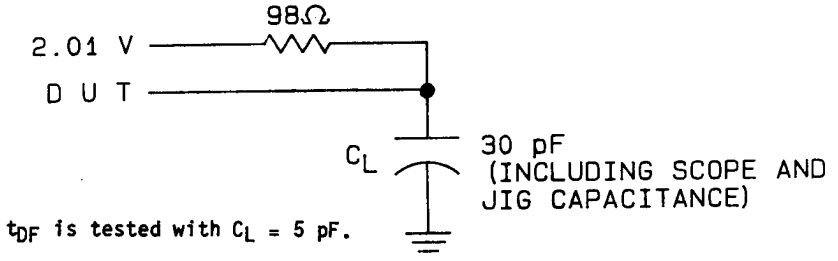


FIGURE 3. AC read timing diagram.

High impedance test systems only.



t_{DF} is tested with C_L = 5 pF.

FIGURE 4. Output load.

3.4 Marking. Marking shall be in accordance with MIL-STD-883 (see 3.1 herein). The part shall be marked with the part number listed in 1.2 herein. In addition, the manufacturer's part number may also be marked as listed in 6.4 herein.

3.5 Processing options. Since the PROM is an unprogrammed memory capable of being programmed by either the manufacturer or the user to result in a wide variety of PROM configurations, two processing options are provided for selection in the contract, using an altered item drawing.

3.5.1 Unprogrammed PROM delivered to the user. All testing shall be verified through group A testing as defined in 4.3.1. It is recommended that users perform subgroups 7 and 9 after programming to verify specific program configuration.

3.5.2 Manufacturer-programmed PROM delivered to the user. All testing requirements and quality assurance provisions herein, including the requirements of the altered item drawing shall be satisfied by the manufacturer prior to delivery.

3.6 Certificate of compliance. A certificate of compliance shall be required from a manufacturer in order to be listed as an approved source of supply in 6.4. The certificate of compliance submitted to DESC-ECS prior to listing as an approved source of supply shall state that the manufacturer's product meets the requirements of MIL-STD-883 (see 3.1 herein) and the requirements herein.

3.7 Certificate of conformance. A certificate of conformance as required in MIL-STD-883 (see 3.1 herein) shall be provided with each lot of microcircuits delivered to this drawing.

3.8 Notification of change. Notification of change to DESC-ECS shall be required in accordance with MIL-STD-883 (see 3.1 herein).

3.9 Verification and review. DESC, DESC's agent, and the acquiring activity retain the option to review the manufacturer's facility and applicable required documentation. Offshore documentation shall be made available onshore at the option of the reviewer.

4. QUALITY ASSURANCE PROVISIONS

4.1 Sampling and inspection. Sampling and inspection procedures shall be in accordance with section 4 of MIL-M-38510 to the extent specified in MIL-STD-883 (see 3.1 herein).

4.2 Screening. Screening shall be in accordance with method 5004 of MIL-STD-883, and shall be conducted on all devices prior to quality conformance inspection. The following additional criteria shall apply:

a. Burn-in test, method 1015 of MIL-STD-883 .

(1) Test condition D or E using the circuit submitted with the certificate of compliance (see 3.6 herein).

(2) T_A = +125°C, minimum.

b. Interim and final electrical test parameters shall be as specified in table II herein, except interim electrical parameter tests prior to burn-in are optional at the discretion of the manufacturer.

4.3 Quality conformance inspection. Quality conformance inspection shall be in accordance with method 5005 of MIL-STD-883 including groups A, B, C, and D inspections. The following additional criteria shall apply.

4.3.1 Group A inspection.

a. Tests shall be as specified in table II herein.

b. Subgroups 5 and 6 in table I, method 5005 of MIL-STD-883 shall be omitted.

c. Subgroup 4 (C_{IN} and C_{OUT} measurements) shall be measured only for the initial test and after process or design changes which may affect capacitance. Sample size is 15 devices with no failures, and all input and output terminals tested.

d. Unprogrammed devices shall be tested for programmability and ac performance compliance to the requirements of group A, subgroups 9, 10 and 11.

(1) A sample shall be selected to satisfy programmability requirements prior to performing subgroup 9. Twelve devices shall be submitted to programming (see 3.2.2.1). If more than two devices fail to program, the lot shall be rejected. At the manufacturers option, the sample may be increased to 24 total devices with no more than 4 total device failures allowable.

(2) Ten devices from the programmablity sample shall be submitted to the requirements of group A, subgroups 9, 10 and 11. If more than two devices fail, the lot shall be rejected. At the manufacturers option, the sample may be increased to 20 total devices with no more than 4 total device failures allowable.

e. Subgroups 7 and 8 shall verify the truth table as specified on figure 2.

4.3.2 Groups C and D inspections.

a. End-point electrical parameters shall be as specified in table II herein.

b. Steady-state life test conditions, method 1005 of MIL-STD-883.

(1) Test condition D or E using the circuit submitted with the certificate of compliance (see 3.6 herein).

(2) T_A = +125°C, minimum.

(3) Test duration: 1,000 hours, except as permitted by method 1005 of MIL-STD-883.

4.4 Programming procedures. The programming procedures shall be as specified by the device manufacturer.

4.5 Electrostatic discharge sensitvity (ESDS). Electrostatic discharge sensitivity (ESDS) testing shall be performed in accordance with MIL-STD-883, method 3015 and MIL-M-38510 for intial testing and after any design or process changes which may affect input or output protection circuitry. The option to categorize devices as ESD sensitive without performing the test is not allowed. Only those device types that pass ESDS testing at 1000 volts or greater shall be considered as conforming to the requirements of this drawing.

TABLE II. Electrical test requirements. 1/

MIL-STD-883 test requirements	Subgroups (per method 5005, table I)
Interim electrical parameters (method 5004)	---
Final electrical test parameters (method 5004) for unprogrammed devices	1*,2,3,7*,8
Final electrical test parameters (method 5004) for programmed devices	1*,2,3,7*,8,9
Group A test requirements (method 5005)	1,2,3,4**,7, 8,9,10,11
Groups C and D end-point electrical parameters (method 5005)	2,3,7,8

* PDA applies to subgroups 1 and 7.
** See 4.3.1c.
1/ Any subgroups at the same temperature may be combined when using a multifunction tester.

5. PACKAGING

5.1 Packaging requirements. The requirements for packaging shall be in accordance with MIL-M-38510.

6. NOTES

6.1 Intended use. Microcircuits conforming to this drawing are intended for use when military specifications do not exist and qualified military devices that will perform the required function are not available for OEM application. When a military specification exists and the product covered by this drawing has been qualified for listing on QPL-38510, the device specified herein will be inactivated and will not be used for new design. The QPL-38510 product shall be the preferred item for all applications.

6.2 Replaceability. Microcircuits covered by this drawing will replace the same generic device covered by a contractor-prepared specification or drawing.

6.3 Comments. Comments on this drawing should be directed to DESC-ECS, Dayton, Ohio 45444, or telephone 513-296-5375.

6.4 Approved sources of supply. Approved sources of supply are listed herein. Additional sources will be added as they become available. The vendor listed herein has agreed to this drawing and a certificate of compliance (see 3.6 herein) has been submitted to DESC-ECS.

Military drawing part number	Vendor CAGE number	Vendor similar part number 1/
5962-8873401JX	66579	WS57C191B-55YMB
5962-8873401KX	66579	WS57C291B-55HMB
5962-8873401LX	66579	WS57C291B-55KMB
5962-88734013X	66579	WS57C291B-55ZMB
5962-8873402JX	66579 65786	WS57C191B-45YMB CY7C292A-45DMB
5962-8873402KX	66579 65786	WS57C291B-45HMB CY7C291A-45KMB
5962-8873402LX	66579 65786	WS57C291B-45KMB CY7C291A-45DMB
5962-88734023X	66579 65786	WS57C291B-45ZMB CY7C291A-45LMB
5962-8873403KX	65786	CY7C291A-35KMB
5962-8873403LX	65786	CY7C291A-35DMB
5962-88734033X	65786	CY7C291A-35LMB
5962-8873403JX	65786	CY7C292A-35DMB
5962-8873404KX	65786	CY7C291A-25KMB
5962-8873404LX	65786	CY7C291A-25DMB

See footnote at end of table.

Military drawing part number	Vendor CAGE number	Vendor similar part number 1/
5962-88734043X	65786	CY7C291A-25LMB
5962-8873404JX	65786	CY7C292A-25DMB

1/ Caution. Do not use this number for item acquisition. Items aquired to this number may not satisfy the performance requirements of this drawing.

Vendor CAGE number	Vendor name and address	Truth table
66579	Waferscale Integration, Incorporated 47280 Kato Road Fremont, CA 94538	A
65786	Cypress Semiconductor Corporation 3901 North First Street San Jose, CA 95134	B

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