REVISIONS			
LTR	DESCRIPTION	DATE (YR-MO-DA)	APPROVED
C	Add device type 05. Add vendor CAGE 27014. Make changes to 1.3, 1.4, table I, figures 1, 3, 4, 5, and 6.	93-05-10	M. A. FRYE
D	Changes in accordance with N.O.R. 5962-R053-94.	94-06-24	M. A. FRYE
E	Redrawn with changes. Technical and editorial changes throughout.	94-10-28	M. A. FRYE
F	Make change to I_{CEX} test for device type 05 as specified under table I. - ro	98-01-06	R. MONNIN

THE ORIGINAL FIRST SHEET OF THIS DRAWING HAS BEEN REPLACED.

REV																				
SHEET																				
REV	F	F																		
SHEET	15	16																		

REV STATUS OF SHEETS	REV	F	F	F	F	F	F	F	F	F	F	F	F	F
	SHEET	1	2	3	4	5	6	7	8	9	10	11	12	13	14

PMIC N/A

STANDARD MICROCIRCUIT DRAWING

THIS DRAWING IS AVAILABLE FOR USE BY ALL DEPARTMENTS AND AGENCIES OF THE DEPARTMENT OF DEFENSE

AMSC N/A

PREPARED BY
GARY ZAHN

CHECKED BY
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APPROVED BY
MICHAEL A. FRYE

DRAWING APPROVAL DATE
89-12-04

REVISION LEVEL
F

DEFENSE SUPPLY CENTER COLUMBUS
COLUMBUS, OHIO 43216

MICROCIRCUIT, LINEAR, CMOS, PRECISION TIMERS, MONOLITHIC SILICON

SIZE	CAGE CODE	
A	**67268**	**5962-89503**

SHEET 1 OF 16

DSCC FORM 2233
APR 97

5962-E119-98

1. SCOPE

1.1 Scope. This drawing describes device requirements for MIL-STD-883 compliant, non-JAN class level B microcircuits in accordance with MIL-PRF-38535, appendix A.

1.2 Part or Identifying Number (PIN). The complete PIN is as shown in the following example:

5962-89503	01	C	X
Drawing number	Device type (see 1.2.1)	Case outline (see 1.2.2)	Lead finish (see 1.2.3)

1.2.1 Device type(s). The device type(s) identify the circuit function as follows:

Device type	Generic number	Circuit function
01	TLC555	CMOS, precision timer, single
02	TLC556	CMOS, precision timer, dual
03	7555	CMOS, low power, precision timer, single
04	7556	CMOS, low power, precision timer, dual
05	LMC555	CMOS, low voltage, precision timer, single

1.2.2 Case outline(s). The case outline(s) are as designated in MIL-STD-1835 and as follows:

Outline letter	Descriptive designator	Terminals	Package style
C	GDIP1-T14 or CDIP2-T14	14	Dual-in-line
G	MACY1-X8	8	Can
P	GDIP1-T8 or CDIP2-T8	8	Dual-in-line
2	CQCC1-N20	20	Square leadless chip carrier

1.2.3 Lead finish. The lead finish is as specified in MIL-PRF-38535, appendix A.

1.3 Absolute maximum ratings.

Supply voltage (V_{DD}):
- Device types 01-04 ..... 18 V dc
- Device type 05 ..... 15 V dc

Input voltage range ..... -0.3 V to V_{DD} (+0.3 V)

Output sink current:
- Device types 01 and 02 ..... 150 mA
- Device types 03 and 04 ..... 20 mA
- Device type 05 ..... 100 mA

Output source current:
- Device types 01 and 02 ..... 15 mA
- Device types 03 and 04 ..... 0.8 mA
- Device type 05 ..... 10 mA

Storage temperature range ..... -65°C to +150°C

Lead temperature (soldering, 10 seconds) ..... +300°C

Junction temperature (T_J) ..... +175°C

1.3 Absolute maximum ratings - Continued.

Power dissipation (P_D): (T_A = +125° C):
Device types 01-04:
Cases C and 2 ..... 550 mW
Case G ..... 23 mW
Case P ..... 420 mW
Device type 05:
Cases C, G, P, and 2 ..... 550 mW
Thermal resistance, junction-to-case (Θ_{JC}):
Cases C and P ..... 28° C/W
Case G:
Device types 01-04 ..... 70° C/W
Device type 05 ..... 30° C/W
Case 2 ..... 20° C/W
Thermal resistance, junction-to-ambient (Θ_{JA}):
Cases C and 2 ..... 91° C/W
Case G:
Device types 01-04 ..... 150° C/W
Device type 05 ..... 180° C/W
Case P:
Device types 01-04 ..... 119° C/W
Device type 05 ..... 125° C/W

1.4 Recommended operating conditions.

Supply voltage range (V_{DD}):
Device types 01-02 ..... +5.0 V dc to +15.0 V dc
Device types 03-04 ..... +5.0 V dc to +18.0 V dc
Device type 05 ..... +1.5 V dc to +15.0 V dc
Ambient operating temperature range ..... -55° C to +125° C

2. APPLICABLE DOCUMENTS

2.1 Government specification, standards, and handbooks. The following specification, standards, and handbooks form a part of this drawing to the extent specified herein. Unless otherwise specified, the issues of these documents are those listed in the issue of the Department of Defense Index of Specifications and Standards (DoDISS) and supplement thereto, cited in the solicitation.

SPECIFICATION

DEPARTMENT OF DEFENSE

MIL-PRF-38535 - Integrated Circuits, Manufacturing, General Specification for.

STANDARDS

DEPARTMENT OF DEFENSE

MIL-STD-883 - Test Method Standard Microcircuits.
MIL-STD-973 - Configuration Management.
MIL-STD-1835 - Interface Standard For Microcircuit Case Outlines.

HANDBOOKS

DEPARTMENT OF DEFENSE

MIL-HDBK-103 - List of Standard Microcircuit Drawings (SMD's).
MIL-HDBK-780 - Standard Microcircuit Drawings.

(Unless otherwise indicated, copies of the specification, standards, and handbooks are available from the Standardization Document Order Desk, 700 Robbins Avenue, Building 4D, Philadelphia, PA 19111-5094.)

2.2 Order of precedence. In the event of a conflict between the text of this drawing and the references cited herein, the text of this drawing takes precedence. Nothing in this document, however, supersedes applicable laws and regulations unless a specific exemption has been obtained.

3. REQUIREMENTS

3.1 Item requirements. The individual item requirements shall be in accordance with MIL-PRF-38535, appendix A for non-JAN class level B devices and as specified herein. Product built to this drawing that is produced by a Qualified Manufacturer Listing (QML) certified and qualified manufacturer or a manufacturer who has been granted transitional certification to MIL-PRF-38535 may be processed as QML product in accordance with the manufacturers approved program plan and qualifying activity approval in accordance with MIL-PRF-38535. This QML flow as documented in the Quality Management (QM) plan may make modifications to the requirements herein. These modifications shall not affect form, fit, or function of the device. These modifications shall not affect the PIN as described herein. A "Q" or "QML" certification mark in accordance with MIL-PRF-38535 is required to identify when the QML flow option is used.

3.2 Design, construction, and physical dimensions. The design, construction, and physical dimensions shall be as specified in MIL-PRF-38535, appendix A and herein.

3.2.1 Case outline(s). The case outline(s) shall be in accordance with 1.2.2 herein.

3.2.2 Terminal connections. The terminal connections shall be as specified on figure 1.

3.2.3 Block diagram(s) and circuit operation table. The block diagram(s) and circuit operation table shall be as specified on figure 2.

3.3 Electrical performance characteristics. Unless otherwise specified herein, the electrical performance characteristics are as specified in table I and shall apply over the full ambient operating temperature range.

3.4 Electrical test requirements. The electrical test requirements shall be the subgroups specified in table II. The electrical tests for each subgroup are described in table I.

3.5 Marking. Marking shall be in accordance with MIL-PRF-38535, appendix A. The part shall be marked with the PIN listed in 1.2 herein. In addition, the manufacturer's PIN may also be marked as listed in MIL-HDBK-103 (see 6.6 herein). For packages where marking of the entire SMD PIN number is not feasible due to space limitations, the manufacturer has the option of not marking the "5962-" on the device.

3.6 Certificate of compliance. A certificate of compliance shall be required from a manufacturer in order to be listed as an approved source of supply in MIL-HDBK-103 (see 6.6 herein). The certificate of compliance submitted to DSCC-VA prior to listing as an approved source of supply shall affirm that the manufacturer's product meets the requirements of MIL-PRF-38535, appendix A and the requirements herein.

3.7 Certificate of conformance. A certificate of conformance as required in MIL-PRF-38535, appendix A shall be provided with each lot of microcircuits delivered to this drawing.

3.8 Notification of change. Notification of change to DSCC-VA shall be required in accordance with MIL-PRF-38535, appendix A.

3.9 Verification and review. DSCC, DSCC's agent, and the acquiring activity retain the option to review the manufacturer's facility and applicable required documentation. Offshore documentation shall be made available onshore at the option of the reviewer.

TABLE I. Electrical performance characteristics.

Test	Symbol	Conditions 1/ $-55°C \le T_A \le +125°C$ unless otherwise specified	Group A subgroups	Device Type	Limits 2/		Unit
					Min	Max	
Power supply 3/	I_{DD}	V_{DD} = 1.5 V	1,2,3	05		200	µA
		V_{DD} = 5.0 V		01		700	
				02		1.4	mA
				03		300	µA
				04		400	
				05		300	
		V_{DD} = 12 V		05		400	
		V_{DD} = 15 V		01		1000	
				02		2.0	mA
				03		300	µA
				04		600	
				05		600	
		V_{DD} = 18 V		03		350	
				04		700	
Trigger voltage	V_{TR}	V_{DD} = 1.5 V	1,2,3	05	0.4	0.6	V
		V_{DD} = 5.0 V		01-04	1.26	2.06	
				05	1.30	2.00	
		V_{DD} = 12.0 V		05	3.70	4.30	
		V_{DD} = 15.0 V		01-04	4.05	5.50	
		V_{DD} = 18.0 V		03-04	4.70	6.85	
Reset voltage level	V_{RESET}		1	01	0.4	1.5	V
			2,3		0.3	1.8	

See footnotes at end of table.

TABLE I. Electrical performance characteristics - Continued.

Test	Symbol	Conditions 1/ $-55°C \le T_A \le +125°C$ unless otherwise specified	Group A subgroups	Device Type	Limits 2/		Unit
					Min	Max	
Trigger current 3/	I_{TR}	V_{DD} = 1.5 V, T_A = +25°C, +125°C	1,2	05		±50	nA
		V_{DD} = 5.0 V, T_A = +25°C, +125°C		03-05		±50	
		V_{DD} = 12.0 V, T_A = +25°C, +125°C		05		±50	
		V_{DD} = 15.0 V, T_A = +25°C, +125°C		03,04		±100	
		V_{DD} = 18.0 V, T_A = +25°C, +125°C		03,04		±100	
Threshold voltage	V_{TH}	V_{DD} = 1.5 V	1,2,3	05	0.70	1.90	V
		V_{DD} = 5.0 V		All	2.70	3.90	
		V_{DD} = 12 V		05	7.30	8.70	
		V_{DD} = 15.0 V		01-04	9.15	10.80	
		V_{DD} = 18.0 V		03-04	10.90	13.15	
Threshold current 3/	I_{TH}	V_{DD} = 1.5 V, T_A = +25°C, +125°C	1,2	05		±50	nA
		V_{DD} = 5.0 V, T_A = +25°C, +125°C		03-05		±50	
		V_{DD} = 12.0 V, T_A = +25°C, +125°C		05		±50	
		V_{DD} = 15.0 V, T_A = +25°C, +125°C		03,04		±100	
		V_{DD} = 18.0 V, T_A = +25°C, +125°C		03,04		±100	

See footnotes at end of table.

TABLE I. Electrical performance characteristics - Continued.

Test	Symbol	Conditions 1/ $-55°C \le T_A \le +125°C$ unless otherwise specified	Group A subgroups	Device Type	Limits 2/		Unit
					Min	Max	
High level output voltage	V_{OH}	V_{DD} = 5.0 V, I_{OH} = -1 mA	1,2,3	01,02	4.10		V
		V_{DD} = 15.0 V, I_{OH} = -10 mA		01,02	12.50		
		V_{DD} = 15.0 V, I_{OH} = -5 mA			13.50		
		V_{DD} = 15.0 V, I_{OH} = -1 mA			14.20		
		V_{DD} = 5.0 V, I_{OH} = -0.8 mA		03,04	3.80		
		V_{DD} = 15.0 V, I_{OH} = -0.8 mA			14.20		
		V_{DD} = 18.0 V, I_{OH} = -0.8 mA			17.30		
		V_{DD} = 1.5 V, I_{OH} = -0.25 mA		05	1.00	1.50	
		V_{DD} = 5.0 V, I_{OH} = -1.0 mA			4.20	5.00	
		V_{DD} = 12.0 V, I_{OH} = -10 mA			10.50	12.00	
		V_{DD} = 12.0 V, I_{OH} = -5 mA			10.70	12.00	
		V_{DD} = 12.0 V, I_{OH} = -1 mA			11.0	12.00	
Monostable timing accuracy	t_{MON}	5.0 V $\le V_{DD} \le$ 15 V, R_T = 10 kΩ, C_T = 0.1 µF, see figures 3 and 5	9	03,04	908	1110	µs
			10,11		858	1161	
		1.5 V $\le V_{DD} \le$ 12 V, R_T = 10 kΩ, C_T = 0.1 µF, see figures 3 and 5	9,10,11	05	900	1250	

See footnotes at end of table.

TABLE I. Electrical performance characteristics - Continued.

Test	Symbol	Conditions 1/ $-55°C \le T_A \le +125°C$ unless otherwise specified	Group A subgroups	Device Type	Limits 2/		Unit
					Min	Max	
Low level output voltage	V_{OL}	V_{DD} = 5.0 V, I_{OL} = 8.0 mA	1,2,3	01,02, 05		0.60	V
		V_{DD} = 5.0 V, I_{OL} = 5.0 mA				0.45	
		V_{DD} = 5.0 V, I_{OL} = 3.2 mA				0.40	
		V_{DD} = 15.0 V, I_{OL} = 100 mA		01,02		3.80	
		V_{DD} = 15.0 V, I_{OL} = 50 mA				1.50	
		V_{DD} = 15.0 V, I_{OL} = 10 mA				0.45	
		V_{DD} = 5.0 V, I_{OL} = 3.2 mA		03,04		0.50	
		V_{DD} = 15.0 V, I_{OL} = 20.0 mA				1.25	
		V_{DD} = 18.0 V, I_{OL} = 3.2 mA				0. 50	
		V_{DD} = 1.5 V, I_{OL} = 1.0 mA		05		0.40	
		V_{DD} = 12.0 V, I_{OL} = 75 mA				3.50	
		V_{DD} = 12.0 V, I_{OL} = 50 mA				2.00	
		V_{DD} = 12.0 V, I_{OL} = 10 mA				1.00	
Astable timing accuracy	t_{AST}	5.0 V $\le V_{DD} \le$ 15 V, R_{TA} = 10 kΩ, R_{TB} = 10 kΩ, C_T = 0.1 µF, see figures 4 and 6	9	03,04	1818	2222	µs
			10,11		1717	2323	
		V_{DD} = 12 V, R_{TA} = 1 kΩ, R_{TB} = 1 kΩ, C_T = 0.1 µF, see figures 4 and 6	9,10,11	05	178	250	
Discharge transistor leakage current	I_{CEX}	V_{DD} = 5.0 V, T_A = +25°C, +125°C	1,2	03,04		300	nA
		V_{DD} = 15.0 V, T_A = +25°C, +125°C				300	
		V_{DD} = 18.0 V, T_A = +25°C, +125°C				300	

See footnotes at end of table.

TABLE I. Electrical performance characteristics - Continued.

Test	Symbol	Conditions 1/ $-55°C \le T_A \le +125°C$ unless otherwise specified	Group A subgroups	Device Type	Limits 2/		Unit
					Min	Max	
Discharge transistor leakage current	I_{CEX}	V_{DD} = 1.5 V, T_A = +25°C, +125°C	1	05		100	nA
			2			1000	
		V_{DD} = 5.0 V, T_A = +25°C, +125°C	1			100	
			2			1000	
		V_{DD} = 12.0 V, T_A = +25°C, +125°C	1			100	
			2			1000	
Reset current 3/	I_R	V_{DD} = 5.0 V, T_A = +25°C, +125°C	1,2	All		±50	nA
		V_{DD} = 15.0 V, T_A = +25°C, +125°C		01-04		±100	
		V_{DD} = 18.0 V, T_A = +25°C, +125°C		03-04		±100	
		V_{DD} = 1.5 V and 5.0 V, T_A = +25°C, +125°C		05		±50	
		V_{DD} = 12.0 V, T_A = +25°C, +125°C				±50	
Discharge transistor saturation voltage	V_{SAT}	V_{DD} = 5.0 V, I_{OL} = 10 mA	1,2,3	01,02		0.60	V
		V_{DD} = 15.0 V, I_{OL} = 100 mA				1.80	
		V_{DD} = 5.0 V, I_{OL} = 10 mA		03,04		0.60	
		V_{DD} = 15.0 V, I_{OL} = 10 mA				0.60	
		V_{DD} = 18.0 V, I_{OL} = 10 mA				0.60	
		V_{DD} = 1.5 V, I_{OL} = 1.0 mA		05		150	mV
		V_{DD} = 5.0 V, I_{OL} = 10 mA				0.30	V
		V_{DD} = 12.0 V, I_{OL} = 25 mA				2.00	

1/ Each side of device types 02 and 04 are tested separately.
2/ The limiting terms "min" (minimum) and "max" (maximum) shall be considered to apply to magnitudes only. Negative current shall be defined as conventional current flow out of a device terminal.
3/ $1/3\ V_{DD} \le V_{IN} \le 2/3\ V_{DD}$.

Device types	01		02 and 04 see note 1	02	03 and 05
Case outlines	P	2	C	2	G and P see note 2
Terminal number	Terminal symbol				
1	GND	NC	DSCH1	NC	GND
2	$\overline{TRTG}$	GND	THRES1	DSCH1	$\overline{TRTG}$
3	OUT	NC	CONT1	THRES1	OUT
4	$\overline{RESET}$	NC	$\overline{RESET1}$	CONT1	$\overline{RESET}$
5	CONT	$\overline{TRTG}$	OUT1	NC	CONT
6	THRES	NC	$\overline{TRTG1}$	$\overline{RESET1}$	THRES
7	DSCH	OUT	GND	NC	DSCH
8	V_{DD}	NC	$\overline{TRTG2}$	OUT1	V_{DD}
9	---	NC	OUT2	$\overline{TRTG1}$	---
10	---	$\overline{RESET}$	$\overline{RESET2}$	GND	---
11	---	NC	CONT2	NC	---
12	---	CONT	THRES2	$\overline{TRTG2}$	---
13	---	NC	DSCH2	OUT2	---
14	---	NC	V_{DD}	$\overline{RESET2}$	---
15	---	THRES	---	NC	---
16	---	NC	---	CONT2	---
17	---	DSCH	---	NC	---
18	---	NC	---	THRES2	---
19	---	NC	---	DSCH2	---
20	---	V_{DD}	---	V_{DD}	---

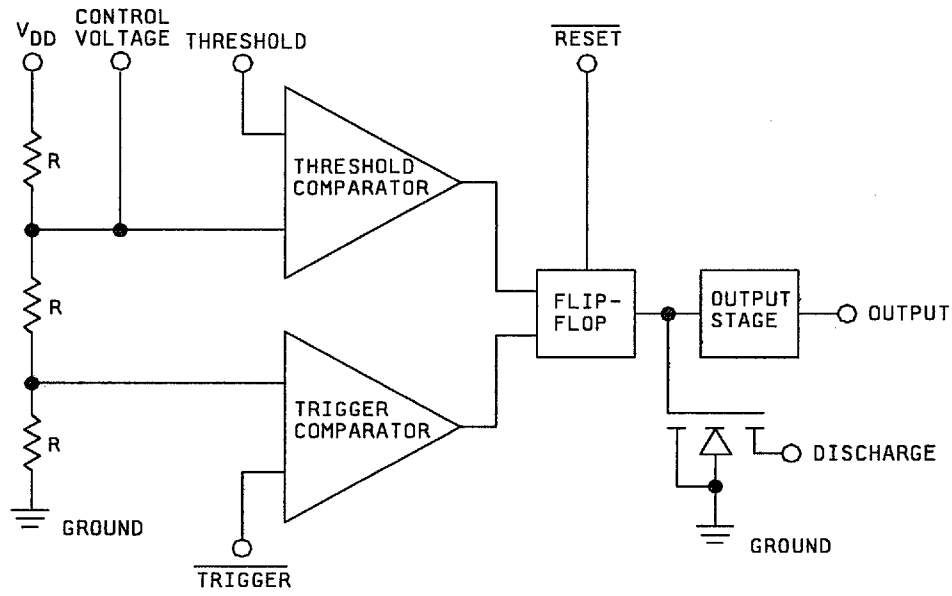
NOTES:
1. V_{DD} and GND are common to both sides.
2. V_{DD} and case are connected.

FIGURE 1. Terminal connections.

Device types 01 - 05

Threshold voltage	Trigger voltage	$\overline{\text{RESET}}$	Output	Discharge switch
Don't care	Don't care	Low	Low	On
> 2/3 (V_{DD})	> 1/3 (V_{DD})	High	Low	On
< 2/3 (V_{DD})	> 1/3 (V_{DD})	High	Stable	Stable
Don't care	< 1/3 (V_{DD})	High	High	Off

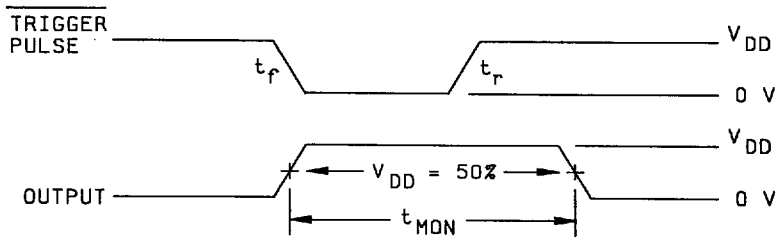
FIGURE 2. Block diagram and circuit operation table..



NOTE: 1 of 2 for device types 02 and 04.

FIGURE 2. Block diagram and circuit operation table - Continued.

Device types 03, 04, and 05



NOTE: $t_r = t_f \leq 10$ ns.

FIGURE 3. Timing parameter (monostable).

Device types 03, 04, and 05

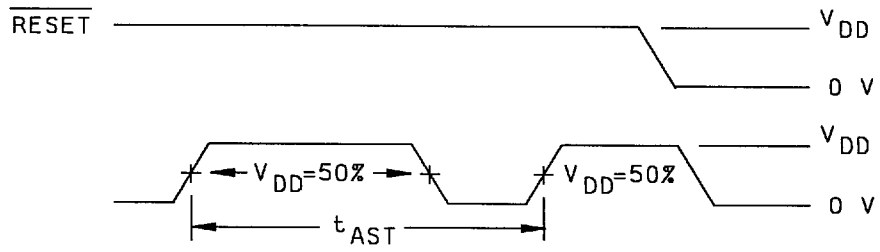


FIGURE 4. Timing parameter (astable).

Device types 03, 04, and 05

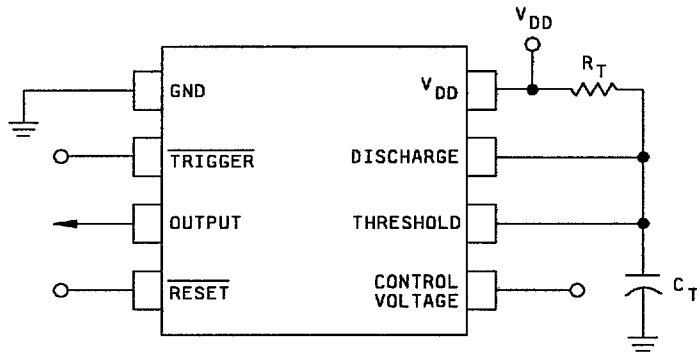


FIGURE 5. Monostable operation.

Device types 03, 04, and 05

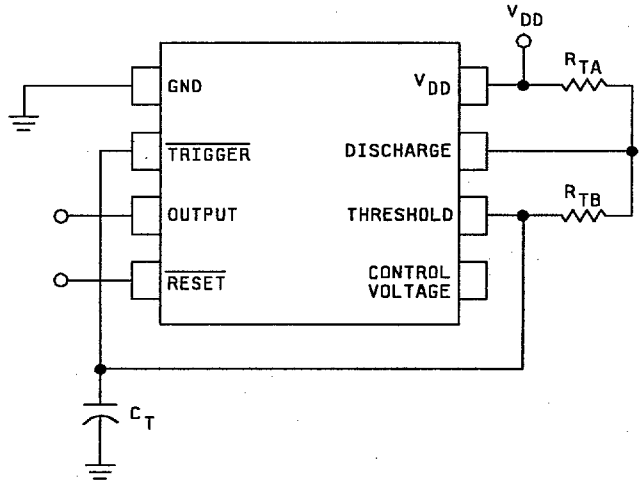


FIGURE 6. Astable operation.

4. QUALITY ASSURANCE PROVISIONS

4.1 Sampling and inspection. Sampling and inspection procedures shall be in accordance with MIL-PRF-38535, appendix A.

4.2 Screening. Screening shall be in accordance with method 5004 of MIL-STD-883, and shall be conducted on all devices prior to quality conformance inspection. The following additional criteria shall apply:

a. Burn-in test, method 1015 of MIL-STD-883.

(1) Test condition A, B, C, or D. The test circuit shall be maintained by the manufacturer under document revision level control and shall be made available to the preparing or acquiring activity upon request. The test circuit shall specify the inputs, outputs, biases, and power dissipation, as applicable, in accordance with the intent specified in test method 1015 of MIL-STD-883.

(2) T_A = +125°C, minimum.

b. Interim and final electrical test parameters shall be as specified in table II herein, except interim electrical parameter tests prior to burn-in are optional at the discretion of the manufacturer.

4.3 Quality conformance inspection. Quality conformance inspection shall be in accordance with method 5005 of MIL-STD-883 including groups A, B, C, and D inspections. The following additional criteria shall apply.

4.3.1 Group A inspection.

a. Tests shall be as specified in table II herein.

b. Subgroups 4, 5, 6, 7, and 8 in table I, method 5005 of MIL-STD-883 shall be omitted.

4.3.2 Groups C and D inspections.

a. End-point electrical parameters shall be as specified in table II herein.

b. Steady-state life test conditions, method 1005 of MIL-STD-883.

(1) Test condition A, B, C, or D. The test circuit shall be maintained by the manufacturer under document revision level control and shall be made available to the preparing or acquiring activity upon request. The test circuit shall specify the inputs, outputs, biases, and power dissipation, as applicable, in accordance with the intent specified in test method 1005 of MIL-STD-883.

(2) T_A = +125°C, minimum.

(3) Test duration: 1,000 hours, except as permitted by method 1005 of MIL-STD-883.

TABLE II. Electrical test requirements.

MIL-STD-883 test requirements	Subgroups (in accordance with MIL-STD-883, method 5005, table I)
Interim electrical parameters (method 5004)	---
Final electrical test parameters (method 5004)	1*, 2, 3, 9
Group A test requirements (method 5005)	1, 2, 3, 9, 10, 11
Groups C and D end-point electrical parameters (method 5005)	1

* PDA applies to subgroup 1.

5. PACKAGING

5.1 Packaging requirements. The requirements for packaging shall be in accordance with MIL-PRF-38535, appendix A.

6. NOTES

6.1 Intended use. Microcircuits conforming to this drawing are intended for use for Government microcircuit applications (original equipment), design applications, and logistics purposes.

6.2 Replaceability. Microcircuits covered by this drawing will replace the same generic device covered by a contractor-prepared specification or drawing.

6.3 Configuration control of SMD's. All proposed changes to existing SMD's will be coordinated with the users of record for the individual documents. This coordination will be accomplished in accordance with MIL-STD-973 using DD Form 1692, Engineering Change Proposal.

6.4 Record of users. Military and industrial users shall inform Defense Supply Center Columbus when a system application requires configuration control and the applicable SMD. DSCC will maintain a record of users and this list will be used for coordination and distribution of changes to the drawings. Users of drawings covering microelectronics devices (FSC 5962) should contact DSCC-VA, telephone (614) 692-0525.

6.5 Comments. Comments on this drawing should be directed to DSCC-VA, Columbus, Ohio 43216-5000, or telephone (614) 692-0674.

6.6 Approved sources of supply. Approved sources of supply are listed in MIL-HDBK-103. The vendors listed in MIL-HDBK-103 have agreed to this drawing and a certificate of compliance (see 3.6 herein) has been submitted to and accepted by DSCC-VA.

STANDARD MICROCIRCUIT DRAWING SOURCE APPROVAL BULLETIN

DATE: 98-01-06

Approved sources of supply for SMD 5962-89503 are listed below for immediate acquisition only and shall be added to MIL-HDBK-103 and QML-38535 during the next revision. MIL-HDBK-103 and QML-38535 will be revised to include the addition or deletion of sources. The vendors listed below have agreed to this drawing and a certificate of compliance has been submitted to and accepted by DSCC-VA. This bulletin is superseded by the next dated revision of MIL-HDBK-103 and QML-38535.

Standard microcircuit drawing PIN 1/	Vendor CAGE number	Vendor similar PIN 2/
5962-8950301PA	01295	TLC555MJGB
5962-89503012A	01295	TLC555MFKB
5962-8950302CA	01295	TLC556MJB
5962-89503022A	01295	TLC556MFKB
5962-8950303GC	34371	ICM7555MTV/883B
5962-8950303PA	3/	HI-7555CM-02
5962-8950304CA	34371	ICM7556MJD/883B
5962-8950305CA	3/	LMC555H/883
5962-8950305GA	27014 4/	LMC555H/883
5962-8950305PA	27014	LMC555J/883

1/ The lead finish shown for each PIN representing a hermetic package is the most readily available from the manufacturer listed for that part. If the desired lead finish is not listed, contact the vendor to determine its availability.
2/ Caution. Do not use this number for item acquisition. Items acquired to this number may not satisfy the performance requirements of this drawing.
3/ Not available from an approved source of supply.
4/ This device has an end-of-life date of 27 February 1998.

Vendor CAGE number	Vendor name and address
01295	Texas Instruments, Incorporated P.O. Box 655012 Dallas, TX 75265 Point of contact: I-20 at FM 1788 Midland, TX 79711-0448
27014	National Semiconductor 2900 Semiconductor Drive P.O. Box 58090 Santa Clara, CA 95052-8090
34371	Harris Semiconductor P.O. Box 883 Melbourne, FL 32902-0883