REVISIONS			
LTR	DESCRIPTION	DATE (YR-MO-DA)	APPROVED

REV																								
SHEET																								
REV																								
SHEET																								
REV STATUS OF SHEETS	REV																							
	SHEET	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15								

PMIC N/A

STANDARDIZED MILITARY DRAWING

THIS DRAWING IS AVAILABLE FOR USE BY ALL DEPARTMENTS AND AGENCIES OF THE DEPARTMENT OF DEFENSE

AMSC N/A

PREPARED BY
Rick C. Officer

CHECKED BY
Charles E. Besore

APPROVED BY

DRAWING APPROVAL DATE
13 DECEMBER 1989

REVISION LEVEL

DEFENSE ELECTRONICS SUPPLY CENTER
DAYTON, OHIO 45444

MICROCIRCUIT, LINEAR, 12-BIT CMOS, HIGH-SPEED A/D CONVERTER, MONOLITHIC SILICON

SIZE	CAGE CODE	
A	67268	5962-89655

SHEET 1

DESC FORM 193
SEP 87

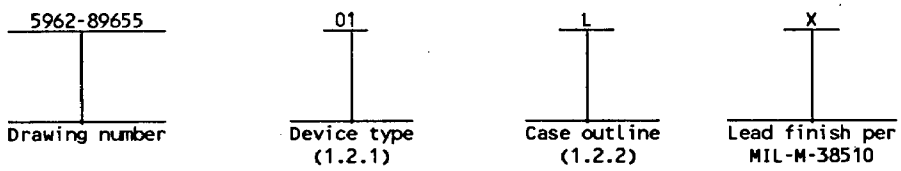
* U.S. GOVERNMENT PRINTING OFFICE: 1987 — 748-129/60911

5962-E1390

1. SCOPE

1.1 Scope. This drawing describes device requirements for class B microcircuits in accordance with 1.2.1 of MIL-STD-883, "Provisions for the use of MIL-STD-883 in conjunction with compliant non-JAN devices".

1.2 Part number. The complete part number shall be as shown in the following example:



1.2.1 Device types. The device types shall identify the circuit function as follows:

Device type	Generic number	Circuit function	Linearity	Conversion time (max)
01	AD7672TQ10	12-bit CMOS ADC	11-bit	10 µs
02	AD7672UQ10	12-bit CMOS ADC	12-bit	10 µs
03	AD7672TQ05	12-bit CMOS ADC	11-bit	5.0 µs
04	AD7672UQ05	12-bit CMOS ADC	12-bit	5.0 µs

1.2.2 Case outline. The case outline shall be as designated in appendix C of MIL-M-38510, and as follows:

Outline letter	Case outline
L	D-9 (24-lead, 1.280" x .310" x .200"), dual-in-line package

1.3 Absolute maximum ratings.

V_{DD} to DGND	-0.3 V dc to +7.0 V dc
V_{SS} to DGND	+0.3 V dc to -17 V dc
AGND to DGND	-0.3 V dc to V_{DD} +0.3 V dc
A_{IN1}, A_{IN2} to AGND	-15 V dc to +15 V dc
Digital input voltage to DGND: (CLK_{IN}, CS, RD)	-0.3 V dc to V_{DD} +0.3 V dc
Digital output voltage to DGND: (D_{B11}-D_{B0}, BUSY, CLK_{OUT})	-0.3 V dc to V_{DD} +0.3 V dc
Storage temperature range	-65°C to +150°C
Lead temperature (soldering, 10 seconds)	+300°C
Power dissipation (P_D) $T_A \leq 75°C$	1.0 W 1/
Thermal resistance, junction-to-case (Θ_{JC})	See MIL-M-38510, appendix C
Junction temperature (T_J)	+175°C

1/ Derate above T_A = +75°C at 10 mW/°C.

1.4 Recommended operating conditions.

Operating voltage range:	
Positive supply (V_{DD})	+4.75 V dc to +5.25 V dc
Negative supply (V_{SS})	-10.8 V dc to -13.2 V dc
Clock frequency (f_{CLK}):	
Device types 01 and 02	1.25 MHz
Device types 03 and 04	2.5 MHz
Reference input voltage	-5.0 V dc
Analog input voltage ranges (A_{IN})	
(applies to slow memory mode)	0 to +5.0 V dc,
	0 to + 10 V dc and ±5.0 V dc
Operating ambient temperature range (T_A)	-55°C to +125°C

2. APPLICABLE DOCUMENTS

2.1 Government specification, standard, and bulletin. Unless otherwise specified, the following specification, standard, and bulletin of the issue listed in that issue of the Department of Defense Index of Specifications and Standards specified in the solicitation, form a part of this drawing to the extent specified herein.

SPECIFICATION

MILITARY

MIL-M-38510 - Microcircuits, General Specification for.

STANDARD

MILITARY

MIL-STD-883 - Test Methods and Procedures for Microelectronics.

BULLETIN

MILITARY

MIL-BUL-103 - List of Standardized Military Drawings (SMD's).

(Copies of the specification, standard, and bulletin required by manufacturers in connection with specific acquisition functions should be obtained from the contracting activity or as directed by the contracting activity.)

2.2 Order of precedence. In the event of a conflict between the text of this drawing and the references cited herein, the text of this drawing shall take precedence.

3. REQUIREMENTS

3.1 Item requirements. The individual item requirements shall be in accordance with 1.2.1 of MIL-STD-883, "Provisions for the use of MIL-STD-883 in conjunction with compliant non-JAN devices" and as specified herein.

3.2 Design, construction, and physical dimensions. The design, construction, and physical dimensions shall be as specified in MIL-M-38510 and herein.

3.2.1 Terminal connections. The terminal connections shall be as specified on figure 1.

3.2.2 Case outline. The case outline shall be in accordance with 1.2.2 herein.

3.3 Electrical performance characteristics. Unless otherwise specified herein, the electrical performance characteristics are as specified in table I and apply over the full ambient operating temperature range.

3.4 Electrical test requirements. The electrical test requirements shall be the subgroups specified in table II. The electrical tests for each subgroup are described in table I.

3.5 Marking. Marking shall be in accordance with MIL-STD-883 (see 3.1 herein). The part shall be marked with the part number listed in 1.2 herein. In addition, the manufacturer's part number may also be marked as listed in MIL-BUL-103 (see 6.6 herein).

3.6 Certificate of compliance. A certificate of compliance shall be required from a manufacturer in order to be listed as an approved source of supply in MIL-BUL-103 (see 6.6 herein). The certificate of compliance submitted to DESC-ECS prior to listing as an approved source of supply shall affirm that the manufacturer's product meets the requirements of MIL-STD-883 (see 3.1 herein) and the requirements herein.

3.7 Certificate of conformance. A certificate of conformance as required in MIL-STD-883 (see 3.1 herein) shall be provided with each lot of microcircuits delivered to this drawing.

3.8 Notification of change. Notification of change to DESC-ECS shall be required in accordance with MIL-STD-883 (see 3.1 herein).

3.9 Verification and review. DESC, DESC's agent, and the acquiring activity retain the option to review the manufacturer's facility and applicable required documentation. Offshore documentation shall be made available onshore at the option of the reviewer.

TABLE I. Electrical performance characteristics.

Test	Symbol	Conditions 1/ $-55°C \le T_A \le +125°C$ unless otherwise specified		Device type	Group A subgroups	Limits Min	Limits Max	Unit
Digital input low voltage	V_{INL}	$\overline{CS}$, $\overline{RD}$, CLK_{IN}, V_{DD} = 4.75 V, V_{SS} = -12 V		All	1,2,3	0.8		V
Digital input high voltage	V_{INH}	$\overline{CS}$, $\overline{RD}$, CLK_{IN}, V_{DD} = 4.75, V_{SS} = -12 V		All	1,2,3	2.4		V
Analog input current (unipolar)	I_{IN1}	Input ranges = 0 V to 5.0 V or 0 V to 10 V		All	1,2,3		3.5	mA
Analog input current (bipolar)	I_{IN2}	Input range = ±5.0 V		All	1,2,3		±1.75	mA
Reference input current	I_{REF}	V_{DD} = 5.0 V, V_{SS} = -12 V		All	1,2,3	-3.0		µA
Digital input current	I_{IN}	V_{DD} = 5.25 V, V_{SS} = -12 V, A_{IN} = 0 to V_{DD}	$\overline{CS}$, $\overline{RD}$	All	1,2,3		±10	µA
			CLK_{IN}	All	1,2,3		±20	µA
Digital output low voltage	V_{OL}	D_{B11} - D_{B0}, $\overline{BUSY}$, CLK_{OUT} V_{DD} = 4.75 V, V_{SS} = -12 V, I_{SINK} = 1.6 mA		All	1,2,3		0.4	V
Digital output high voltage	V_{OH}	D_{B11} - D_{B0}, $\overline{BUSY}$, CLK_{OUT} V_{DD} = 4.75 V, V_{SS} = -12 V I_{SOURCE} = 200 µA		All	1,2,3	4.0		V
Floating state leakage current current	I_{LKG}	D_{B11} - D_{B0}, V_{SS} = 15 V, V_{DD} = 5.25 V		All	1,2,3		±10	µA
Integral linearity error	LE	V_{DD} = 5.0 V, V_{SS} = -12 V, Input range = ±5.0 V		01,03	1,2,3		±1.0	LSB
				02,04	1,2,3		±1.0	
				02,04	1,2,12		±0.5	

See footnotes at end of table.

TABLE I. Electrical performance characteristics - Continued.

Test	Symbol	Conditions 1/ $-55°C \le T_A \le +125°C$ unless otherwise specified	Device type	Group A subgroups	Limits Min	Limits Max	Unit
Differential linearity error	DLE	V_{DD} = 5.0 V, V_{SS} = -12 V	All	1,2,3		±0.9	LSB
Power supply current from V_{DD}	I_{DD}	$\overline{CS}$ = $\overline{RD}$ = $\overline{BUSY}$ = HIGH, V_{DD} = 5.25 V, V_{SS} = -13.2 V, A_{IN1} = 5.0 V = A_{IN2}	All	1,2,3		7.0	mA
Power supply current from V_{SS}	I_{SS}					-12	
Unipolar offset error	V_{OS}	V_{DD} = 5.0 V, V_{SS} = -12 V, Input range = 0 V to 5.0 V or 0 V to 10 V	All	1		±5.0	LSB
			01,03	2,3		±6.0	
			02,04			±4.0	
			02,04	12		±3.0	
Unipolar full scale error	AE	V_{DD} = 5.0 V, V_{SS} = -12 V, Input range = 0 V to 5.0 V or 0 V to 10 V	All	1		±5.0	LSB
			01,03	2,3		±7.0	
			02,04			±6.0	
			02,04	12		±3.0	
Bipolar zero error	B_{PZE}	V_{DD} = 5.0 V, V_{SS} = -12 V, Input range = ±5.0 V	All	1		±5.0	LSB
			01,03	2,3		±6.0	
			02,04			±4.0	
			02,04	12		±3.0	

See footnotes at end of table.

TABLE I. Electrical performance characteristics - Continued.

Test	Symbol	Conditions 1/ $-55°C \le T_A \le +125°C$ unless otherwise specified		Device type	Group A subgroups	Limits Min	Limits Max	Unit
Bipolar gain error	B_{PAE}	V_{DD} = 5.0 V, V_{SS} = -12 V, Input range = ±5.0 V		All	1		±5.0	LSB
				01,03	2,3		±7.0	
				02,04			±6.0	
				02,04	12		±4.0	
Digital input capacitance 2/	C_{IN}	$\overline{CS}$, $\overline{RD}$, CLK_{IN}, V_{DD} = 4.75, V_{SS} = -12 V, T_A = +25°C		All	4		10	pF
Floating state output capacitance 2/	C_{OUT}	T_A = +25°C		All	4		15	pF
Conversion time using synchronous clock	t_{CONV1}	See figures 2,3		01,02	9,10,11		10	µs
				03,04			5.0	
Conversion time using asynchronous clock	t_{CONV2}	1/		01,02	9,10,11	9.6	10.4	
				03,04		4.8	5.2	
$\overline{CS}$ to $\overline{RD}$ setup time	t_1	See figures 4,5 3/		All	9,10,11	0		ns
$\overline{RD}$ to $\overline{BUSY}$ propagation delay	t_2	See figures 2,3 3/		All	9		190	ns
					10,11		270	
Data access time after $\overline{RD}$	t_3	See figures 2,3,4 4/	C_L = 60 pF	All	9		110	ns
					10,11		150	
			C_L = 100 pF	All	9		125	ns
					10,11		170	

See footnotes at end of table.

TABLE I. Electrical performance characteristics - Continued.

Test	Symbol	Conditions 1/ $-55°C \le T_A \le +125°C$ unless otherwise specified	Device type	Group A subgroups	Limits		Unit
					Min	Max	
$\overline{RD}$ pulse width	t_4	See figures 2,3 3/	All	9,10,11	t_3		ns
$\overline{CS}$ to $\overline{RD}$ hold time	t_5	See figures 2,3 3/	All	9,10,11	0		ns
Data setup time after $\overline{BUSY}$	t_6	C_L = 60 pF, See figures 2,3,4 3/ 4/	All	9		70	ns
				10,11		100	
Bus relinquish time	t_7	See figures 2,3,5 5/	All	9	28	83	ns
				10,11	20	90	
Delay between successive read operations	t_8	3/	All	9,10,11	200		ns

1/ Conversion time using asynchronous clock is measured by setting the clock frequency at the appropriate value (see 1.4) and checking all remaining tested specifications.

2/ If not tested, shall be guaranteed to the limits specified in table I.

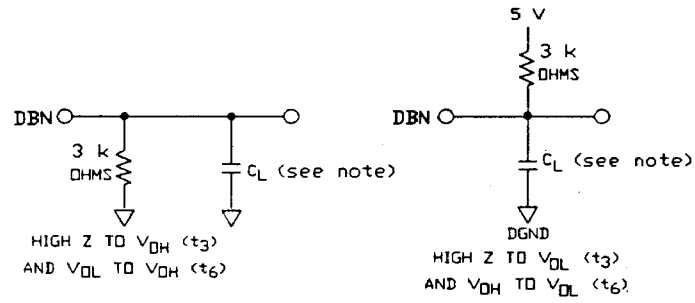
3/ All input control signals are specified with $t_r = t_f = 5$ ns (10% to 90% of +5.0 V) and timed from a voltage level of 1.6 V. Time t_6 and t_8 are measured only for the initial test and after process or design changes which may affect switching parameters.

4/ Time t_3 and t_6 are measured with the load circuits of figure 4 and defined as the time required for an output to cross 0.8 V or 2.4 V.

5/ Time t_7 is defined as the time required for the data lines to change 0.5 V when loaded with the circuits of figure 5. t_7 is tested at +25°C, with C_L = 60 pF.

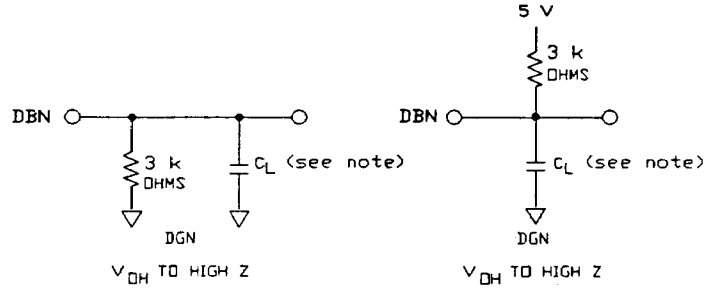
Device types	01,02,03, and 04
Case outline	L
Terminal number	Terminal symbol
1	A_{IN1}
2	V_{REF}
3	AGND
4	D_{B11} (MSB)
5	D_{B10}
6	D_{B9}
7	D_{B8}
8	D_{B7}
9	D_{B6}
10	D_{B5}
11	D_{B4}
12	DGND
13	D_{B3}
14	D_{B2}
15	D_{B1}
16	D_{B0} (LSB)
17	CLK_{IN}
18	$\overline{CLK}_{OUT}$
19	$\overline{RD}$
20	$\overline{CS}$
21	$\overline{BUSY}$
22	V_{SS}
23	V_{DD}
24	A_{IN2}

FIGURE 1. Terminal connections.



NOTE: C_L = Load capacitance and includes scope and jig capacitance.

FIGURE 2. Load circuit for access time.



NOTE: C_L = Load capacitance and includes scope and jig capacitance.

FIGURE 3. Load circuit for bus relinquish time.

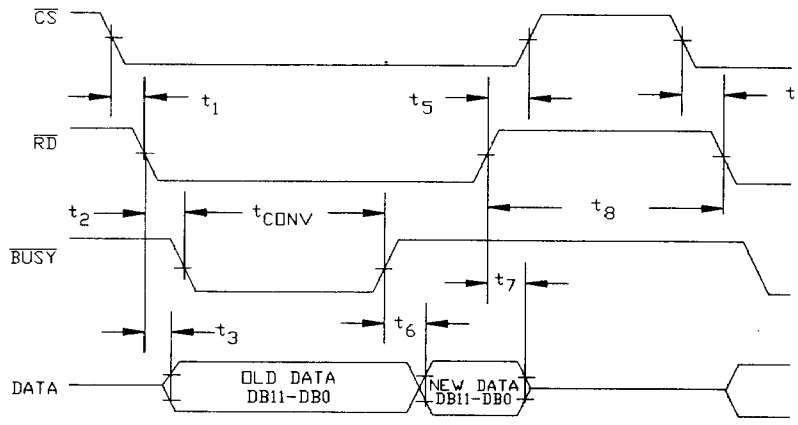


FIGURE 4. Slow memory mode timing diagram.

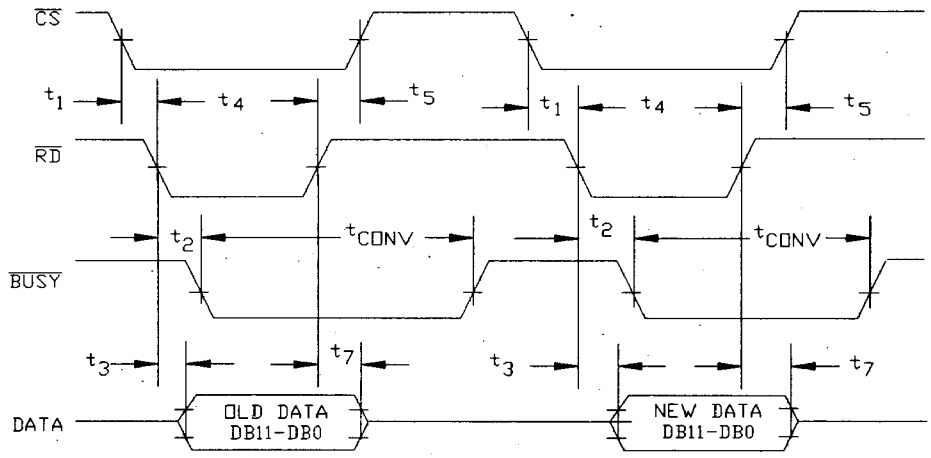


FIGURE 5. ROM mode timing diagram.

4. QUALITY ASSURANCE PROVISIONS

4.1 Sampling and inspection. Sampling and inspection procedures shall be in accordance with section 4 of MIL-M-38510 to the extent specified in MIL-STD-883 (see 3.1 herein).

4.2 Screening. Screening shall be in accordance with method 5004 of MIL-STD-883, and shall be conducted on all devices prior to quality conformance inspection. The following additional criteria shall apply:

a. Burn-in test, method 1015 of MIL-STD-883.

(1) Test condition A, B, C, or D using the circuit submitted with the certificate of compliance (see 3.6 herein).

(2) T_A = +125°C, minimum.

b. Interim and final electrical test parameters shall be as specified in table II herein, except interim electrical parameter tests prior to burn-in are optional at the discretion of the manufacturer.

c. Subgroup 12 test is used for grading and part selection at T_A = +25°C and is not included in PDA calculations.

4.3 Quality conformance inspection. Quality conformance inspection shall be in accordance with method 5005 of MIL-STD-883 including groups A, B, C, and D inspections. The following additional criteria shall apply.

4.3.1 Group A inspection.

a. Tests shall be as specified in table II herein.

b. Subgroups 5, 6, 7, and 8 in table I, method 5005 of MIL-STD-883 shall be omitted.

c. Subgroup 4 (C_{IN} and C_{OUT} measurements) shall be measured only for the initial test and after process or design changes which may affect capacitance. A minimum sample size of 15 devices with zero rejects shall be required.

d. Subgroup 12 test is used for grading and part selection at T_A = +25°C and is not included in PDA calculations.

4.3.2 Groups C and D inspections.

a. End-point electrical parameters shall be as specified in table II herein.

b. Steady-state life test conditions, method 1005 of MIL-STD-883.

(1) Test condition A, B, C, or D using the circuit submitted with the certificate of compliance (see 3.6 herein).

(2) T_A = +125°C, minimum.

(3) Test duration: 1,000 hours, except as permitted by method 1005 of MIL-STD-883.

TABLE II. Electrical test requirements.

MIL-STD-883 test requirements	Subgroups (per method 5005, table I)
Interim electrical parameters (method 5004)	1
Final electrical test parameters (method 5004)	1*,2,3,12
Group A test requirements (method 5005)	1,2,3,4,9,10**, 11**,12
Groups C and D end-point electrical parameters (method 5005)	1

* PDA applies to subgroup 1.
** Subgroups 10 and 11, if not tested, shall be guaranteed to the limits specified in table I.

5. PACKAGING

5.1 Packaging requirements. The requirements for packaging shall be in accordance with MIL-M-38510.

6. NOTES

6.1 Intended use. Microcircuits conforming to this drawing are intended for use when military specifications do not exist and qualified military devices that will perform the required function are not available for OEM application. When a military specification exists and the product covered by this drawing has been qualified for listing on QPL-38510, the device specified herein will be inactivated and will not be used for new design. The QPL-38510 product shall be the preferred item for all applications.

6.2 Replaceability. Microcircuits covered by this drawing will replace the same generic device covered by a contractor-prepared specification or drawing.

6.3 Configuration control of SMD's. All proposed changes to existing SMD's will be coordinated with the users of record for the individual documents. This coordination will be accomplished in accordance with MIL-STD-481 using DD Form 1693, Engineering Change Proposal (Short Form).

6.4 Record of users. Military and industrial users shall inform Defense Electronics Supply Center when a system application requires configuration control and the applicable SMD. DESC will maintain a record of users and this list will be used for coordination and distribution of changes to the drawings. Users of drawings covering microelectronics devices (FSC 5962) should contact DESC-ECS, telephone (513) 296-6022.

6.5 Comments. Comments on this drawing should be directed to DESC-ECS, Dayton, Ohio 45444, or telephone (513) 296-5375.

6.6 Approved source of supply. An approved source of supply is listed MIL-BUL-103. Additional sources will be added to MIL-BUL-103 as they become available. The vendor listed in MIL-BUL-103 has agreed to this drawing and a certificate of compliance (see 3.6 herein) has been submitted to and accepted by DESC-ECS. The approved source of supply listed below is for information purposes only and is current only to the date of the last action of this document.

Military drawing part number	Vendor CAGE number	Vendor similar part number 1/
5962-8965501LX	24355	AD7672TQ10/883B
5962-8965502LX	24355	AD7672UQ10/883B
5962-8965503LX	24355	AD7672TQ05/883B
5962-8965504LX	24355	AD7672UQ05/883B

1/ Caution. Do not use this number for item acquisition. Items acquired by this number may not satisfy the performance requirements of this drawing.

Vendor CAGE number	Vendor name and address
24355	Analog Devices One Technology Way Norwood, MA 02062-9106