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PMIC N/A  <b>STANDARDIZED MILITARY DRAWING</b>  THIS DRAWING IS AVAILABLE FOR USE BY ALL DEPARTMENTS AND AGENCIES OF THE DEPARTMENT OF DEFENSE  AMSC N/A	PREPARED BY <i>Larry T. Handen</i> CHECKED BY <i>Tim H. Noh</i> APPROVED BY <i>DMC</i>	DEFENSE ELECTRONICS SUPPLY CENTER DAYTON, OHIO 45444  MICROCIRCUITS, DIGITAL, BIPOLAR, ADVANCED SCHOTTKY TTL, TRANSCEIVERS/REGISTERS, MONOLITHIC SILICON			
	DRAWING APPROVAL DATE 4 DECEMBER 1989  REVISION LEVEL	<table style="width: 100%;"> <tr> <td style="width: 15%;">SIZE <b>A</b></td> <td style="width: 35%;">CAGE CODE <b>67268</b></td> <td style="width: 50%;"><b>5962-89754</b></td> </tr> </table>	SIZE <b>A</b>	CAGE CODE <b>67268</b>	<b>5962-89754</b>
SIZE <b>A</b>	CAGE CODE <b>67268</b>	<b>5962-89754</b>			
		SHEET 1			

DESC FORM 193  
SEP 87

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## 1. SCOPE

1.1 Scope. This drawing describes device requirements for class B microcircuits in accordance with 1.2.1 of MIL-STD-883, "Provisions for the use of MIL-STD-883 in conjunction with compliant non-JAN devices".

1.2 Part number. The complete part number shall be as shown in the following example:

5962-89754	01	K	X
┆	┆	┆	┆
┆	┆	┆	┆
┆	┆	┆	┆
Drawing number	Device type (1.2.1)	Case outline (1.2.2)	Lead finish per MIL-M-38510

1.2.1 Device types. The device types shall identify the circuit function as follows:

Device type	Generic number	Circuit function
01	54F646	Transceivers/registers
02	54F648	Transceivers/registers, inverted

1.2.2 Case outlines. The case outlines shall be as designated in appendix C of MIL-M-38510, and as follows:

Outline letter	Case outline
K	F-6 (24-lead, .640" x .420" x .090"), flat package
L	D-9 (24-lead, 1.280" x .310" x .200"), dual-in-line package
3	C-4 (28-terminal, .460" x .460" x .100"), square chip carrier package

## 1.3 Absolute maximum ratings.

Supply voltage range	- - - - -	-0.5 V dc to +7.0 V dc
Input voltage range	- - - - -	-0.5 V dc to +7.0 V dc
Input current range	- - - - -	-30 mA to +5.0 mA
Voltage applied to any output in the disabled state	- - - - -	-0.5 V dc to +5.5 V dc
Voltage applied to any output in the high state	- - - - -	-0.5 V dc to $V_{CC}$
Current into any output in the low state	- - - - -	96 mA
Maximum power dissipation ( $P_D$ ) <sup>1/</sup>	- - - - -	825 mW
Storage temperature range	- - - - -	-65°C to +150°C
Ambient temperature under bias	- - - - -	-55°C to +125°C
Lead temperature (soldering, 10 seconds)	- - - - -	+300°C
Junction temperature ( $T_J$ )	- - - - -	175°C
Thermal resistance, junction-to-case ( $\theta_{JC}$ )	- - - - -	See MIL-M-38510, appendix C

<sup>1/</sup> Must withstand the added  $P_D$  due to short circuit test, e.g.,  $I_{OS}$ .

<b>STANDARDIZED MILITARY DRAWING</b> DEFENSE ELECTRONICS SUPPLY CENTER DAYTON, OHIO 45444	SIZE <b>A</b>	5962-89754	
		REVISION LEVEL	SHEET 2

#### 1.4 Recommended operating conditions.

Supply voltage range ( $V_{CC}$ )	- - - - -	+4.5 V dc minimum to +5.5 V dc maximum
Minimum high level input voltage ( $V_{IH}$ )	- - - - -	2.0 V dc
Maximum low level input voltage ( $V_{IL}$ )	- - - - -	0.8 V dc
Maximum input clamp current ( $I_{IC}$ )	- - - - -	-18 mA
Maximum high level output current ( $I_{OH}$ )	- - - - -	-12 mA
Maximum low level output current ( $I_{OL}$ )	- - - - -	48 mA
Case operating temperature range ( $T_C$ )	- - - - -	-55°C to +125°C
Setup time $A_n$ , $B_n$ , $\bar{A}_n$ , $\bar{B}_n$ to CPAB, CPBA ( $t_s$ )	- - - - -	5.0 ns
Hold time $A_n$ , $B_n$ , $\bar{A}_n$ , $\bar{B}_n$ to CPAB, CPBA ( $t_h$ ):		
$T_C = +25^\circ\text{C}$	- - - - -	1.5 ns
$T_C = -55^\circ\text{C}, +125^\circ\text{C}$	- - - - -	2.5 ns
Pulse width CPAB, CPBA	- - - - -	5.0 ns
Maximum clock frequency ( $f_{MAX}$ ):		
$T_C = +25^\circ\text{C}$	- - - - -	90 MHz
$T_C = -55^\circ\text{C}, +125^\circ\text{C}$	- - - - -	75 MHz

#### 2. APPLICABLE DOCUMENTS

2.1 Government specification, standard, and bulletin. Unless otherwise specified, the following specification, standard, and bulletin of the issue listed in that issue of the Department of Defense Index of Specifications and Standards specified in the solicitation, form a part of this drawing to the extent specified herein.

##### SPECIFICATION

###### MILITARY

MIL-M-38510 - Microcircuits, General Specification for.

##### STANDARD

###### MILITARY

MIL-STD-883 - Test Methods and Procedures for Microelectronics.

##### BULLETIN

###### MILITARY

MIL-BUL-103 - List of Standardized Military Drawings (SMD's).

(Copies of the specification, standard, and bulletin required by manufacturers in connection with specific acquisition functions should be obtained from the contracting activity or as directed by the contracting activity.)

2.2 Order of precedence. In the event of a conflict between the text of this drawing and the references cited herein, the text of this drawing shall take precedence.

#### 3. REQUIREMENTS

3.1 Item requirements. The individual item requirements shall be in accordance with 1.2.1 of MIL-STD-883, "Provisions for the use of MIL-STD-883 in conjunction with compliant non-JAN devices" and as specified herein.

3.2 Design, construction, and physical dimensions. The design, construction, and physical dimensions shall be as specified in MIL-M-38510 and herein.

<b>STANDARDIZED MILITARY DRAWING</b> DEFENSE ELECTRONICS SUPPLY CENTER DAYTON, OHIO 45444	SIZE <b>A</b>		5962-89754
		REVISION LEVEL	SHEET 3

- 3.2.1 Terminal connections. The terminal connections shall be as specified on figure 1.
- 3.2.2 Truth tables. The truth tables shall be as specified on figure 2.
- 3.2.3 Logic diagrams. The logic diagrams shall be as specified on figure 3.
- 3.2.4 Test circuit and switching waveforms. The test circuit and switching waveforms shall be as specified on figure 4.
- 3.2.5 Case outlines. The case outlines shall be in accordance with 1.2.2 herein.
- 3.3 Electrical performance characteristics. Unless otherwise specified herein, the electrical performance characteristics are as specified in table I and apply over the full case operating temperature range.
- 3.4 Electrical test requirements. The electrical test requirements shall be the subgroups specified in table II. The electrical tests for each subgroup are described in table I.
- 3.5 Marking. Marking shall be in accordance with MIL-STD-883 (see 3.1 herein). The part shall be marked with the part number listed in 1.2 herein. In addition, the manufacturer's part number may also be marked as listed in MIL-BUL-103 (see 6.6 herein).
- 3.6 Certificate of compliance. A certificate of compliance shall be required from a manufacturer in order to be listed as an approved source of supply in MIL-BUL-103 (see 6.6 herein). The certificate of compliance submitted to DESC-ECC prior to listing as an approved source of supply shall affirm that the manufacturer's product meets the requirements of MIL-STD-883 (see 3.1 herein) and the requirements herein.
- 3.7 Certificate of conformance. A certificate of conformance as required in MIL-STD-883 (see 3.1 herein) shall be provided with each lot of microcircuits delivered to this drawing.
- 3.8 Notification of change. Notification of change to DESC-ECC shall be required in accordance with MIL-STD-883 (see 3.1 herein).
- 3.9 Verification and review. DESC, DESC's agent, and the acquiring activity retain the option to review the manufacturer's facility and applicable required documentation. Offshore documentation shall be made available onshore at the option of the reviewer.
4. **QUALITY ASSURANCE PROVISIONS**
- 4.1 Sampling and inspection. Sampling and inspection procedures shall be in accordance with section 4 of MIL-M-38510 to the extent specified in MIL-STD-883 (see 3.1 herein).
- 4.2 Screening. Screening shall be in accordance with method 5004 of MIL-STD-883, and shall be conducted on all devices prior to quality conformance inspection. The following additional criteria shall apply:
- a. Burn-in test, method 1015 of MIL-STD-883.
    - (1) Test condition A, B, C, or D using the circuit submitted with the certificate of compliance (see 3.6 herein).
    - (2)  $T_A = +125^{\circ}\text{C}$ , minimum.
  - b. Interim and final electrical test parameters shall be as specified in table II herein, except interim electrical parameter tests prior to burn-in are optional at the discretion of the manufacturer.

<b>STANDARDIZED MILITARY DRAWING</b> DEFENSE ELECTRONICS SUPPLY CENTER DAYTON, OHIO 45444	SIZE <b>A</b>		5962-89754
		REVISION LEVEL	SHEET 4

TABLE I. Electrical performance characteristics.

Test	Symbol	Conditions -55°C < T <sub>C</sub> < +125°C unless otherwise specified		Device types	Group A subgroups	Limits		Unit
						Min	Max	
High level output voltage	V <sub>OH</sub>	V <sub>CC</sub> = 4.5 V V <sub>IH</sub> = 2.0 V V <sub>IL</sub> = 0.8 V	I <sub>OH</sub> = -12 mA	A11	1, 2, 3	2.0		V
Low level output voltage	V <sub>OL</sub>		I <sub>OL</sub> = 48 mA	A11	1, 2, 3		0.55	V
Input clamp voltage	V <sub>IC</sub>		I <sub>C</sub> = -18 mA	A11	1, 2, 3		-1.2	V
High level input current	I <sub>IH1</sub>	V <sub>CC</sub> = 5.5 V  1/	V <sub>IN</sub> = 2.7 V (non I/O pins)	A11	1, 2, 3		20	μA
	I <sub>IH2</sub>		V <sub>IN</sub> = 7.0 V				100	
	I <sub>IH3</sub>		V <sub>IN</sub> = 5.5 V (I/O pins)				1.0	mA
Low level input current	I <sub>IL</sub>	V <sub>CC</sub> = 5.5 V 1/ V <sub>IN</sub> = 0.5 V (non I/O pins)		A11	1, 2, 3		-0.6	mA
Short circuit output current	I <sub>OS</sub>	V <sub>CC</sub> = 5.5 V 2/ V <sub>OUT</sub> = 0.0 V		A11	1, 2, 3	-100	-225	mA
Off-state output current	I <sub>OZH</sub>	V <sub>CC</sub> = 5.5 V V <sub>IH</sub> = 2.0 V	V <sub>IN</sub> = 2.7 V	A11	1, 2, 3		70	μA
	I <sub>OZL</sub>		V <sub>IN</sub> = 0.5 V		1, 2, 3		-650	
Supply current	I <sub>CCH</sub>	V <sub>CC</sub> = 5.5 V		A11	1, 2, 3		135	mA
	I <sub>CCL</sub>				1, 2, 3		150	mA
	I <sub>CCZ</sub>				1, 2, 3		150	mA
Functional tests		See 4.3.1c		A11	7, 8			

See footnotes at end of table.

<b>STANDARDIZED MILITARY DRAWING</b> DEFENSE ELECTRONICS SUPPLY CENTER DAYTON, OHIO 45444	SIZE <b>A</b>		5962-89754
		REVISION LEVEL	SHEET 5

TABLE I. Electrical performance characteristics - Continued.

Test	Symbol	Conditions -55°C < T <sub>C</sub> < +125°C unless otherwise specified	Device types	Group A subgroups	Limits		Unit	
					Min	Max		
Propagation delay time, A <sub>n</sub> , B <sub>n</sub> to B <sub>n</sub> , A <sub>n</sub> or A <sub>n</sub> , B <sub>n</sub> to B <sub>n</sub> , A <sub>n</sub>	t <sub>PLH1</sub>	C <sub>L</sub> = 50 pF R <sub>1</sub> = 500Ω R <sub>2</sub> = 500Ω see figure 4	V <sub>CC</sub> = 5.0 V	A11	9	1	7	ns
			V <sub>CC</sub> = 4.5 V to 5.5 V	01	10, 11	1	8	
	02			1		9		
	t <sub>PHL1</sub>		V <sub>CC</sub> = 5.0 V	A11	9	1	6.5	
V <sub>CC</sub> = 4.5 V to 5.5 V			10, 11		1	8		
Propagation delay time, CPBA, CPAB to A <sub>n</sub> , B <sub>n</sub> , A <sub>n</sub> , B <sub>n</sub>	t <sub>PLH2</sub>		V <sub>CC</sub> = 5.0 V	A11	9	2	7	ns
			V <sub>CC</sub> = 4.5 V to 5.5 V		10, 11	2	8.5	
	t <sub>PHL2</sub>		V <sub>CC</sub> = 5.0 V	A11	9	2	8	
		V <sub>CC</sub> = 4.5 V to 5.5 V	10, 11		2	9.5		
Propagation delay time, SBA, SAB to A <sub>n</sub> , B <sub>n</sub> , A <sub>n</sub> , B <sub>n</sub>	t <sub>PLH3</sub>	V <sub>CC</sub> = 5.0 V	A11	9	2	8.5	ns	
		V <sub>CC</sub> = 4.5 V to 5.5 V		10, 11	2	11		
	t <sub>PHL3</sub>	V <sub>CC</sub> = 5.0 V	A11	9	2	8		
		V <sub>CC</sub> = 4.5 V to 5.5 V		10, 11	2	10		
Output enable time, OE to A <sub>n</sub> , B <sub>n</sub> , A <sub>n</sub> , B <sub>n</sub>	t <sub>pZH1</sub>	V <sub>CC</sub> = 5.0 V	A11	9	2	8.5	ns	
		V <sub>CC</sub> = 4.5 V to 5.5 V		10, 11	2	10		
	t <sub>pZL1</sub>	V <sub>CC</sub> = 5.0 V	A11	9	2	8.5		
		V <sub>CC</sub> = 4.5 V to 5.5 V		10, 11	2	10		

See footnotes at end of table.

<b>STANDARDIZED MILITARY DRAWING</b> DEFENSE ELECTRONICS SUPPLY CENTER DAYTON, OHIO 45444	SIZE <b>A</b>		5962-89754
		REVISION LEVEL	SHEET 6

TABLE I. Electrical performance characteristics - Continued.

Test	Symbol	Conditions -55°C < T <sub>C</sub> < +125°C unless otherwise specified	Device types	Group A subgroups	Limits		Unit	
					Min	Max		
Output enable time, DIR to An, Bn, $\overline{A}n$ , $\overline{B}n$	t <sub>PZH2</sub>	C <sub>L</sub> = 50 pF R <sub>1</sub> = 500Ω R <sub>2</sub> = 500Ω see figure 4	V <sub>CC</sub> = 5.0 V	A11	9	2	8.5	ns
			V <sub>CC</sub> = 4.5 V to 5.5 V	A11	10, 11	2	10	
	t <sub>PZL2</sub>		V <sub>CC</sub> = 5.0 V	A11	9	2	10	
			V <sub>CC</sub> = 4.5 V to 5.5 V	A11	10, 11	2	12	
Output disable time, OE to An, Bn, $\overline{A}n$ , $\overline{B}n$	t <sub>PHZ1</sub>	V <sub>CC</sub> = 5.0 V	A11	9	1	7.5	ns	
		V <sub>CC</sub> = 4.5 V to 5.5 V	A11	10, 11	1	9		
	t <sub>PLZ1</sub>	V <sub>CC</sub> = 5.0 V	A11	9	1	7.5		
		V <sub>CC</sub> = 4.5 V to 5.5 V	A11	10, 11	1	9		
Output disable time, DIR to An, Bn, $\overline{A}n$ , $\overline{B}n$	t <sub>PHZ2</sub>	V <sub>CC</sub> = 5.0 V	A11	9	1	7.5	ns	
		V <sub>CC</sub> = 4.5 V to 5.5 V	A11	10, 11	1	9		
	t <sub>PLZ2</sub>	V <sub>CC</sub> = 5.0 V	A11	9	1	10		
		V <sub>CC</sub> = 4.5 V to 5.5 V	A11	10, 11	1	12		

1/ For I/O ports, the parameters I<sub>IH</sub> and I<sub>IL</sub> include the off-state output current.

2/ Not more than one output will be shorted at one time and the duration of the short circuit condition shall not exceed one second.

<b>STANDARDIZED MILITARY DRAWING</b> DEFENSE ELECTRONICS SUPPLY CENTER DAYTON, OHIO 45444	SIZE <b>A</b>		5962-89754
		REVISION LEVEL	SHEET 7

Device types	01		02	
Case outlines	K and L	3	K and L	3
Terminal number	Terminal symbol		Terminal symbol	
1	CPAB	NC	CPAB	NC
2	SAB	CPAB	SAB	CPAB
3	DIR	SAB	DIR	SAB
4	A1	DIR	A1	DIR
5	A2	A1	A2	A1
6	A3	A2	A3	A2
7	A4	A3	A4	A3
8	A5	NC	A5	NC
9	A6	A4	A6	A4
10	A7	A5	A7	A5
11	A8	A6	A8	A6
12	GND	A7	GND	A7
13	B8	A8	B8	A8
14	B7	GND	B7	GND
15	B6	NC	B6	NC
16	B5	B8	B5	B8
17	B4	B7	B4	B7
18	B3	B6	B3	B6
19	B2	B5	B2	B5
20	B1	B4	B1	B4
21	OE	B3	OE	B3
22	SBA	NC	SBA	NC
23	CPBA	B2	CPBA	B2
24	VCC	B1	VCC	B1
25	---	OE	---	OE
26	---	SBA	---	SBA
27	---	CPBA	---	CPBA
28	---	VCC	---	VCC

NC = No connection

FIGURE 1. Terminal connections.

<b>STANDARDIZED MILITARY DRAWING</b> DEFENSE ELECTRONICS SUPPLY CENTER DAYTON, OHIO 45444	SIZE <b>A</b>		5962-89754
		REVISION LEVEL	SHEET 8



Device type 01

Inputs						Inputs/outputs <sup>1/</sup>		Operating mode
DIR	$\overline{OE}$	CPAB	CPBA	SAB	SBA	A <sub>0</sub> through A <sub>7</sub>	B <sub>0</sub> through B <sub>7</sub>	
X	H	H/L	H/L	X	X	Input	Input	Isolation
X	H			X	X	Input	Input	Store A and B data
L	L	X	X	X	L	Output	Input	Real time B data to A bus
L	L	X	X	X	H	Output	Input	Stored B data to A bus
H	L	X	X	L	X	Input	Output	Real time A data to B bus
H	L	H/L	X	H	X	Input	Output	Stored A data to B bus

Device type 02

Inputs						Inputs/outputs <sup>1/</sup>		Operating mode
DIR	$\overline{OE}$	CPAB	CPBA	SAB	SBA	$\overline{A_0}$ through $\overline{A_7}$	$\overline{B_0}$ through $\overline{B_7}$	
X	H	H/L	H/L	X	X	Input	Input	Isolation
X	H			X	X	Input	Input	Store A and B data
L	L	X	X	X	L	Output	Input	Real time $\overline{B}$ data to A bus
L	L	X	X	X	H	Output	Input	Stored $\overline{B}$ data to A bus
H	L	X	X	L	X	Input	Output	Real time $\overline{A}$ data to B bus
H	L	H/L	X	H	X	Input	Output	Stored $\overline{A}$ data to B bus

H = High voltage level  
 L = Low voltage level  
 X = Irrelevant  
 = Low to high clock transition  
 H/L = High or low voltage level

<sup>1/</sup> The data output functions may be enabled or disabled by various signals at  $\overline{OE}$  or DIR inputs. Data input functions are always enabled, i.e., data at the bus pins will be stored on every low to high transition on the clock inputs.

FIGURE 2. Truth tables.

<b>STANDARDIZED MILITARY DRAWING</b> DEFENSE ELECTRONICS SUPPLY CENTER DAYTON, OHIO 45444	SIZE <b>A</b>		5962-89754
		REVISION LEVEL	SHEET 9

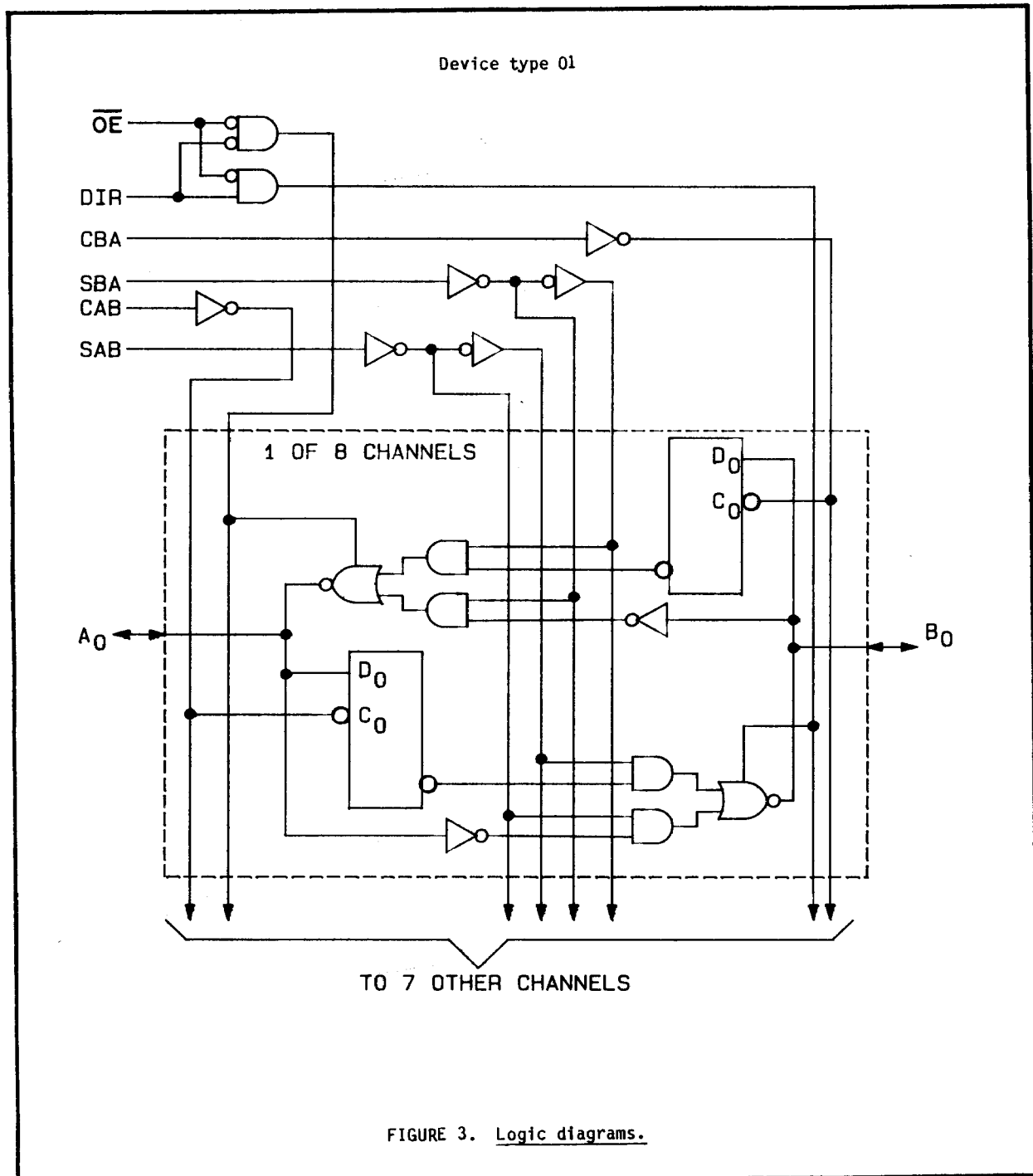


FIGURE 3. Logic diagrams.

<b>STANDARDIZED MILITARY DRAWING</b> DEFENSE ELECTRONICS SUPPLY CENTER DAYTON, OHIO 45444	SIZE <b>A</b>		5962-89754
		REVISION LEVEL	SHEET 10

Device type 02

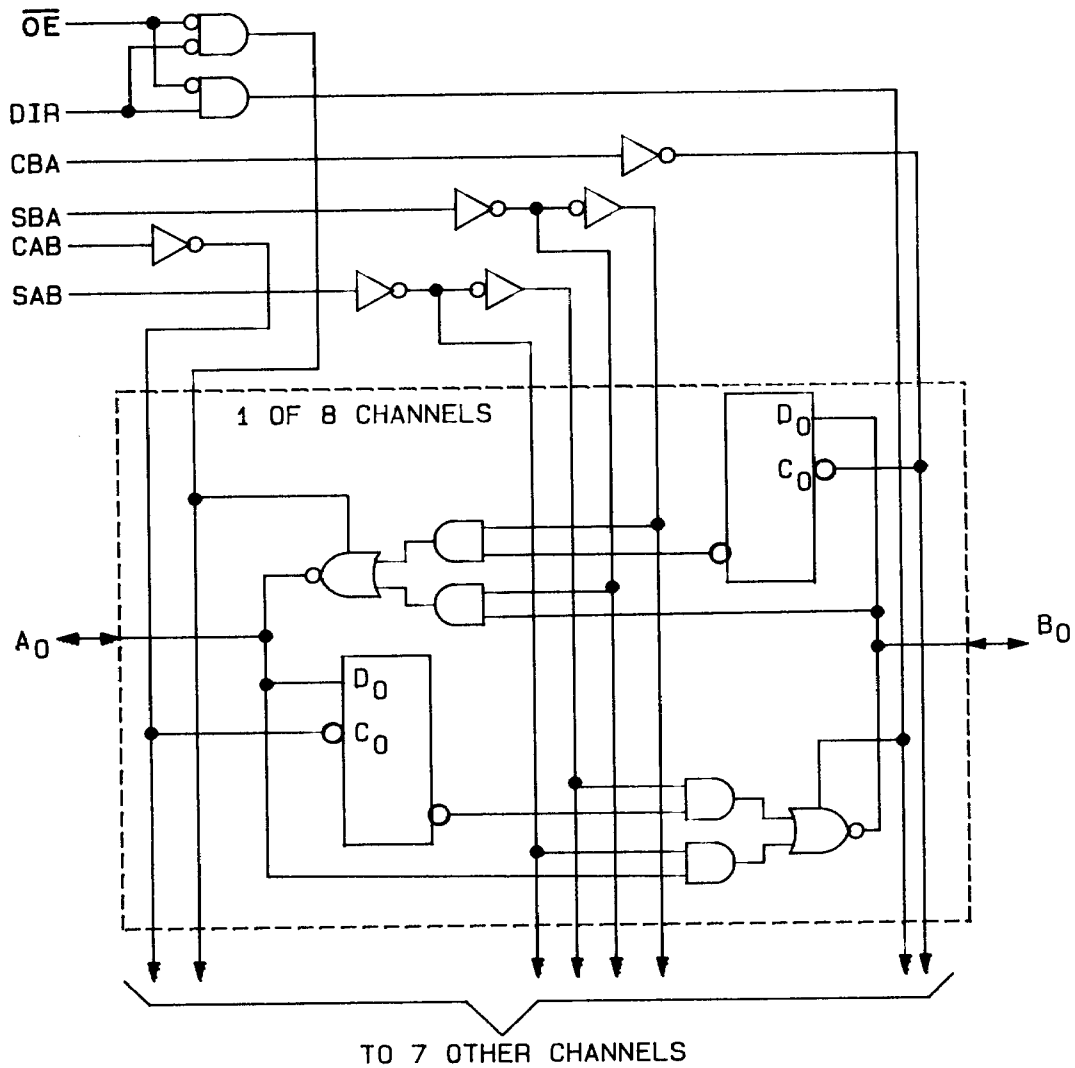


FIGURE 3. Logic diagrams - Continued.

<b>STANDARDIZED MILITARY DRAWING</b> DEFENSE ELECTRONICS SUPPLY CENTER DAYTON, OHIO 45444	SIZE <b>A</b>	5962-89754	
		REVISION LEVEL	SHEET 11

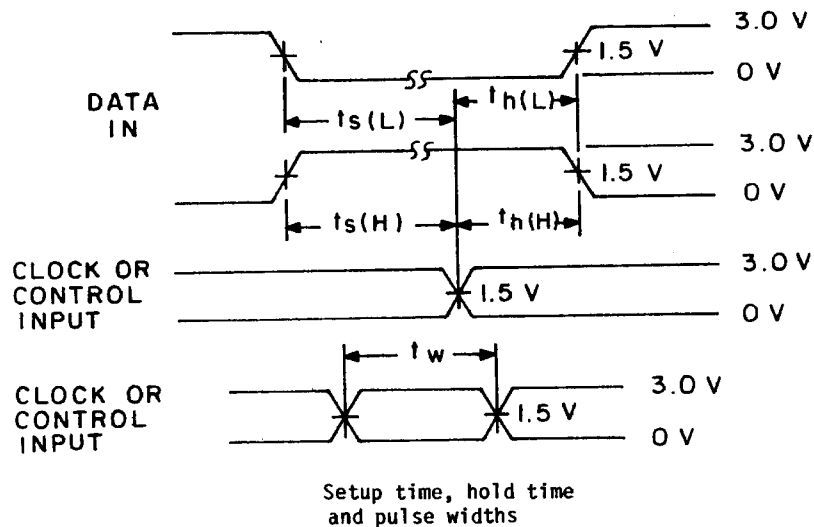
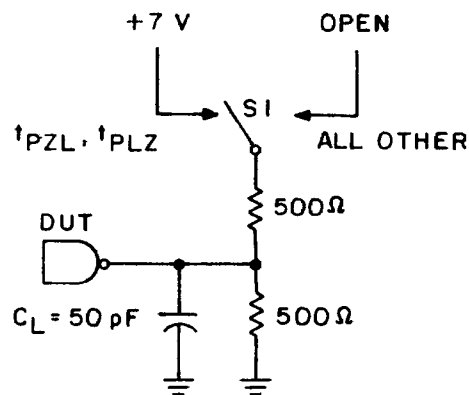
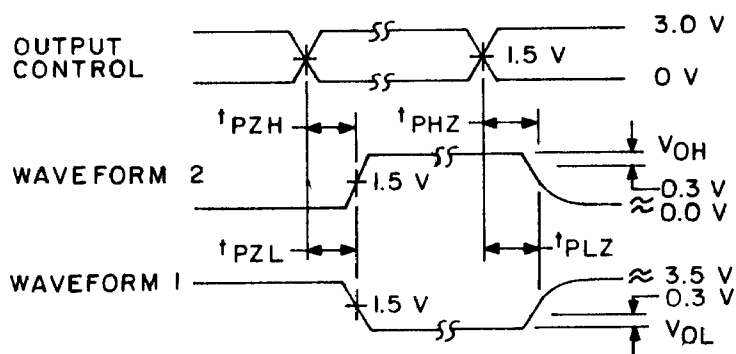
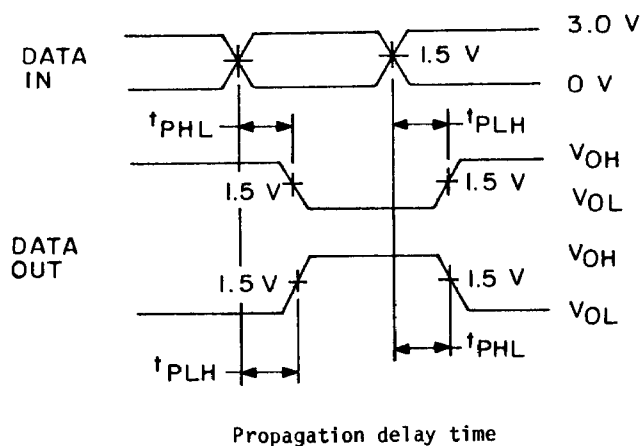


FIGURE 4. Test circuit and switching waveforms.

<b>STANDARDIZED MILITARY DRAWING</b> DEFENSE ELECTRONICS SUPPLY CENTER DAYTON, OHIO 45444	SIZE <b>A</b>	5962-89754	
	REVISION LEVEL		SHEET 12



**NOTES:**

1.  $C_L$  includes probe and jig capacitance.
2. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
3. All input pulses have the following characteristics: PRR = 1 MHz,  $t_r = t_f = 2.5$  ns, duty cycle = 50 percent.
4. When measuring propagation delay times of three-state outputs, switch S1 is open.
5. When measuring pulse widths  $t_r = t_f \leq 1$  ns.
6. The outputs are measured one at a time with one input transition per measurement.

FIGURE 4. Test circuit and switching waveforms - Continued.

<b>STANDARDIZED MILITARY DRAWING</b> DEFENSE ELECTRONICS SUPPLY CENTER DAYTON, OHIO 45444	SIZE <b>A</b>	5962-89754	
		REVISION LEVEL	SHEET 13

4.3 Quality conformance inspection. Quality conformance inspection shall be in accordance with method 5005 of MIL-STD-883 including groups A, B, C, and D inspections. The following additional criteria shall apply.

4.3.1 Group A inspection.

- a. Tests shall be as specified in table II herein.
- b. Subgroups 4, 5, and 6 in table I, method 5005 of MIL-STD-883 shall be omitted.
- c. Subgroups 7 and 8 tests shall verify the truth table as specified on figure 2 herein.

4.3.2 Groups C and D inspections.

- a. End-point electrical parameters shall be as specified in table II herein.
- b. Steady-state life test conditions, method 1005 of MIL-STD-883.
  - (1) Test condition A, B, C, or D using the circuit submitted with the certificate of compliance (see 3.6 herein).
  - (2)  $T_A = +125^{\circ}\text{C}$ , minimum.
  - (3) Test duration: 1,000 hours, except as permitted by method 1005 of MIL-STD-883.

TABLE II. Electrical test requirements.

MIL-STD-883 test requirements	Subgroups (per method 5005, table I)
Interim electrical parameters (method 5004)	---
Final electrical test parameters (method 5004)	1*, 2, 3, 7, 8, 9
Group A test requirements (method 5005)	1, 2, 3, 7, 8, 9, 10, 11
Groups C and D end-point electrical parameters (method 5005)	1, 2, 3

\*PDA applies to subgroup 1.

<b>STANDARDIZED MILITARY DRAWING</b> DEFENSE ELECTRONICS SUPPLY CENTER DAYTON, OHIO 45444	SIZE <b>A</b>		5962-89754
		REVISION LEVEL	SHEET 14

## 5. PACKAGING

5.1 Packaging requirements. The requirements for packaging shall be in accordance with MIL-M-38510.

## 6. NOTES

6.1 Intended use. Microcircuits conforming to this drawing are intended for use when military specifications do not exist and qualified military devices that will perform the required function are not available for OEM application. When a military specification exists and the product covered by this drawing has been qualified for listing on QPL-38510, the device specified herein will be inactivated and will not be used for new design. The QPL-38510 product shall be the preferred item for all applications.

6.2 Replaceability. Microcircuits covered by this drawing will replace the same generic device covered by a contractor-prepared specification or drawing.

6.3 Configuration control of SMD's. All proposed changes to existing SMD's will be coordinated with the users of record for the individual documents. This coordination will be accomplished in accordance with MIL-STD-481 using DD Form 1693, Engineering Change Proposal (Short Form).

6.4 Record of users. Military and industrial users shall inform Defense Electronics Supply Center when a system application requires configuration control and the applicable SMD. DESC will maintain a record of users and this list will be used for coordination and distribution of changes to the drawings. Users of drawings covering microelectronics devices (FSC 5962) should contact DESC-ECC, telephone (513) 296-6022.

6.5 Comments. Comments on this drawing should be directed to DESC-ECC, Dayton, Ohio 45444, or telephone (513) 296-8525.

<b>STANDARDIZED MILITARY DRAWING</b> DEFENSE ELECTRONICS SUPPLY CENTER DAYTON, OHIO 45444	SIZE <b>A</b>		5962-89754
		REVISION LEVEL	SHEET 15

6.6 Approved source of supply. An approved source of supply is listed in MIL-BUL-103. Additional sources will be added to MIL-BUL-103 as they become available. The vendor listed in MIL-BUL-103 has agreed to this drawing and a certificate of compliance (see 3.6 herein) has been submitted to and accepted by DESC-ECC. The approved source of supply listed below is for information purposes only and is current only to the date of the last action of this document.

Military drawing part number	Vendor CAGE number	Vendor similar part number <u>1/</u>
5962-8975401KX	27014	54F646FMQB
5962-8975401LX	27014	54F646SDMQB
5962-89754013X	27014	54F646LMQB
5962-8975402KX	27014	54F648FMQB
5962-8975402LX	27014	54F648SDMQB
5962-89754023X	27014	54F648LMQB

1/ Caution. Do not use this number for item acquisition. Items acquired to this number may not satisfy the performance requirements of this drawing.

Vendor CAGE  
number

27014

Vendor name  
and address

National Semiconductor Corporation  
2900 Semiconductor Drive  
Santa Clara, CA 95052  
Point of contact: 333 Western Avenue  
South Portland, ME 04106

<b>STANDARDIZED MILITARY DRAWING</b> DEFENSE ELECTRONICS SUPPLY CENTER DAYTON, OHIO 45444	SIZE <b>A</b>	5962-89754	
		REVISION LEVEL	SHEET 16

DESC FORM 193A  
SEP 87

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