

REVISIONS

LTR	DESCRIPTION	DATE (YR-MO-DA)	APPROVED
B	Add device types 02, 03, and 04. Changes in table I and figure 1. Editorial changes throughout.	93-05-26	M. A. Frye

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REV STATUS OF SHEETS				REV	B	B	B	B	B	B	B	B	B	B	B	B																	
				SHEET	1	2	3	4	5	6	7	8	9	10	11																		
PMIC N/A				PREPARED BY Rick C. Officer				DEFENSE ELECTRONICS SUPPLY CENTER DAYTON, OHIO 45444																									
STANDARDIZED MILITARY DRAWING THIS DRAWING IS AVAILABLE FOR USE BY ALL DEPARTMENTS AND AGENCIES OF THE DEPARTMENT OF DEFENSE AMSC N/A				CHECKED BY Charles E. Besore																													
				APPROVED BY Michael A. Frye																													
				DRAWING APPROVAL DATE 90-03-08																													
				REVISION LEVEL B																													
								SIZE A				CAGE CODE 67268				5962-89830																	
								SHEET 1 OF 11								1																	

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5962-E248-93

DISTRIBUTION STATEMENT A. Approved for public release; distribution is unlimited.

1. SCOPE

1.1 Scope. This drawing describes device requirements for class B microcircuits in accordance with 1.2.1 of MIL-STD-883, "Provisions for the use of MIL-STD-883 in conjunction with compliant non-JAN devices".

1.2 Part or Identifying Number (PIN). The complete PIN shall be as shown in the following example:

5962-89830	01	R	X
Drawing number	Device type (see 1.2.1)	Case outline (see 1.2.2)	Lead finish (see 1.2.3)

1.2.1 Device type(s). The device type(s) shall identify the circuit function as follows:

Device type	Generic number	Circuit function	Gain error
01	LTC1090	10-bit data acquisition system	±2.0 LSB
02	LTC1290B	12-bit data acquisition system	±0.5 LSB
03	LTC1290C	12-bit data acquisition system	±1.0 LSB
04	LTC1290D	12-bit data acquisition system	±4.0 LSB

1.2.2 Case outline(s). The case outline(s) shall be as designated in MIL-STD-1835 and as follows:

Outline letter	Descriptive designator	Terminals	Package style
R	GDIP1-T20 or CDIP2-T20	20	dual-in-line

1.2.3 Lead finish. The lead finish shall be as specified in MIL-M-38510. Finish letter "X" shall not be marked on the microcircuit or its packaging. The "X" designation is for use in specifications when lead finishes A, B, and C are considered acceptable and interchangeable without preference.

1.3 Absolute maximum ratings. 1/

Supply voltage (V+) to GND or (V-)	12 V dc
Negative supply voltage (V-)	-6 V to GND
Analog and reference input voltage range	(V-) -0.3 V to V+ +0.3 V
Digital input voltage range	-0.3 V to 12 V
Digital output voltage range	-0.3 V to V+ +0.3 V
Power dissipation (P _D)	500 mW
Lead temperature (soldering, 10 seconds)	+300°C
Storage temperature range	-65°C to +150°C
Junction temperature (T _J)	175°C
Thermal resistance, junction-to-case (θ _{JC})	See MIL-STD-1835
Thermal resistance, junction-to-ambient (θ _{JA})	70°C/W

1/ All voltage values are with respect to ground with DGND, AGND, and REF- wired together, unless otherwise noted.

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1.4 Recommended operating conditions. 2/

Positive supply voltage range (V+)	4.5 V dc to 10 V dc
Negative supply voltage range (V-)	-5.5 V dc to 0
Shift clock frequency range (f _{SCLK}):	
Device type 01	0 to 1.0 MHz
Device type 02, 03, 04	0 to 2.0 MHz
A/D clock frequency range (f _{ACLK}):	
Device type 01	f _{SCLK} to 2.0 MHz
Device type 02, 03, 04	f _{SCLK} to 4.0 MHz
Total cycle time (t _{CYC}):	
Device type 01	10 SCLK + 48 ACLK cycles minimum
Device type 02, 03, 04	12 SCLK + 56 ACLK cycles minimum
Hold time, CS low after last SCLK negative edge (t _{HCS})	0 ns minimum
Hold time, D _{IN} after SCLK positive edge (t _{HD}):	
Device type 01	150 ns minimum
Device type 02, 03, 04	50 ns minimum
Setup time CS negative edge before clocking in first address bit (t _{SUCS}):	
Device type 01	2 ACLK cycles + 1 μs minimum
Device type 02, 03, 04	2 ACLK cycles + 100 ns minimum
Setup time, D _{IN} stable before SCLK positive edge (t _{SUD}):	
Device type 01	400 ns minimum
Device type 02, 03, 04	50 ns minimum
ACLK high time (t _{WHACK})	127 ns minimum
ACLK low time (t _{WLACK})	200 ns minimum
CS high time during conversion (t _{WHCS}):	
Device type 01	44 ACLK cycles minimum
Device type 02, 03, 04	52 ACLK cycles minimum
Ambient operating temperature range (T _A)	-55°C to +125°C

2. APPLICABLE DOCUMENTS

2.1 Government specification, standards, and bulletin. Unless otherwise specified, the following specification, standards, and bulletin of the issue listed in that issue of the Department of Defense Index of Specifications and Standards specified in the solicitation, form a part of this drawing to the extent specified herein.

SPECIFICATION

MILITARY

MIL-M-38510 - Microcircuits, General Specification for.

STANDARDS

MILITARY

MIL-STD-883 - Test Methods and Procedures for Microelectronics.
MIL-STD-1835 - Microcircuit Case Outlines.

BULLETIN

MILITARY

MIL-BUL-103 - List of Standardized Military Drawings (SMD's).

(Copies of the specification, standards, and bulletin required by manufacturers in connection with specific acquisition functions should be obtained from the contracting activity or as directed by the contracting activity.)

2/ V+ = 5.0 V dc, unless otherwise noted.

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2.2 Order of precedence. In the event of a conflict between the text of this drawing and the references cited herein, the text of this drawing shall take precedence.

3. REQUIREMENTS

3.1 Item requirements. The individual item requirements shall be in accordance with 1.2.1 of MIL-STD-883, "Provisions for the use of MIL-STD-883 in conjunction with compliant non-JAN devices" and as specified herein.

3.2 Design, construction, and physical dimensions. The design, construction, and physical dimensions shall be as specified in MIL-M-38510 and herein.

3.2.1 Case outline. The case outline shall be in accordance with 1.2.2 herein.

3.2.2 Terminal connections. The terminal connections shall be as specified on figure 1.

3.3 Electrical performance characteristics. Unless otherwise specified herein, the electrical performance characteristics are as specified in table I and shall apply over the full (case or ambient) operating temperature range.

3.4 Electrical test requirements. The electrical test requirements shall be the subgroups specified in table II. The electrical tests for each subgroup are described in table I.

3.5 Marking. Marking shall be in accordance with MIL-STD-883 (see 3.1 herein). The part shall be marked with the PIN listed in 1.2 herein. In addition, the manufacturer's PIN may also be marked as listed in MIL-BUL-103 (see 6.6 herein).

3.6 Certificate of compliance. A certificate of compliance shall be required from a manufacturer in order to be listed as an approved source of supply in MIL-BUL-103 (see 6.6 herein). The certificate of compliance submitted to DESC-EC prior to listing as an approved source of supply shall affirm that the manufacturer's product meets the requirements of MIL-STD-883 (see 3.1 herein) and the requirements herein.

3.7 Certificate of conformance. A certificate of conformance as required in MIL-STD-883 (see 3.1 herein) shall be provided with each lot of microcircuits delivered to this drawing.

3.8 Notification of change. Notification of change to DESC-EC shall be required in accordance with MIL-STD-883 (see 3.1 herein).

3.9 Verification and review. DESC, DESC's agent, and the acquiring activity retain the option to review the manufacturer's facility and applicable required documentation. Offshore documentation shall be made available onshore at the option of the reviewer.

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TABLE I. Electrical performance characteristics.

Test	Symbol	Conditions ^{1/} $-55^{\circ}\text{C} \leq T_A \leq +125^{\circ}\text{C}$ unless otherwise specified	Group A subgroups	Device type	Limits		Unit
					Min	Max	
High level input voltage	V_{IH}	$V+ = 5.25 \text{ V}$	1, 2, 3	ALL	2.0		V
Low level input voltage	V_{IL}	$V+ = 4.75 \text{ V}$	1, 2, 3	ALL		0.8	V
High level input current	I_{IH}	$V_{IN} = V+$	1, 2, 3	ALL		2.5	μA
Low level input current	I_{IL}	$V_{IN} = 0 \text{ V}$	1, 2, 3	ALL		-2.5	μA
High level output voltage	V_{OH}	$V+ = 4.75 \text{ V},$ $I_O = 360 \mu\text{A}$	1, 2, 3	ALL	2.4		V
Low level output voltage	V_{OL}	$V+ = 4.75 \text{ V},$ $I_O = 1.6 \text{ mA}$	1, 2, 3	ALL		0.4	V
Hi-Z output leakage	I_{OZ}	$V_{OUT} = V+, \overline{\text{CS}} \text{ high}$	1, 2, 3	ALL		3.0	μA
		$V_{OUT} = 0 \text{ V}, \overline{\text{CS}} \text{ high}$				-3.0	
Positive supply current	$I+$	$\overline{\text{CS}}$ high, REF+ open	1, 2, 3	01		2.5	mA
				02,03,04		12	
Reference current	I_{REF}	$V_{REF} = 5 \text{ V}$	1, 2, 3	01		1.0	mA
				02,03,04		0.05	
Negative supply current	$I-$	$\overline{\text{CS}}$ high, $V- = -5 \text{ V}$	1, 2, 3	ALL		50	μA
Offset error ^{2/}	V_{OS}		1, 2, 3	01		± 0.5	LSB
				02,03,04		± 1.5	
Linearity error ^{2/ 3/}			1, 2, 3	01,02,03		± 0.5	LSB
				04		± 0.75	
Gain error ^{2/}	A_E		1, 2, 3	01		± 2.0	LSB
				02		± 0.5	
				03		± 1.0	
				04		± 4.0	

See footnotes at end of table.

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TABLE I. Electrical performance characteristics - Continued.

Test	Symbol	Conditions ^{1/} -55°C ≤ T _A ≤ +125°C unless otherwise specified	Group A subgroups	Device type	Limits		Unit
					Min	Max	
Total unadjusted ^{2/} ^{4/} error		V _{REF} = 5 V	1, 2, 3	01		±2.0	LSB
Analog and REF ^{5/} input range			1, 2, 3	ALL	(V-) -0.02	(V+) +0.02	V
On channel leakage current ^{6/}	R _{ON}	On channel = 5 V, Off channel = 0 V	1, 2, 3	ALL		1	μA
		On channel = 0 V, Off channel = 5 V	1, 2, 3	ALL		-1	
Off channel leakage current ^{6/}	R _{OFF}	On channel = 5 V, Off channel = 0 V	1, 2, 3	ALL		-1	μA
		On channel = 0 V, Off channel = 5 V	1, 2, 3	ALL		1	
Delay time, SCLK negative edge to D _{OUT} data valid	t _{dDO}	See figures 2 and 3	9, 10, 11	01		450	ns
				02,03,04		270	
Delay time, CS positive edge to D _{OUT} Hi-Z	t _{dis}	See figures 2 and 3	9, 10, 11	01		300	ns
				02,03,04		100	
Delay time, 2nd CLK negative edge to D _{OUT} enabled	t _{en}	See figures 2 and 3	9, 10, 11	01		400	ns
				02,03,04		200	
D _{OUT} fall time	t _f	See figures 2 and 3	9, 10, 11	01		300	ns
				02,03,04		130	
D _{OUT} rise time	t _r	See figures 2 and 3	9, 10, 11	01		300	ns
				02,03,04		50	

^{1/} V₊ = 5 V, V_{REF+} = 5 V, V_{REF-} = 0 V, V₋ = 0 V for unipolar mode and -5 V for bipolar mode, ACLK = 4.0 MHz unless otherwise specified.

^{2/} Applies for both unipolar and bipolar modes.

^{3/} Linearity error is specified between the actual end-points of the A/D transfer curve.

^{4/} Total unadjusted error includes offset, gain, linearity, multiplexer and hold step errors.

^{5/} Two on-chip diodes are tied to each reference and analog input which will conduct for reference or analog input voltages, one diode drop below V₋ or one diode drop above V_{CC}. Be careful during testing at low V_{CC} levels (4.5 V), as high level reference or analog inputs (5 V) can cause this input diode to conduct, especially at elevated temperatures, and cause errors for inputs near full-scale. This specification allows 50 mV forward bias of either diode. This means that as long as the reference or analog input does not exceed the supply voltage by more than 50 mV, the output code will be correct. To achieve an absolute 0 V to 5 V input voltage range will therefore require a minimum supply voltage of 4.950 V over initial tolerance, temperature variations and loading.

^{6/} Channel leakage current is measured after the channel selection.

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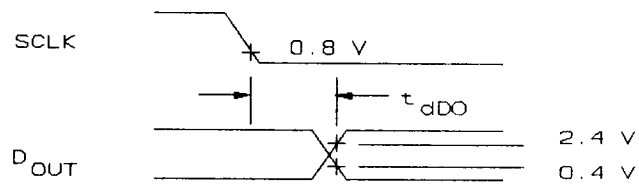
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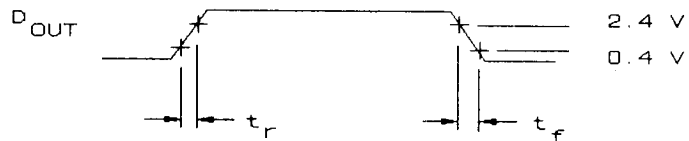
Device type	01,02,03,04
Case outline	R
Terminal number	Terminal symbol
1	CH0
2	CH1
3	CH2
4	CH3
5	CH4
6	CH5
7	CH6
8	CH7
9	COM
10	DGND
11	AGND
12	V-
13	REF-
14	REF+
15	CS
16	D _{OUT}
17	D _{IN}
18	SCLK
19	ACLK
20	V+

FIGURE 1. Terminal connections.

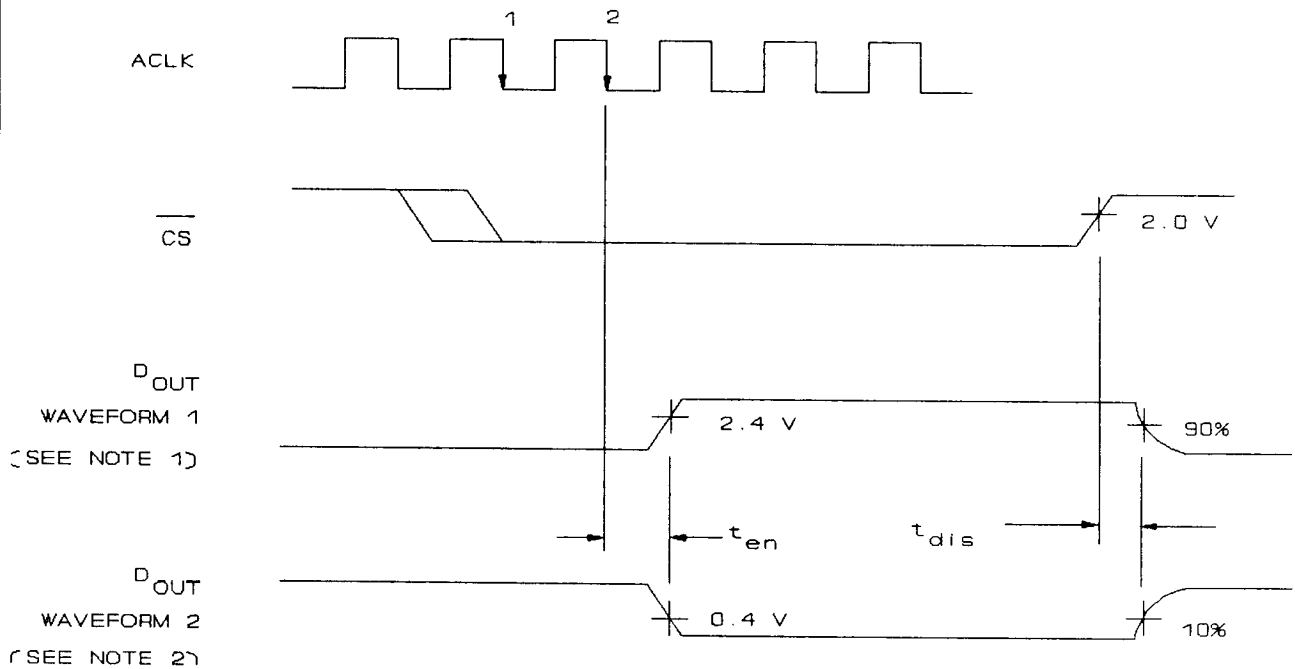
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D_{OUT} RISE AND FALL TIMES, t_r , t_f



t_{en} AND t_{dis}



NOTES:

1. Waveform 1 is for an output with internal conditions such that the output is high unless disabled by the output control.
2. Waveform 2 is for an output with internal conditions such that the output is low unless disabled by the output control.

FIGURE 2. Timing waveforms.

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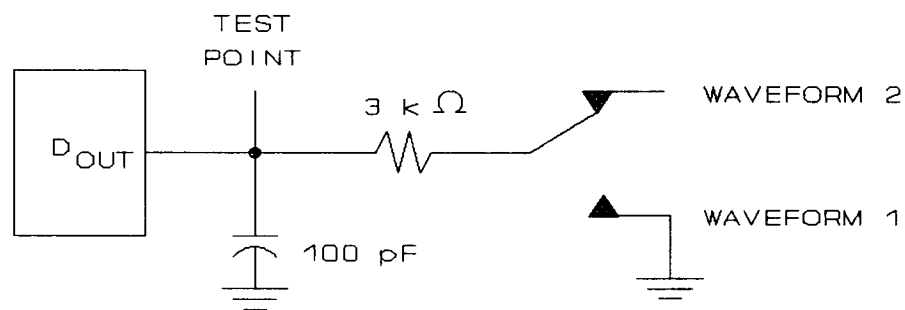
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LOAD CIRCUIT FOR t_{dis} AND t_{en}



LOAD CIRCUIT FOR t_{dDO} , t_r , AND t_f

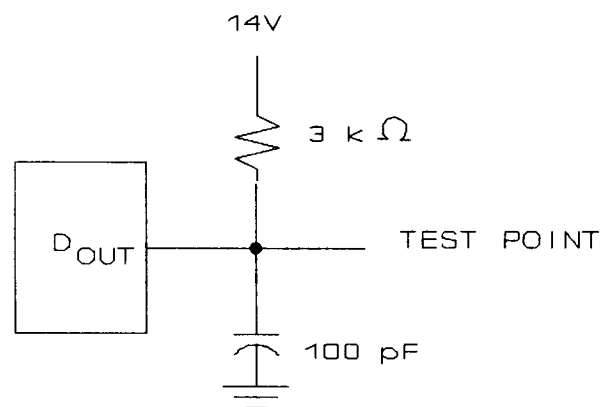


FIGURE 3. Test circuits.

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TABLE II. Electrical test requirements.

MIL-STD-883 test requirements	Subgroups (in accordance with method 5005, table I)
Interim electrical parameters (method 5004)	1
Final electrical test parameters (method 5004)	1*, 2, 3, 9, 10, 11
Group A test requirements (method 5005)	1, 2, 3, 9, 10, 11
Groups C and D end-point electrical parameters (method 5005)	1

* PDA applies to subgroup 1.

4. QUALITY ASSURANCE PROVISIONS

4.1 Sampling and inspection. Sampling and inspection procedures shall be in accordance with section 4 of MIL-M-38510 to the extent specified in MIL-STD-883 (see 3.1 herein).

4.2 Screening. Screening shall be in accordance with method 5004 of MIL-STD-883, and shall be conducted on all devices prior to quality conformance inspection. The following additional criteria shall apply:

a. Burn-in test, method 1015 of MIL-STD-883.

(1) Test condition A, B, C, or D. The test circuit shall be maintained by the manufacturer under document revision level control and shall be made available to the preparing or acquiring activity upon request. The test circuit shall specify the inputs, outputs, biases, and power dissipation, as applicable, in accordance with the intent specified in test method 1015 of MIL-STD-883.

(2) $T_A = +125^{\circ}\text{C}$, minimum.

b. Interim and final electrical test parameters shall be as specified in table II herein, except interim electrical parameter tests prior to burn-in are optional at the discretion of the manufacturer.

4.3 Quality conformance inspection. Quality conformance inspection shall be in accordance with method 5005 of MIL-STD-883 including groups A, B, C, and D inspections. The following additional criteria shall apply.

4.3.1 Group A inspection.

a. Tests shall be as specified in table II herein.

b. Subgroups 4, 5, 6, 7, and 8 in table I, method 5005 of MIL-STD-883 shall be omitted.

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4.3.2 Groups C and D inspections.

- a. End-point electrical parameters shall be as specified in table II herein.
- b. Steady-state life test conditions, method 1005 of MIL-STD-883.
 - (1) Test condition A, B, C, or D. The test circuit shall be maintained by the manufacturer under document revision level control and shall be made available to the preparing or acquiring activity upon request. The test circuit shall specify the inputs, outputs, biases, and power dissipation, as applicable, in accordance with the intent specified in test method 1005 of MIL-STD-883.
 - (2) $T_A = +125^{\circ}\text{C}$, minimum.
 - (3) Test duration: 1,000 hours, except as permitted by method 1005 of MIL-STD-883.

5. PACKAGING

5.1 Packaging requirements. The requirements for packaging shall be in accordance with MIL-M-38510.

6. NOTES

6.1 Intended use. Microcircuits conforming to this drawing are intended for use when military specifications do not exist and qualified military devices that will perform the required function are not available for original equipment manufacturer application. When a military specification exists and the product covered by this drawing has been qualified for listing on QPL-38510, the device specified herein will be inactivated and will not be used for new design. The QPL-38510 product shall be the preferred item for all applications.

6.2 Replaceability. Microcircuits covered by this drawing will replace the same generic device covered by a contractor-prepared specification or drawing.

6.3 Configuration control of SMD's. All proposed changes to existing SMD's will be coordinated with the users of record for the individual documents. This coordination will be accomplished in accordance with MIL-STD-481 using DD Form 1693, Engineering Change Proposal (Short Form).

6.4 Record of users. Military and industrial users shall inform Defense Electronics Supply Center when a system application requires configuration control and the applicable SMD. DESC will maintain a record of users and this list will be used for coordination and distribution of changes to the drawings. Users of drawings covering microelectronics devices (FSC 5962) should contact DESC-EC, telephone (513) 296-6047.

6.5 Comments. Comments on this drawing should be directed to DESC-EC, Dayton, Ohio 45444, or telephone (513) 296-5377.

6.6 Approved sources of supply. Approved sources of supply are listed in MIL-BUL-103. The vendors listed in MIL-BUL-103 have agreed to this drawing and a certificate of compliance (see 3.6 herein) has been submitted to and accepted by DESC-EC.

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