REVISIONS

LTR	DESCRIPTION	DATE (YR-MO-DA)	APPROVED
A	Add "Changes in accordance with NOR 5962-R04893.	92-12-09	M. A. Frye
B	Add "Changes in accordance with NOR 5962-R07193.	93-01-22	M. A. Frye
C	Added one device type, made format changes, and editorial changes throughout.	94-01-27	M. A. Frye

THE ORIGINAL FIRST PAGE OF THIS DRAWING HAS BEEN REPLACED.

REV																			
SHEET																			
REV	C																		
SHEET	15																		

REV STATUS OF SHEETS	REV	C	C	C	C	C	C	C	C	B	B	B	B	C	C
	SHEET	1	2	3	4	5	6	7	8	9	10	11	12	13	14

PMIC N/A

STANDARDIZED MILITARY DRAWING

THIS DRAWING IS AVAILABLE FOR USE BY ALL DEPARTMENTS AND AGENCIES OF THE DEPARTMENT OF DEFENSE

AMSC N/A

PREPARED BY
Kenneth Rice

CHECKED BY
Charles Reusing

APPROVED BY
Michael A. Frye

DRAWING APPROVAL DATE
18 November 1989

REVISION LEVEL
C

DEFENSE ELECTRONICS SUPPLY CENTER
DAYTON, OHIO 45444

MICROCIRCUIT, MEMORY, DIGITAL, CMOS, EE PROGRAMMABLE ARRAY LOGIC, MONOLITHIC SILICON

SIZE	CAGE CODE	5962-89840
A	67268	

SHEET 1 OF 15

DESC FORM 193
JUL 91

5962-E116-94

1. SCOPE

1.1 Scope. This drawing describes device requirements for class B microcircuits in accordance with 1.2.1 of MIL-STD-883, "Provisions for the use of MIL-STD-883 in conjunction with compliant non-JAN devices".

1.2 Part or Identifying Number (PIN). The complete PIN shall be as shown in the following example:

1.2.1 Device type(s). The device type(s) shall identify the circuit function as follows:

Device type	Generic number	Circuit function	Access time
01	20V8	20-input, 8-output, EE CMOS, architecturally generic, programmable AND-OR array	30
02	20V8	20-input, 8-output, EE CMOS, architecturally generic, programmable AND-OR array	20
03	20V8	20-input, 8-output, EE CMOS, architecturally generic, programmable AND-OR array	15
04	20V8	20-input, 8-output, EE CMOS, architecturally generic, programmable AND-OR array	10

1.2.2 Case outline(s). The case outline(s) shall be as designated in MIL-STD-1835 and as follows:

Outline letter	Descriptive designator	Terminals	Package style
L	GDIP3-T24 or CDIP4-T24	24	Dual-in-line package
3	CQCC1-N28	28	Square chip carrier package

1.2.3 Lead finish. The lead finish shall be as specified in MIL-STD-883 (see 3.1 herein). Finish letter "X" shall not be marked on the microcircuit or its packaging. The "X" designation is for use in specifications when lead finishes A, B, and C are considered acceptable and interchangeable without preference.

1.3 Absolute maximum ratings.

Supply voltage range	-0.5 V dc to +7.0 V dc
Input voltage range applied	-2.5 V dc to V_{CC} + 1.0 V dc 1/
Off-state output voltage range applied	-2.5 V dc to V_{CC} + 1.0 V dc 1/
Storage temperature range	-65°C to +150°C
Maximum power dissipation (P_D) 2/	1.5 W
Lead temperature (soldering, 10 seconds)	+260°C
Thermal resistance, junction-to-case (θ_{JC})	See MIL-STD-1835
Junction temperature (TJ)	+175°C
Data retention	10 years (minimum)
Endurance	100 erase/write cycles (minimum)

1/ Minimum input voltage is -0.5 V dc which may undershoot to -2.5 V dc for pulses less than 20 ns.
2/ Must withstand the added P_D due to short circuit test, e.g., I_{OS}.

1.4 Recommended operating conditions.

Supply voltage range (V_{CC})	4.5 V dc to 5.5 V dc
High level input voltage range (V_{IH})	2.0 V dc to V_{CC} + 1.0 V dc
Low level input voltage range (V_{IL})	V_{SS} -0.5 V dc to +0.8 V dc
High level output current (I_{OH})	-2.0 mA maximum
Low level output current (I_{OL})	12 mA maximum
Case operating temperature range (T_C)	-55°C to +125°C

2. APPLICABLE DOCUMENTS

2.1 Government specification, standards, and bulletin. Unless otherwise specified, the following specification, standards, and bulletin of the issue listed in that issue of the Department of Defense Index of Specifications and Standards specified in the solicitation, form a part of this drawing to the extent specified herein.

SPECIFICATION

MILITARY

MIL-I-38535 - Integrated Circuits (Microcircuits) Manufacturing, General Specification for.

STANDARDS

MILITARY

MIL-STD-883 - Test Methods and Procedures for Microelectronics.
MIL-STD-1835 - Microcircuit Case Outlines.

BULLETIN

MILITARY

MIL-BUL-103 - List of Standardized Military Drawings (SMD's).

(Copies of the specification, standards, and bulletin required by manufacturers in connection with specific acquisition functions should be obtained from the contracting activity or as directed by the contracting activity.)

2.2 Order of precedence. In the event of a conflict between the text of this drawing and the references cited herein, the text of this drawing shall take precedence.

3. REQUIREMENTS

3.1 Item requirements. The individual item requirements shall be in accordance with 1.2.1 of MIL-STD-883, "Provisions for the use of MIL-STD-883 in conjunction with compliant non-JAN devices" and as specified herein. Product built to this drawing that is produced by a Qualified Manufacturer Listing (QML) certified and qualified manufacturer or a manufacturer who has been granted transitional certification to MIL-I-38535 may be processed as QML product in accordance with the manufacturers approved program plan and qualifying activity approval in accordance with MIL-I-38535. This QML flow as documented in the Quality Management (QM) plan may make modifications to the requirements herein. These modifications shall not affect form, fit, or function of the device. These modifications shall not affect the PIN as described herein. A "Q" or "QML" certification mark in accordance with MIL-I-38535 is required to identify when the QML flow option is used.

3.2 Design, construction, and physical dimensions. The design, construction, and physical dimensions shall be as specified in MIL-STD-883 (see 3.1 herein) and herein.

3.2.1 Case outline(s). The case outline(s) shall be in accordance with 1.2.2 herein.

3.2.2 Terminal connections. The terminal connections shall be as specified on figure 1.

3.2.3 Truth table (unprogrammed devices). The truth tables for unprogrammed devices shall be as specified on figure 2.

3.2.4 Programmed devices. The requirements for supplying programmed devices are not a part of this drawing.

3.3 Electrical performance characteristics. Unless otherwise specified herein, the electrical performance characteristics are as specified in table I and shall apply over the full case operating temperature range.

3.4 Electrical test requirements. The electrical test requirements shall be the subgroups specified in table II. The electrical tests for each subgroup are described in table I.

3.5 Marking. Marking shall be in accordance with MIL-STD-883 (see 3.1 herein). The part shall be marked with the PIN listed in 1.2 herein. In addition, the manufacturer's PIN may also be marked as listed in MIL-BUL-103 (see 6.6 herein).

3.6 Certificate of compliance. A certificate of compliance shall be required from a manufacturer in order to be listed as an approved source of supply in MIL-BUL-103 (see 6.6 herein). The certificate of compliance submitted to DESC-EC prior to listing as an approved source of supply shall affirm that the manufacturer's product meets the requirements of MIL-STD-883 (see 3.1 herein) and the requirements herein.

3.7 Certificate of conformance. A certificate of conformance as required in MIL-STD-883 (see 3.1 herein) shall be provided with each lot of microcircuits delivered to this drawing.

3.8 Notification of change. Notification of change to DESC-EC shall be required in accordance with MIL-STD-883 (see 3.1 herein).

3.9 Verification and review. DESC, DESC's agent, and the acquiring activity retain the option to review the manufacturer's facility and applicable required documentation. Offshore documentation shall be made available onshore at the option of the reviewer.

4. QUALITY ASSURANCE PROVISIONS

4.1 Sampling and inspection. Sampling and inspection procedures shall be in accordance with MIL-STD-883 (see 3.1 herein).

4.2 Screening. Screening shall be in accordance with method 5004 of MIL-STD-883, and shall be conducted on all devices prior to quality conformance inspection. The following additional criteria shall apply:

a. Burn-in test, method 1015 of MIL-STD-883.

(1) Test condition D. The test circuit shall be maintained by the manufacturer under document revision level control and shall be made available to the preparing or acquiring activity upon request. The test circuit shall specify the inputs, outputs, biases, and power dissipation, as applicable, in accordance with the intent specified in test method 1015 of MIL-STD-883.

(2) T_A = +125°C, minimum.

(3) Devices shall be burned-in containing a pattern that assures all inputs and I/O's are dynamically switched. This pattern must have all cells programmed in a high or low state (not neutralized).

(4) The burn-in pattern shall be read before and after burn-in. The pattern shall be read after burn-in at margin voltage levels (see 4.2c(4)). Devices having any logic array bits not in the proper state (per margin voltage levels) shall constitute a device failure and shall be added as failures for PDA calculation.

b. Interim and final electrical test parameters shall be as specified in table II herein, except interim electrical parameter tests prior to burn-in are optional at the discretion of the manufacturer.

c. An endurance/retention test prior to burn-in, in accordance with method 1033 of MIL-STD-883, shall be included as part of the screening procedure with the following conditions:

(1) Cycling may be at equipment room ambient temperature and shall cycle all bit locations for a minimum of 100 cycles. After cycling, devices containing bits which fail to verify at margin voltage levels (see 4.2c(4)) shall be considered device failures.

TABLE I. Electrical performance characteristics.

Test	Symbol	Conditions $-55°C \le T_C \le +125°C$ $V_{SS} = 0$ V, $4.5\ V \le V_{CC} \le 5.5$ V unless otherwise specified	Device types	Group A subgroups	Limits		Unit
					Min	Max	
Input leakage current	I_{LX}	$0.0\ V \le V_{IN} \le V_{CC}$	01-03, 04	1,2,3	-10 -100	+10 +10	µA
Bidirectional pin leakage current	$I_{I/O/Q}$	$0.0\ V \le V_{I/O/Q} \le V_{CC}$	01-03 04	1,2,3	-10 -100	+10 +10	µA
Output low voltage	V_{OL}	$V_{CC} = 4.5$ V, $I_{OL} = 12$ mA, $V_{IN} = V_{IH}$ or V_{IL}	All	1,2,3		0.5	V
Output high voltage	V_{OH}	$V_{CC} = 4.5$ V, $I_{OH} = -2.0$ mA, $V_{IN} = V_{IH}$ or V_{IL}	All	1,2,3	2.4		V
Input low voltage 1/	V_{IL}		All	1,2,3	V_{SS} -0.5	0.8	V
Input high voltage 1/	V_{IH}		All	1,2,3	2.0	V_{CC} +1.0	V
Operating power supply current	I_{CC}	$V_{IL} = 0.5$ V, $V_{IH} = 3.0$ V, $f_{tog} = 25$ MHz	All	1,2,3		130	mA
Output short circuit current 2/	I_{OS}	$V_{CC} = 5.0$ V, $V_{OUT} = 0.5$ V, $T_A = +25°C$, see 4.3.1e	All	1	-30	-150	mA
Input capacitance	C_{IN}	$V_{CC} = 5.0$ V, $V_I = 2.0$ V, f = 1.0 MHz, $T_A = +25°C$, see 4.3.1c	All	4		8.0	pF
Bidirectional pin capacitance	$C_{I/O/Q}$	$V_{CC} = 5.0$ V, $V_{I/O/Q} = 2.0$ V, f = 1.0 MHz, $T_A = +25°C$, see 4.3.1c	All	4		10	pF
Functional tests		see 4.3.1d	7,8A,8B	All			

See footnotes at end of table.

TABLE I. Electrical performance characteristics - Continued.

Test	Symbol	Conditions $-55°C \le T_C \le +125°C$ V_{SS} = 0 V, 4.5 V $\le V_{CC} \le$ 5.5 V unless otherwise specified	Device types	Group A subgroups	Limits		Unit
					Min	Max	
Input or feedback to nonregistered output	t_{PD}	V_{CC} = 4.5 V, see figures 3 and 4 3/	01	9,10,11	3.0	30	ns
			02		3.0	20	
			03		3.0	15	
			04		2.0	10	
Clock to output delay 4/	t_{CO}		01	9,10,11	2.0	20	ns
			02		2.0	15	
			03		2.0	12	
			04		1.0	7	
Input to output enable	t_{EA1}		01	9,10,11		30	ns
			02			20	
			03			15	
			04			10	
Input to output register enable 4/	t_{EA2}		01	9,10,11		25	ns
			02			18	
			03			15	
			04			10	

See footnotes at end of table.

TABLE I. Electrical performance characteristics - Continued.

Test	Symbol	Conditions $-55°C \le T_C \le +125°C$ V_{SS} = 0 V, 4.5 V ≤ V_{CC} ≤ 5.5 V unless otherwise specified	Device type	Group A subgroups	Limits		Unit
					Min	Max	
Input to output disable 5/	t_{ER1}	V_{CC} = 4.5 V, see figures 3 and 4 3/	01	9,10,11		30	ns
			02			20	
			03			15	
			04			10	
Input to output register disable 4/ 5/	t_{ER2}		01	9,10,11		25	ns
			02			18	
			03			15	
			04			10	
Clock frequency without feedback 4/	f_{CLK1}		01	9,10,11	0.0	33.3	MHz
			02		0.0	41.6	
			03		0.0	50.0	
			04		0.0	62.5	
Clock frequency with feedback 4/	f_{CLK2}		01	9,10,11	0.0	22.2	MHz
			02		0.0	33.3	
			03		0.0	41.6	
			04		0.0	58.8	

See footnotes at end of table.

TABLE I. Electrical performance characteristics - Continued.

Test	Symbol	Conditions $-55°C \le T_C \le +125°C$ V_{SS} = 0 V, 4.5 V ≤ V_{CC} ≤ 5.5 V unless otherwise specified	Device type	Group A subgroups	Limits		Unit
					Min	Max	
Input or feedback setup time, before rising clock 4/	t_S	V_{CC} = 4.5 V, see figures 3 and 4 3/	01	9,10,11	25		ns
			02		15		
			03		12		
			04		10		
Input or feedback hold time after rising clock 4/	t_H		All	9,10,11	0		ns
Clock pulse width, high 4/	t_{PWH}		01	9,10,11	15		ns
			02		12		
			03		10		
			04		8		
Clock pulse width, low 4/	t_{PWL}		01	9,10,11	15		ns
			02		12		
			03		10		
			04		8		

1/ These are absolute values with respect to device ground and all overshoots due to system or tester noise are included.

2/ Not more than one output at a time should be shorted. Short circuit test duration should not exceed 1 second (see 4.3.1d).

3/ AC tests are performed with input rise and fall times (10% to 90%) ≤ 5 ns, timing reference levels of 1.5 V, input pulse levels of 0 to 3.0 V and the output load of figure 3. Input pulse levels are absolute values with respect to device ground and all overshoots due to system or tester noise are included.

4/ Test applies only to registered outputs.

5/ Transition is measured at steady-state high level -500 mV or steady-state low level +500 mV on the output from the 1.5 V level on the input.

Device types	All	
Case outlines	L	3
Terminal number	Terminal symbol	
1	I/CLK	NC
2	I	I/CLK
3	I	I
4	I	I
5	I	I
6	I	I
7	I	I
8	I	NC
9	I	I
10	I	I
11	I	I
12	GND	I
13	I/OE	GND
14	I	NC
15	I/O/Q	I/OE
16	I/O/Q	I
17	I/O/Q	I/O/Q
18	I/O/Q	I/O/Q
19	I/O/Q	I/O/Q
20	I/O/Q	I/O/Q
21	I/O/Q	I/O/Q
22	I/O/Q	NC
23	I	I/O/Q
24	V_{CC}	I/O/Q
25	---	I/O/Q
26	---	I/O/Q
27	---	I
28	---	V_{CC}

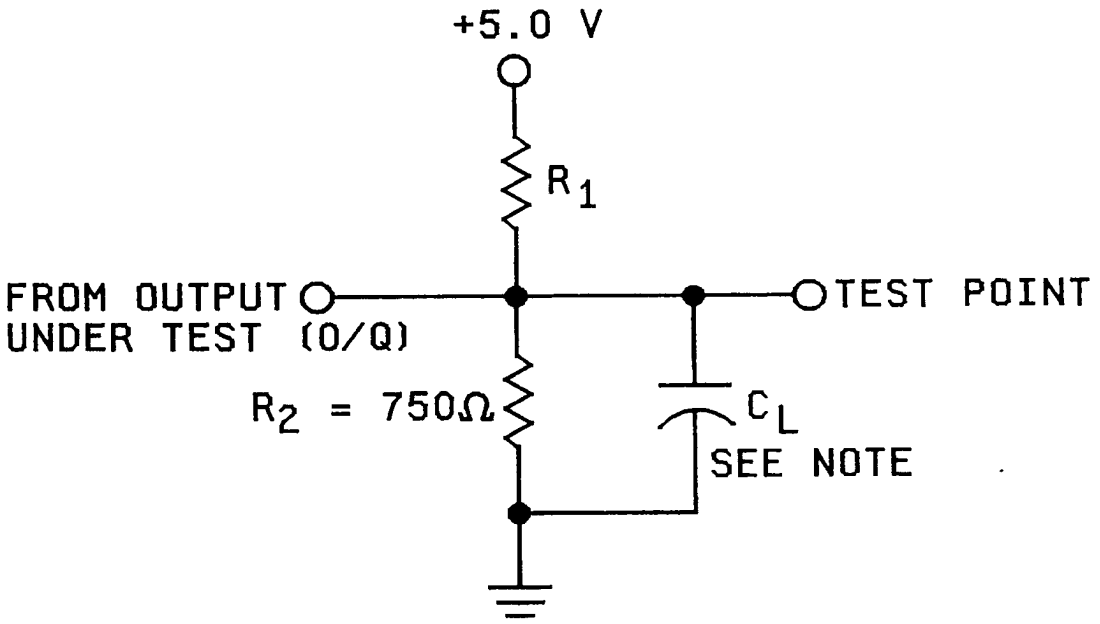
FIGURE 1. Terminal connections.

Inputs													
I/CLK	I/$\overline{OE}$	I	I	I	I	I	I	I	I	I	I	I	I
X	X	X	X	X	X	X	X	X	X	X	X	X	X

Outputs							
I/O/Q	I/O/Q	I/O/Q	I/O/Q	I/O/Q	I/O/Q	I/O/Q	I/O/Q
H	H	H	H	H	H	H	H

X = Don't care state
H = Logic high

FIGURE 2. Truth tables (unprogrammed).



Test	R_1	C_L (minimum)
t_{PD}, t_{CO}, f_{CLK1}, f_{CLK2}	390Ω	50 pF
t_{EA1}, t_{EA2}	Active high = infinity Active low = 390Ω	50 pF
t_{ER1}, t_{ER2}	Active high = infinity Active low = 390Ω	5.0 pF

NOTE: C_L = load capacitance and includes jig and probe capacitance.

FIGURE 3. Output load circuit.

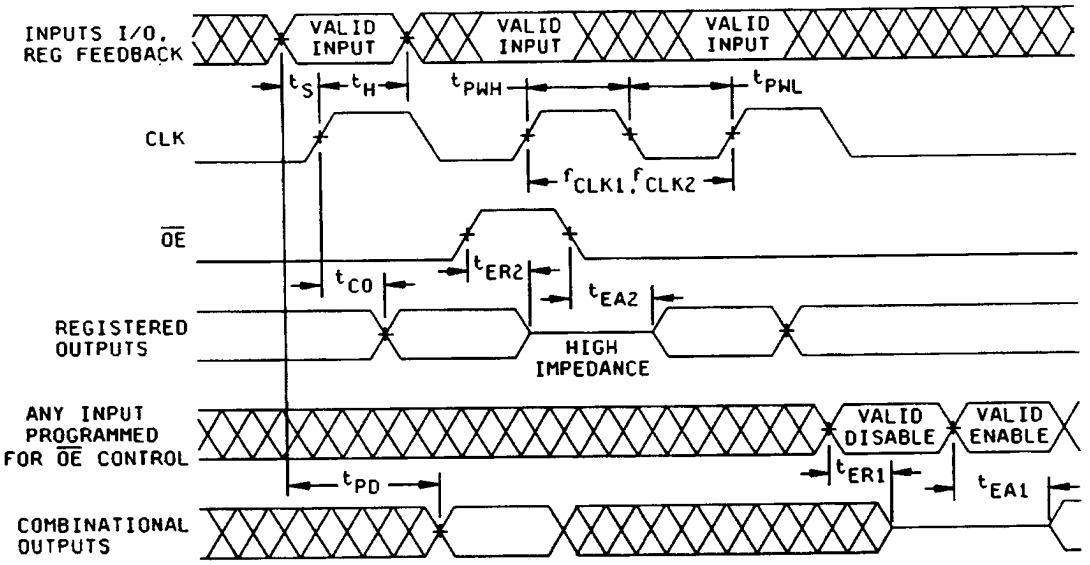


FIGURE 4. Switching waveforms.

TABLE II. Electrical test requirements.

MIL-STD-883 test requirements	Subgroups (in accordance with method 5005, table I)
Interim electrical parameters (method 5004)	---
Final electrical test parameters (method 5004)	1*, 2, 3, 7*, 8A, 8B, 9, 10, 11
Group A test requirements (method 5005)	1, 2, 3, 4**, 7, 8A, 8B, 9, 10, 11
Group C and D end-point electrical parameters (method 5005)	2, 3, 7, 8A, 8B

* PDA applies to subgroups 1 and 7.
** See 4.3.1c.

(2) The retention pattern must have 100 percent of the logic array programmed.

(3) After cycling, perform a high temperature unbiased bake for a minimum 48 hours at +150°C. The bake time may be accelerated by using higher temperature in accordance with the Arrhenius Relationship:

$$A_F = e^{-\frac{E_A}{K}\left[\frac{1}{T1}-\frac{1}{T2}\right]}$$

A_F = acceleration factor (unitless quantity) = t_1/t_2.
T = temperature in Kelvin (i.e., °C + 273 = K)
t_1 = time (hours) at temperature T_1
t_2 = time (hours) at temperature T_2
K = Boltzmanns constant = 8.62×10^{-5} eV/°K using an apparent activation energy (E_A) of 0.6 eV.

The maximum bake temperature shall not exceed +200°C.

(4) Read the data retention pattern at margin voltage levels ($V_{TL} \leq 1.0$ V and $V_{TH} \geq 4.0$ V) and test using subgroups 1 and 7 (at the manufacturer's option, high temperature equivalent subgroups 2 and 8A or low temperature equivalent subgroups 3 and 8B may be used in lieu of subgroups 1 and 7) after cycling and bake, prior to burn-in. Devices having any logic array bits not in the proper state after storage shall constitute device failure.

(5) At the manufacturer's option, the testing specified in 4.2c(4) may be deleted if the devices are put into burn-in with no reprogramming allowed between the start of data retention bake and the end of burn-in. Exercising this option will result in data retention bake failures being caught and included in post-burn-in PDA calculations.

4.3 Quality conformance inspection. Quality conformance inspection shall be in accordance with method 5005 of MIL-STD-883 including groups A, B, C, and D inspections. The following additional criteria shall apply.

4.3.1 Group A inspection.

a. Tests shall be as specified in table II herein.

b. Subgroups 5 and 6 in table I, method 5005 of MIL-STD-883 shall be omitted.

c. Subgroup 4 (C_{IN} and C_{OUT} measurements) shall be measured only for the initial test and after process or design changes which may affect capacitance. Sample size is 15 devices with no failures, and all input and output terminals tested.

d. Subgroups 7, 8A, and 8B shall consist of verifying functionality of the device. These tests form a part of the the vendors test tape and shall be maintained and available from the approved sources of supply.

e. I_{OS} measurements in subgroup 1 shall be measured only for the initial test and after process or design changes which may affect I_{OS}. Sample size is 15 devices with no failures, and all output terminals tested.

4.3.2 Groups C and D inspections.

a. End-point electrical parameters shall be as specified in table II herein.

b. Steady-state life test conditions, method 1005 of MIL-STD-883.

(1) Test condition D. The test circuit shall be maintained by the manufacturer under document revision level control and shall be made available to the preparing or acquiring activity upon request. The test circuit shall specify the inputs, outputs, biases, and power dissipation, as applicable, in accordance with the intent specified in test method 1005 of MIL-STD-883.

(2) T_A = +125°C, minimum.

(3) Test duration: 1,000 hours, except as permitted by method 1005 of MIL-STD-883.

(4) All devices shall be programmed with a pattern that assures all inputs and I/O's are dynamically switched.

c. An extended data retention test shall be added, a new sample shall be selected and the sample size, frequency of testing, and LTPD shall be the same as that required for subgroup 1 of group C inspection. Extended data retention shall also consist of as follows:

(1) All devices shall have 100 percent of the logic array programmed with a charge on all cells, such that the cell will not be in a neutral state.

(2) Unbiased bake for 1,000 hours (minimum) at +150°C (minimum). The unbiased bake time may be accelerated by using a higher temperature in accordance with the Arrhenius Relationship:

$$A_F = e^{-\frac{E_A}{K}\left[\frac{1}{T1} - \frac{1}{T2}\right]}$$

A_F = acceleration factor (unitless quantity) = t_1/t_2.
T = temperature in Kelvin (i.e., °C + 273 = K)
t_1 = time (hours) at temperature T_1
t_2 = time (hours) at temperature T_2
K = Boltzmanns constant = 8.62×10^{-5} eV/°K using an apparent activation energy (E_A) of 0.6 eV.

The maximum bake temperature shall not exceed +200°C.

(3) Read the pattern after bake and perform end-point electrical tests in accordance with table II herein for group C.

4.4 Programming procedures. The programming procedures shall be as specified by the device manufacturer and shall be made available to the user on request.

4.5 Erasing procedures. The erasing procedures shall be as specified by the device manufacturer and shall be made available to the user on request.

5. PACKAGING

5.1 Packaging requirements. The requirements for packaging shall be in accordance with MIL-STD-883 (see 3.1 herein).

6. NOTES

6.1 Intended use. Microcircuits conforming to this drawing are intended for use for Government microcircuit applications (original equipment), design applications, and logistics purposes.

6.2 Replaceability. Microcircuits covered by this drawing will replace the same generic device covered by a contractor-prepared specification or drawing.

6.3 Configuration control of SMD's. All proposed changes to existing SMD's will be coordinated with the users of record for the individual documents. This coordination will be accomplished in accordance with MIL-STD-973 using DD Form 1692, Engineering Change Proposal (Short Form).

6.4 Record of users. Military and industrial users shall inform Defense Electronics Supply Center when a system application requires configuration control and the applicable SMD. DESC will maintain a record of users and this list will be used for coordination and distribution of changes to the drawings. Users of drawings covering microelectronics devices (FSC 5962) should contact DESC-EC, telephone (513) 296-6047.

6.5 Comments. Comments on this drawing should be directed to DESC-EC, Dayton, Ohio 45444, or telephone (513) 296-5377.

6.6 Approved sources of supply. Approved sources of supply are listed in MIL-BUL-103. The vendors listed in MIL-BUL-103 have agreed to this drawing and a certificate of compliance (see 3.6 herein) has been submitted to and accepted by DESC-EC.