| REVISIONS | | | |
|---|---|---|---|
| LTR | DESCRIPTION | DATE (YR-MO-DA) | APPROVED |
| A | Add device type 02. Technical and editorial changes throughout. Add case outlines D and 2. | 92-04-16 | M. A. Frye |

DO NOT USE 02CX FOR NEW DESIGN.
USE QPL'd M38510/65005BCX.

THE ORIGINAL FIRST PAGE OF THIS DRAWING HAS BEEN REPLACED.

| REV | | | | | | | | | | | | | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| SHEET | | | | | | | | | | | | | | | | | | | |
| REV | | | | | | | | | | | | | | | | | | | |
| SHEET | | | | | | | | | | | | | | | | | | | |

| REV STATUS OF SHEETS | REV | A | A | A | A | A | A | A | A | A | A | A | A | A |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | SHEET | 1 | 2 | 3 | 4 | 5 | 6 | 7 | 8 | 9 | 10 | 11 | 12 | 13 |

PMIC N/A

**STANDARDIZED MILITARY DRAWING**

THIS DRAWING IS AVAILABLE FOR USE BY ALL DEPARTMENTS AND AGENCIES OF THE DEPARTMENT OF DEFENSE

AMSC N/A

PREPARED BY
Monica Poelking

CHECKED BY
Monica Poelking

APPROVED BY
Michael Frye

DRAWING APPROVAL DATE
89-09-07

REVISION LEVEL
A

DEFENSE ELECTRONICS SUPPLY CENTER
DAYTON, OHIO 45444

MICROCIRCUITS, DIGITAL, HIGH SPEED CMOS, QUAD 2-INPUT NAND SCHMITT TRIGGER, MONOLITHIC SILICON

| SIZE | CAGE CODE | 5962-89845 |
|---|---|---|
| A | 67268 | |

SHEET 1 OF 13

1. SCOPE

1.1 Scope. This drawing describes device requirements for class B microcircuits in accordance with 1.2.1 of MIL-STD-883, "Provisions for the use of MIL-STD-883 in conjunction with compliant non-JAN devices".

1.2 Part or Identifying Number (PIN). The complete PIN shall be as shown in the following example:


1.2.1 Device type(s). The device type(s) shall identify the circuit function as follows:

| Device type | Generic number | Circuit function |
|---|---|---|
| 01 | 54HCT132 | Quad 2-input NAND Schmitt trigger, TTL compatible inputs |
| 02 | 54HC132 | Quad 2-input NAND Schmitt trigger |

1.2.2 Case outline(s). The case outline(s) shall be as designated in appendix C of MIL-M-38510, and as follows:

| Outline letter | Case outline |
|---|---|
| C | D-1 (14-lead, .785" x .310" x .200"), dual-in-line package |
| D | F-2 (14-lead, .390" x .260" x .085"), flat package |
| 2 | C-2 (20 terminal, .358" x .358" x .100"), leadless chip carrier package |

1.3 Absolute maximum ratings. 1/

| | |
|---|---|
| Supply voltage range | -0.5 V dc to +7.0 V dc |
| DC input voltage range | -0.5 V dc to $V_{CC}$ + 0.5 V dc |
| DC output voltage range | -0.5 V dc to $V_{CC}$ + 0.5 V dc |
| DC input clamp diode current | ±20 mA |
| DC output clamp diode current (per pin) | ±20 mA |
| DC output current (per pin) | ±25 mA |
| DC $V_{CC}$ or GND current | ±50 mA |
| Storage temperature range | -65°C to +150°C |
| Maximum power dissipation ($P_D$) | 500 mW 2/ |
| Lead temperature (soldering, 10 seconds) | +300°C |
| Thermal resistance, junction-to-case ($\Theta_{JC}$) | See MIL-M-38510, appendix C |
| Junction temperature ($T_J$) | +175°C |

1.4 Recommended operating conditions.

| | |
|---|---|
| Supply voltage range ($V_{CC}$): | |
| Device type 01 | +4.5 V dc to +5.5 V dc |
| Device type 02 | +2.0 V dc to +6.0 V dc |
| Input voltage range ($V_{IN}$) | 0.0 V dc to $V_{CC}$ |
| Output voltage range ($V_{OUT}$) | 0.0 V dc to $V_{CC}$ |
| Case operating temperature range ($T_C$) | -55°C to +125°C |
| Input rise or fall time ($t_r$, $t_f$): | |
| $V_{CC}$ = 4.5 V | 0 to unlimited |

1/ Unless otherwise specified, all voltages are referenced to ground. Stresses above the absolute maximum rating may cause permanent damage to the device. Extended operation at the maximum levels may degrade performance and affect reliability.

2/ For $T_C$ = +100°C to +125°C, derate linearly at 8 mW/°C to 300 mW/°C for case outline C, derate linearly at 12 mW/°C for case outlines D and 2.

2. APPLICABLE DOCUMENTS

2.1 Government specification, standard, and bulletin. Unless otherwise specified, the following specification, standard, and bulletin of the issue listed in that issue of the Department of Defense Index of Specifications and Standards specified in the solicitation, form a part of this drawing to the extent specified herein.

SPECIFICATION

MILITARY

MIL-M-38510 - Microcircuits, General Specification for.

STANDARD

MILITARY

MIL-STD-883 - Test Methods and Procedures for Microelectronics.

BULLETIN

MILITARY

MIL-BUL-103 - List of Standardized Military Drawings (SMD's).

(Copies of the specification, standard, and bulletin required by manufacturers in connection with specific acquisition functions should be obtained from the contracting activity or as directed by the contracting activity.)

2.2 Order of precedence. In the event of a conflict between the text of this drawing and the references cited herein, the text of this drawing shall take precedence.

3. REQUIREMENTS

3.1 Item requirements. The individual item requirements shall be in accordance with 1.2.1 of MIL-STD-883, "Provisions for the use of MIL-STD-883 in conjunction with compliant non-JAN devices" and as specified herein.

3.2 Design, construction, and physical dimensions. The design, construction, and physical dimensions shall be as specified in MIL-M-38510 and herein.

3.2.1 Case outline(s). The case outline(s) shall be in accordance with 1.2.2 herein.

3.2.2 Terminal connections. The terminal connections shall be as specified on figure 1.

3.2.3 Truth table. The truth table shall be as specified on figure 2.

3.2.4 Logic diagram. The logic diagram shall be as specified on figure 3.

3.2.5 Hysteresis definition, characterization, and test setup. The hysteresis definition, characterization, and test setup shall be as specified on figure 4.

3.3 Electrical performance characteristics. Unless otherwise specified herein, the electrical performance characteristics are as specified in table I and shall apply over the full case operating temperature range.

3.4 Electrical test requirements. The electrical test requirements shall be the subgroups specified in table II. The electrical tests for each subgroup are described in table I.

3.5 Marking. Marking shall be in accordance with MIL-STD-883 (see 3.1 herein). The part shall be marked with the PIN listed in 1.2 herein. In addition, the manufacturer's PIN may also be marked as listed in MIL-BUL-103 (see 6.6 herein).

3.6 Certificate of compliance. A certificate of compliance shall be required from a manufacturer in order to be listed as an approved source of supply in MIL-BUL-103 (see 6.6 herein). The certificate of compliance submitted to DESC-ECC prior to listing as an approved source of supply shall affirm that the manufacturer's product meets the requirements of MIL-STD-883 (see 3.1 herein) and the requirements herein.

TABLE I. Electrical performance characteristics.

| Test | Symbol | Conditions 1/ $-55°C \le T_C \le +125°C$ unless otherwise specified | Device types | Group A subgroups | Limits | | Unit |
|---|---|---|---|---|---|---|---|
| | | | | | Min | Max | |
| Positive going threshold voltage (see figure 4) | $V_{T+}$ | $V_{CC}$ = 4.5 V | 01 | 1, 2, 3 | 1.2 | 1.9 | V |
| | | $V_{CC}$ = 5.5 V 2/ | 01 | | 1.4 | 2.1 | |
| | | $V_{CC}$ = 2.0 V | 02 | | 0.7 | 1.5 | |
| | | $V_{CC}$ = 4.5 V | 02 | | 1.5 | 3.15 | |
| | | $V_{CC}$ = 6.0 V | 02 | | 2.1 | 4.2 | |
| Negative going threshold voltage (see figure 4) | $V_{T-}$ | $V_{CC}$ = 4.5 V | 01 | 1, 2, 3 | 0.5 | 1.2 | V |
| | | $V_{CC}$ = 5.5 V 2/ | 01 | | 0.6 | 1.4 | |
| | | $V_{CC}$ = 2.0 V | 02 | | 0.3 | 1.0 | |
| | | $V_{CC}$ = 4.5 V | 02 | | 0.9 | 2.45 | |
| | | $V_{CC}$ = 6.0 V | 02 | | 1.2 | 3.2 | |
| Hysteresis voltage (see figure 4) | $V_H$ | $V_{CC}$ = 4.5 V | 01 | 1, 2, 3 | 0.4 | 1.4 | V |
| | | $V_{CC}$ = 5.5 V 2/ | 01 | | 0.4 | 1.5 | |
| | | $V_{CC}$ = 2.0 V | 02 | | 0.2 | 1.2 | |
| | | $V_{CC}$ = 4.5 V | 02 | | 0.4 | 2.1 | |
| | | $V_{CC}$ = 6.0 V | 02 | | 0.5 | 2.5 | |

See footnotes at end of table.

TABLE I. Electrical performance characteristics.

| Test | Symbol | Conditions 1/ $-55°C \le T_C \le +125°C$ unless otherwise specified | | Device types | Group A subgroups | Limits | | Unit |
|---|---|---|---|---|---|---|---|---|
| | | | | | | Min | Max | |
| High level output voltage | $V_{OH}$ | $V_{CC}$ = 4.5 V, $V_{IN}$ = $V_T$+ maximum or $V_T$- minimum | CMOS loads $\|I_O\|$ = 20 µA | 01 | 1, 2, 3 | 4.4 | | V |
| | | | TTL loads $\|I_O\|$ = 4.0 mA | 01 | 1 | 3.98 | | |
| | | | | | 2, 3 | 3.7 | | |
| | | $V_{CC}$ = 2.0 V, $V_{IN}$ = $V_T$+ maximum or $V_T$- minimum, $\|I_O\|$ = 20 µA | | 02 | 1, 2, 3 | 1.9 | | |
| | | $V_{CC}$ = 4.5 V, $V_{IN}$ = $V_T$+ maximum or $V_T$- minimum, $\|I_O\|$ = 20 µA | | 02 | | 4.4 | | |
| | | $V_{CC}$ = 6.0 V, $V_{IN}$ = $V_T$+ maximum or $V_T$- minimum, $\|I_O\|$ = 20 µA | | 02 | | 5.9 | | |
| | | $V_{CC}$ = 4.5 V, $V_{IN}$ = $V_T$+ maximum or $V_T$- minimum, $\|I_O\|$ = 4.0 mA | | 02 | | 3.7 | | |
| | | $V_{CC}$ = 6.0 V, $V_{IN}$ = $V_T$+ maximum or $V_T$- minimum, $\|I_O\|$ = 5.2 mA | | 02 | | 5.2 | | |

See footnotes at end of table.

TABLE I. Electrical performance characteristics.

| Test | Symbol | Conditions 1/ $-55°C \le T_C \le +125°C$ unless otherwise specified | | Device types | Group A subgroups | Limits Min | Limits Max | Unit |
|---|---|---|---|---|---|---|---|---|
| Low level output voltage | $V_{OL}$ | $V_{CC}$ = 4.5 V, $V_{IN}$ = $V_T$+ maximum or $V_T$- minimum | CMOS loads $\|I_O\|$ = 20 µA | 01 | 1, 2, 3 | | 0.1 | V |
| | | | TTL loads $\|I_O\|$ = 4.0 mA | 01 | 1 | | 0.26 | |
| | | | | | 2, 3 | | 0.4 | |
| | | $V_{CC}$ = 2.0 V, $V_{IN}$ = $V_T$+ minimum or $V_T$- maximum, $\|I_O\|$ = 20 µA | | 02 | 1, 2, 3 | | 0.1 | |
| | | $V_{CC}$ = 4.5 V, $V_{IN}$ = $V_T$+ minimum or $V_T$- maximum, $\|I_O\|$ = 20 µA | | 02 | | | 0.1 | |
| | | $V_{CC}$ = 6.0 V, $V_{IN}$ = $V_T$+ minimum or $V_T$- maximum, $\|I_O\|$ = 20 µA | | 02 | | | 0.1 | |
| | | $V_{CC}$ = 4.5 V, $V_{IN}$ = $V_T$+ minimum or $V_T$- maximum, $\|I_O\|$ = 4.0 mA | | 02 | | | 0.4 | |
| | | $V_{CC}$ = 6.0 V, $V_{IN}$ = $V_T$+ minimum or $V_T$- maximum, $\|I_O\|$ = 5.2 mA | | 02 | | | 0.4 | |
| Input leakage current | $I_{IN}$ | $V_{CC}$ = 5.5 V, $V_{IN}$ = $V_{CC}$ or GND | | 01 | 1 | | ±0.1 | µA |
| | | | | | 2, 3 | | ±1.0 | |
| | | $V_{CC}$ = 6.0 V, $V_{IN}$ = $V_{CC}$ or GND | | 02 | 1, 2, 3 | | ±1.0 | |

See footnotes at end of table.

TABLE I. Electrical performance characteristics.

| Test | Symbol | Conditions 1/ $-55°C \le T_C \le +125°C$ unless otherwise specified | Device types | Group A subgroups | Limits Min | Limits Max | Unit |
|---|---|---|---|---|---|---|---|
| Quiescent supply current | $I_{CC}$ | $V_{CC}$ = 5.5 V, $V_{IN}$ = $V_{CC}$ or GND, $I_{OUT}$ = 0 µA | 01 | 1 | | 2.0 | µA |
| | | | | 2, 3 | | 40 | |
| | | $V_{CC}$ = 6.0 V, $V_{IN}$ = $V_{CC}$ or GND, $I_{OUT}$ = 0 µA | 02 | 1, 2, 3 | | 40 | |
| Additional quiescent supply current | $\Delta I_{CC}$ | Any 1 input: 2/ $V_{IN}$ = 2.4 V, Other inputs: $V_{IN}$ = $V_{CC}$ or GND, $I_{OUT}$ = 0.0 A, $V_{CC}$ = 5.5 V | 01 | 1, 2, 3 | | 1.08 | mA |
| Input capacitances | $C_{IN}$ | See 4.3.1c | All | 4 | | 10 | pF |
| Power dissipation capacitance | $C_{PD}$ | See 4.3.1c 3/ | All | 4 | | 40 | pF |
| Functional tests | | See 4.3.1d | All | 7, 8 | | | |
| Propagation delay time, A to Y, B to Y | $t_{PHL}$, $t_{PLH}$ | $V_{CC}$ = 4.5 V, $C_L$ = 50 pF minimum, See figure 5 | 01 | 9 | | 33 | ns |
| | | | | 10, 11 | | 50 | |
| | | $V_{CC}$ = 2.0 V, $C_L$ = 50 pF, See figure 5 | 02 | 9 | | 125 | |
| | | | | 10, 11 | | 190 | |
| | | $V_{CC}$ = 4.5 V, $C_L$ = 50 pF, See figure 5 | 02 | 9 | | 25 | |
| | | | | 10, 11 | | 38 | |
| | | $V_{CC}$ = 6.0 V, $C_L$ = 50 pF, See figure 5 | 02 | 9 | | 21 | |
| | | | | 10, 11 | | 32 | |

See footnotes at end of table.

TABLE I. Electrical performance characteristics - Continued.

| Test | Symbol | Conditions 1/ $-55°C \le T_C \le +125°C$ unless otherwise specified | Device types | Group A subgroups | Limits Min | Limits Max | Unit |
|---|---|---|---|---|---|---|---|
| Output transition time 4/ | $t_{TLH}$, $t_{THL}$ | $V_{CC}$ = 4.5 V, $C_L$ = 50 pF minimum, See figure 5 | 01 | 9 | | 15 | ns |
| | | | | 10, 11 | | 22 | |
| | | $V_{CC}$ = 2.0 V, $C_L$ = 50 pF, See figure 5 | 02 | 9 | | 75 | |
| | | | | 10, 11 | | 110 | |
| | | $V_{CC}$ = 4.5 V, $C_L$ = 50 pF, See figure 5 | 02 | 9 | | 15 | |
| | | | | 10, 11 | | 22 | |
| | | $V_{CC}$ = 6.0 V, $C_L$ = 50 pF, See figure 5 | 02 | 9 | | 13 | |
| | | | | 10, 11 | | 19 | |

1/ For a power supply of 5 V ±10 percent, the worst case output voltages ($V_{OH}$ and $V_{OL}$) occur for HC and HCT at 4.5 V. Thus, the 4.5 V values should be used when designing with this supply. Worst cases $V_{IH}$ and $V_{IL}$ occur at $V_{CC}$ = 5.5 V and 4.5 V respectively. (The $V_{IH}$ value at 5.5 V is 3.85 V.) The worst case leakage current ($I_{IN}$, $I_{CC}$, and $I_{OZ}$) occur for CMOS at a higher voltage and so the 6.0 V values for HC and 5.5 V for HCT should be used. Power dissipation capacitance ($C_{PD}$), typically 100 pF, determines the no load dynamic power consumption, $P_D = C_{PD} V_{CC}^2 f + I_{CC} V_{CC}$ for HC and $P_D = C_{PD} V_{CC}^2 f + I_{CC} V_{CC} + n \Delta I_{CC} V_{CC}$ for HCT where the n represents the number of inputs of TTL voltage levels. The no load dynamic current consumption, $I_S = C_{PD} V_{CC} f + I_{CC}$ for HC and $I_S = C_{PD} V_{CC} f + I_{CC} + n \Delta I_{CC}$ for HCT, where the n represents the number of inputs at TTL voltage levels.

2/ This test is guaranteed, if not tested, to the limits specified in table I.

3/ Power dissipation capacitance ($C_{PD}$), determines the dynamic power consumption, $P_D$ (total) = $(C_{PD} + C_L) V_{CC}^2 f + (V_{CC} \times I_{CC}) + n (\Delta I_{CC} \times V_{CC} d$, and the dynamic current consumption ($I_S$) is, $I_S = (C_{PD} + C_L) V_{CC} f$.

Where: $P_D$ = dynamic power dissipation.
$C_L$ = load capacitance on each output.
$C_{PD}$ = power dissipation capacitance of the device.
f = input switching frequency.
n = number of inputs switching.
d = duty cycle.

4/ Transition time ($t_{TLH}$, $t_{THL}$), if not tested, shall be guaranteed to the specified limits in table I.

| Device types | 01 and 02 | |
|---|---|---|
| Case outlines | C and D | 2 |
| Terminal number | Terminal symbol | |
| 1 | A1 | NC |
| 2 | B1 | A1 |
| 3 | Y1 | B1 |
| 4 | A2 | Y1 |
| 5 | B2 | NC |
| 6 | Y2 | A2 |
| 7 | GND | NC |
| 8 | Y3 | B2 |
| 9 | A3 | Y2 |
| 10 | B3 | GND |
| 11 | Y4 | NC |
| 12 | A4 | Y3 |
| 13 | B4 | A3 |
| 14 | $V_{CC}$ | B3 |
| 15 | --- | NC |
| 16 | --- | Y4 |
| 17 | --- | NC |
| 18 | --- | A4 |
| 19 | --- | B4 |
| 20 | --- | $V_{CC}$ |

NC = No connection.

FIGURE 1. Terminal connections.

| Inputs | | Output |
|---|---|---|
| A | B | Y |
| L | L | H |
| L | H | H |
| H | L | H |
| H | H | L |

H = High voltage level
L = Low voltage level

FIGURE 2. Truth table.

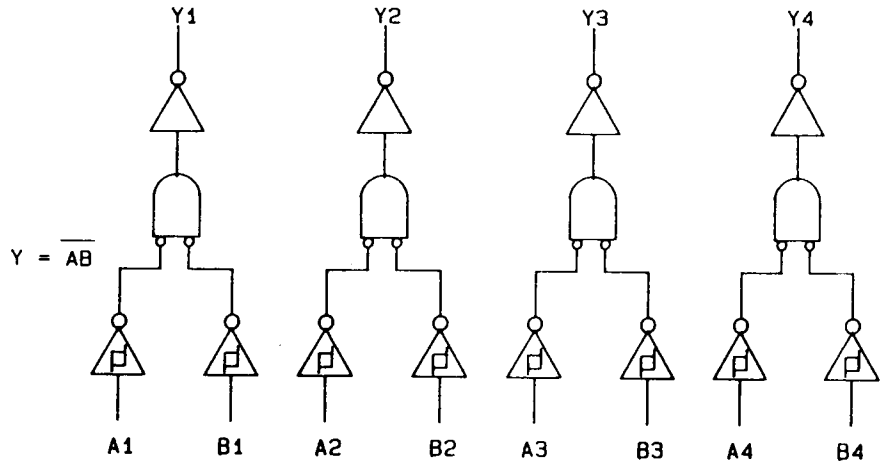
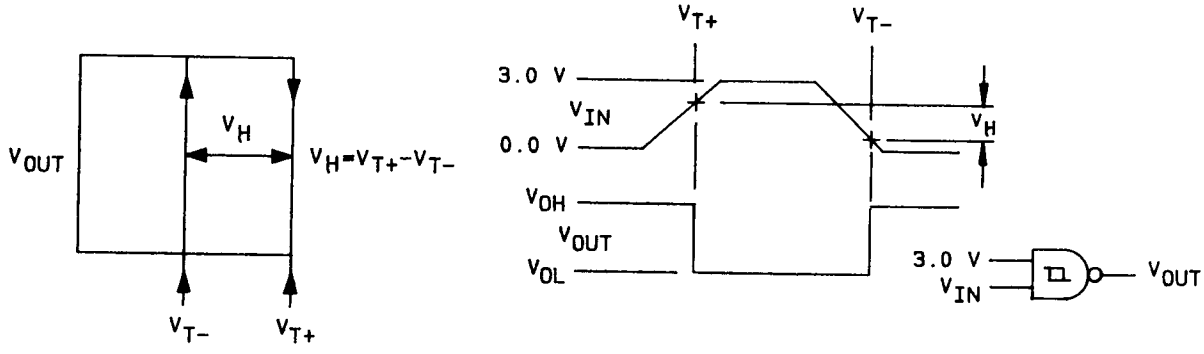



FIGURE 3. Logic diagram.

Device type 01




Device type 02

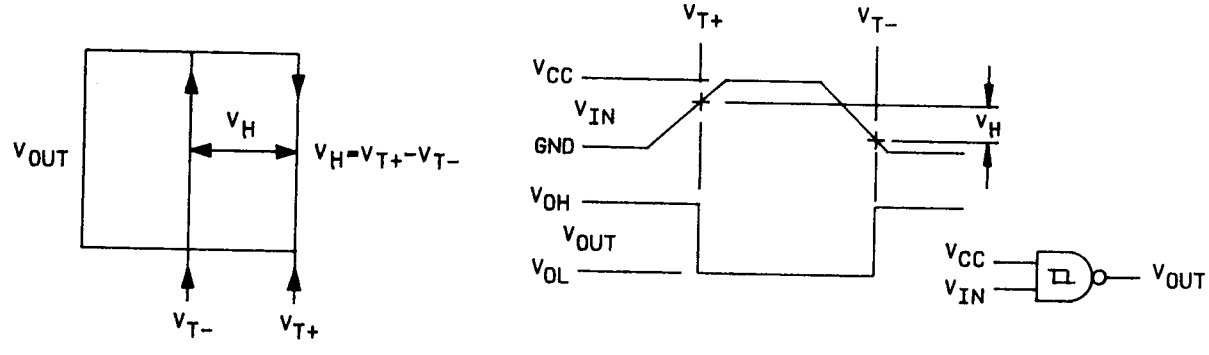
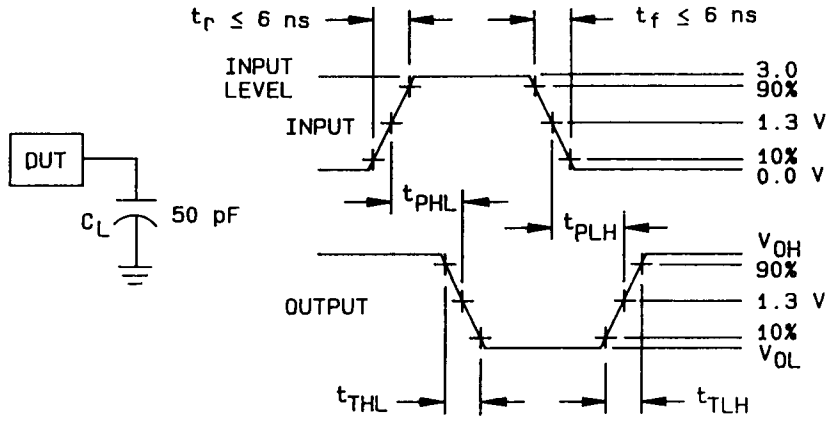
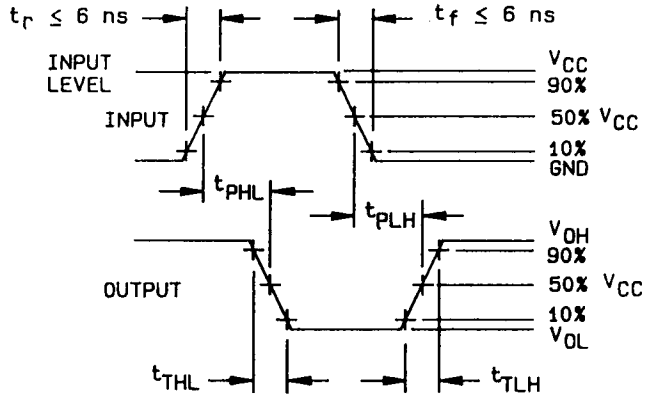



FIGURE 4. Hysteresis definition, characterization, and test setup.

Device type 01




Device type 02




$C_L$ = 50 pF, includes probe and jig capacitance.

FIGURE 5. Test circuit and switching waveforms.

3.7 Certificate of conformance. A certificate of conformance as required in MIL-STD-883 (see 3.1 herein) shall be provided with each lot of microcircuits delivered to this drawing.

3.8 Notification of change. Notification of change to DESC-ECC shall be required in accordance with MIL-STD-883 (see 3.1 herein).

3.9 Verification and review. DESC, DESC's agent, and the acquiring activity retain the option to review the manufacturer's facility and applicable required documentation. Offshore documentation shall be made available onshore at the option of the reviewer.

4. QUALITY ASSURANCE PROVISIONS

4.1 Sampling and inspection. Sampling and inspection procedures shall be in accordance with section 4 of MIL-M-38510 to the extent specified in MIL-STD-883 (see 3.1 herein).

4.2 Screening. Screening shall be in accordance with method 5004 of MIL-STD-883, and shall be conducted on all devices prior to quality conformance inspection. The following additional criteria shall apply:

a. Burn-in test, method 1015 of MIL-STD-883.

(1) Test condition A, B, C, or D using the circuit submitted with the certificate of compliance (see 3.6 herein).

(2) $T_A$ = +125°C, minimum.

b. Interim and final electrical test parameters shall be as specified in table II herein, except interim electrical parameter tests prior to burn-in are optional at the discretion of the manufacturer.

4.3 Quality conformance inspection. Quality conformance inspection shall be in accordance with method 5005 of MIL-STD-883 including groups A, B, C, and D inspections. The following additional criteria shall apply.

4.3.1 Group A inspection.

a. Tests shall be as specified in table II herein.

b. Subgroups 5 and 6 in table I, method 5005 of MIL-STD-883 shall be omitted.

c. Subgroup 4 ($C_{IN}$ and $C_{PD}$ measurements) shall be measured only for the initial test and after process or design changes which may affect input capacitance. Capacitance shall be measured between the designated terminal and GND at a frequency of 1 MHz. Test all applicable pins on five devices with zero failures.

d. Subgroups 7 and 8 shall include verification of the truth table.

4.3.2 Groups C and D inspections.

a. End-point electrical parameters shall be as specified in table II herein.

b. Steady-state life test conditions, method 1005 of MIL-STD-883.

(1) Test condition A, B, C, or D using the circuit submitted with the certificate of compliance (see 3.6 herein).

(2) $T_A$ = +125°C, minimum.

(3) Test duration: 1,000 hours, except as permitted by method 1005 of MIL-STD-883.

TABLE II. Electrical test requirements.

| MIL-STD-883 test requirements | Subgroups (per method 5005, table I) |
|---|---|
| Interim electrical parameters (method 5004) (method 5004) | --- |
| Final electrical test parameters (method 5004) | 1*, 2, 3, 7, 8, 9 |
| Group A test requirements (method 5005) | 1, 2, 3, 4, 7, 8, 9, 10**, 11** |
| Groups C and D end-point electrical parameters (method 5005) | 1, 2, 3 |

* PDA applies to subgroup 1.
** Subgroups 10 and 11, if not tested, shall be guaranteed to the specified limits in table I.

5. PACKAGING

5.1 Packaging requirements. The requirements for packaging shall be in accordance with MIL-M-38510.

6. NOTES

6.1 Intended use. Microcircuits conforming to this drawing are intended for use when military specifications do not exist and qualified military devices that will perform the required function are not available for OEM application. When a military specification exists and the product covered by this drawing has been qualified for listing on QPL-38510, the device specified herein will be inactivated and will not be used for new design. The QPL-38510 product shall be the preferred item for all applications.

6.2 Replaceability. Replaceability is determined as follows:

a. Microcircuits covered by this drawing will replace the same generic device covered by a contractor-prepared specification or drawing.

b. When a QPL source is established, the device specified in this drawing will be replaced by the microcircuit identified as PIN M38510/65005XXX.

6.3 Configuration control of SMD's. All proposed changes to existing SMD's will be coordinated with the users of record for the individual documents. This coordination will be accomplished in accordance with MIL-STD-481 using DD Form 1693, Engineering Change Proposal (Short Form).

6.4 Record of users. Military and industrial users shall inform Defense Electronics Supply Center when a system application requires configuration control and the applicable SMD. DESC will maintain a record of users and this list will be used for coordination and distribution of changes to the drawings. Users of drawings covering microelectronics devices (FSC 5962) should contact DESC-ECC, telephone (513) 296-6022.

6.5 Comments. Comments on this drawing should be directed to DESC-ECC, Dayton, Ohio 45444, or telephone (513) 296-8525.

6.6 Approved sources of supply. Approved sources of supply are listed in MIL-BUL-103. The vendors listed in MIL-BUL-103 have agreed to this drawing and a certificate of compliance (see 3.6 herein) has been submitted to and accepted by DESC-ECC.