REVISIONS			
LTR	DESCRIPTION	DATE (YR-MO-DA)	APPROVED
A	Add changes in accordance with NOR 5962-R200-93.	93-07-08	M. A. Frye
B	Add device type 04. Format update, editorial changes throughout.	95-11-27	M. A. Frye

REV																			
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SHEET																			

REV STATUS OF SHEETS	REV	B	B	B	B	B	B	B	B	B	B	B	B	B	B
	SHEET	1	2	3	4	5	6	7	8	9	10	11	12	13	14

PMIC N/A

STANDARD MICROCIRCUIT DRAWING

THIS DRAWING IS AVAILABLE FOR USE BY ALL DEPARTMENTS AND AGENCIES OF THE DEPARTMENT OF DEFENSE

AMSC N/A

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DRAWING APPROVAL DATE
90-01-26

REVISION LEVEL
B

DEFENSE ELECTRONICS SUPPLY CENTER
DAYTON, OHIO 45444

MICROCIRCUIT, MEMORY, DIGITAL, CMOS, 8K X 9 SRAM (STANDARD POWER), MONOLITHIC SILICON

SIZE	CAGE CODE	
A	67268	**5962-89883**

SHEET 1 OF 14

DESC FORM 193
JUL 94

5962-E302-95

DISTRIBUTION STATEMENT A. Approved for public release; distribution is unlimited.

1. SCOPE

1.1 Scope. This drawing describes device requirements for class B microcircuits in accordance with 1.2.1 of MIL-STD-883, "Provisions for the use of MIL-STD-883 in conjunction with compliant non-JAN devices".

1.2 Part or Identifying Number (PIN). The complete PIN shall be as shown in the following example:

1.2.1 Device types. The device types shall identify the circuit function as follows:

Device type	Generic number	Circuit function	Toggle speed
01	See 6.6	8192 X 9 CMOS static RAM	55 ns
02	See 6.6	8192 X 9 CMOS static RAM	45 ns
03	See 6.6	8192 X 9 CMOS static RAM	35 ns
04	See 6.6	8192 X 9 CMOS static RAM	35 ns

1.2.2 Case outline(s). The case outline(s) shall be as designated in MIL-STD-1835 and as follows:

Outline letter	Descriptive designator	Terminals	Package style
X	CDIP3-T28 and GDIP4-T28	28	dual-in-line package
Y	CDFP4-F28	28	flat package
Z	CQCC3-N28	28	rectangular chip carrier package

1.3 Absolute maximum ratings.

Supply voltage to ground potential range	-0.5 V dc to +7.0 V dc
DC voltage applied to outputs range	-0.5 V dc to +7.0 V dc
DC input voltage range	-0.5 V dc to V_{CC} + 0.5 V dc
DC output current	20 mA
Storage temperature range	-65°C to +150°C
Maximum power dissipation (P_D)	1.0 W
Lead temperature (soldering, 10 seconds)	+300°C
Thermal resistance, junction-to-case (θ_{JC}):	
Cases X and Z	See MIL-STD-1835
Case Y	30°C/W
Junction temperature (T_J)	+150°C 1/

1.4 Recommended operating conditions.

Supply voltage range (V_{CC})	4.5 V dc to 5.5 V dc
High level input voltage range (V_{IH})	2.2 V dc to V_{CC} + 0.5 V dc
Low level input voltage range (V_{IL})	-0.3 V dc to +0.8 V dc
Case operating temperature range (T_C)	-55°C to +125°C

2. APPLICABLE DOCUMENTS

2.1 Government specification, standards,and bulletin. Unless otherwise specified, the following specification, standards, and bulletin of the issue listed in that issue of the Department of Defense Index of Specifications and Standards specified in the solicitation, form a part of this drawing to the extent specified herein.

SPECIFICATION

MILITARY

MIL-PRF-38535 - Microcircuits, General Specification for.

1/ Maximum junction temperature may be increased to +175°C during burn-in and steady-state life.

STANDARD

MILITARY

MIL-STD-883 - Test Methods and Procedures for Microelectronics.
MIL-STD-1835 - Microcircuit Case Outlines.

BULLETIN

MILITARY

MIL-BUL-103 - List of Standard Microcircuits Drawings (SMD's).

(Copies of the specification, standard, and bulletin required by manufacturers in connection with specific acquisition functions should be obtained from the contracting activity or as directed by the contracting activity.)

2.2 Order of precedence. In the event of a conflict between the text of this drawing and the references cited herein, the text of this drawing shall take precedence.

3. REQUIREMENTS

3.1 Item requirements. The individual item requirements shall be in accordance with 1.2.1 of MIL-STD-883, "Provisions for the use of MIL-STD-883 in conjunction with compliant non-JAN devices" and as specified herein. Product built to this drawing that is produced by a Qualified Manufacturer Listing (QML) certified and qualified manufacturer or a manufacturer who has been granted transitional certification to MIL-PRF-38535 may be processed as QML product in accordance with the manufacturers approved program plan and qualifying activity approval in accordance with MIL-PRF-38535. This QML flow as documented in the Quality Management (QM) plan may make modifications to the requirements herein. These modifications shall not affect form, fit, or function of the device. These modifications shall not affect the PIN as described herein. A "Q" or "QML" certification mark in accordance with MIL-PRF-38535 is required to identify when the QML flow option is used.

3.2 Design, construction, and physical dimensions. The design, construction, and physical dimensions shall be as specified in MIL-STD-883 (see 3.1 herein) and herein.

3.2.1 Terminal connections. The terminal connections shall be as specified on figure 1.

3.2.2 Truth table. The logic block diagram shall be as specified on figure 2.

3.2.3 Case outline. The case outline shall be in accordance with 1.2.2 herein.

3.2.4 Die overcoat. Polyimide and silicone coatings are allowable as an overcoat on the die for alpha particle protection provided that each coated microcircuit inspection lot (as defined in MIL-PRF-38535) shall be subjected to and pass the internal moisture content test, (method 1018 of MIL-STD-883), the frequency of the internal water vapor testing may not be decreased unless approved by the preparing activity.

3.3 Electrical performance characteristics. Unless otherwise specified herein, the electrical performance characteristics are as specified in table I and apply over the full case operating temperature range.

3.4 Electrical test requirements. The electrical test requirements shall be the subgroups specified in table II. The electrical tests for each subgroup are described in table I.

3.5 Marking. Marking shall be in accordance with MIL-STD-883 (see 3.1 herein). The part shall be marked with the PIN listed in 1.2 herein. In addition, the manufacturer's PIN may also be marked as listed in MIL-BUL-103 (see 6.7 herein).

3.6 Certificate of compliance. A certificate of compliance shall be required from a manufacturer in order to be listed as an approved source of supply in MIL-BUL-103 (see 6.7 herein). The certificate of compliance submitted to DESC-ECS prior to listing as an approved source of supply shall affirm that the manufacturer's product meets the requirements of MIL-STD-883 (see 3.1 herein) and the requirements herein.

3.7 Certificate of conformance. A certificate of conformance as required in MIL-STD-883 (see 3.1 herein) shall be provided with each lot of microcircuits delivered to this drawing.

3.8 Notification of change. Notification of change to DESC-ECS shall be required in accordance with MIL-STD-883 (see 3.1 herein).

3.9 Verification and review. DESC, DESC's agent, and the acquiring activity retain the option to review the manufacturer's facility and applicable required documentation. Offshore documentation shall be made available onshore at the option of the reviewer.

TABLE I. Electrical performance characteristics.

Test	Symbol	Conditions $4.5\ V \le V_{CC} \le 5.5\ V$, $-55°C \le T_C \le +125°C$ unless otherwise specified	Group A subgroups	Device type	Limits		Unit
					Min	Max	
High level output voltage	V_{OH}	V_{CC} = 4.5 V, I_{OH} = -4.0 mA, V_{IL} = 0.8 V, V_{IH} = 2.2 V	1,2,3	All	2.4		V
Low level output voltage	V_{OL}	V_{CC} = 5.5 V, I_{OL} = 4.0 mA, V_{IL} = 0.8 V, V_{IH} = 2.2 V	1,2,3	All		0.4	V
Input load current	I_I	V_{IN} = 0 V and 5.5 V, V_{CC} = 5.5 V	1,2,3	All	-10	+10	µA
Output current high impedance	I_{OZ}	V_{IN} = 0 V and 5.5 V, V_{CC} = 5.5 V with no load	1,2,3	All	-10	+10	µA
Operating supply current	I_{CC1}	$\overline{W}$, $\overline{E}$ = V_{IL}, S = V_{IH}, V_{CC} = V_{IN} = 5.5 V, I_O = 0 mA, f = 1/tAVAV, Addresses = 0.8 to 2.2 V	1,2,3	All		140	mA
Standby supply current, TTL level inputs	I_{CC2}	f = 0 MHz, all other inputs ≤ V_{IL} or ≥ V_{IH}, V_{CC} = 5.5 V, $\overline{E}$ ≥ V_{IH}	1,2,3	All		30	mA
Standby supply current, CMOS level inputs	I_{CC3}	f = 0 MHz, V_{IN} ≤ 0.2 V or V_{IN} ≥ V_{CC} - 0.2 V, V_{CC} = 5.5 V, V_{CC} - 0.2 V ≤ $\overline{E}$	1,2,3	01,02,03		1.0	mA
				04		10	
Input capacitance	C_{IN}	V_{CC} = 5.0 V, f = 1 MHz, V_{IN}, V_{OUT} = 0 V, TA = +25°C, See 4.3.1c	4	All	---	10	pF
Output capacitance	C_{OUT}			All		12	pF
Functional test	FT	See 4.4.1d	7,8A,8B	All			
Read cycle time	t_{AVAV}	See figure 3 and 4 1/	9,10,11	01	55		ns
				02	45		
				03,04	35		
Address valid to data valid	t_{AVQV}		9,10,11	01		55	ns
				02		45	
				03,04		35	
Output hold from address change	t_{AVQX}		9,10,11	All	5.0		ns
Chip enable access time	t_{ELQV}		9,10,11	01		55	ns
						30	
	t_{SHQV}			02		45	
						25	
				03		35	
						20	
				04		35	
						25	

See footnotes at end of table.

TABLE I. Electrical performance characteristics - Continued.

Test	Symbol	Conditions $4.5\ V \le V_{CC} \le 5.5\ V$ $-55°C \le T_C \le +125°C$ unless otherwise specified	Group A subgroups	Device type	Limits		Unit
					Min	Max	
Chip enable to output in low Z	t_{ELQX} t_{SHQX}	See figures 3 and 4 2/	9,10,11	All	5.0		ns
Chip disable to output in high Z	t_{EHQZ} t_{SLQZ}	See figures 3 and 4 2/ 3/	9,10,11	01		35	ns
				02		25	
				03,04		20	
Output enable low to data valid	t_{GLQV}	See figures 3 and 4 1/	9,10,11	01		30	ns
				02		25	
				03,04		20	
Output enable low to low Z	t_{GLQX}	See figures 3 and 4 2/	9,10,11	All	5.0		ns
Output enable high to high Z	t_{GHQZ}	See figures 3 and 4 2/ 3/	9,10,11	01		30	ns
				02		25	
				03,04		20	
Write cycle time	t_{AVAV}	See figures 3 and 4 1/	9,10,11	01	55		ns
				02	45		
				03,04	35		
Chip enable time to end of write	t_{ELWH}, t_{ELEH}		9,10,11	01	45		ns
					30		
	t_{SHWH}, t_{SHSL}			02	40		
					25		
				03	30		
					20		
				04	30		
					30		
Address setup to write end	t_{AVWH}		9,10,11	01	50		ns
				02	35		
				03,04	30		
Address hold from write end (write recovery)	t_{WHAX}, t_{EHAX}, t_{SLAX}		9,10,11	All	0		ns
Address setup to write start	t_{AVWL}, t_{AVEL}, t_{AVSH}		9,10,11	All	0		ns
Write enable pulse width	t_{WLWH}, t_{WLEH}, t_{WLSL}		9,10,11	01	30		ns
				02,04	25		
				03	20		

See footnotes at end of table.

TABLE I. Electrical performance characteristics - Continued.

Test	Symbol	Conditions $4.5\ V \le V_{CC} \le 5.5\ V$, $-55°C \le T_C \le +125°C$ unless otherwise specified	Group A subgroups	Device type	Limits		Unit
					Min	Max	
Data setup to write end	t_{DVWH}, t_{DVEH}, t_{DVSL}	See figures 3 and 4 1/	9,10,11	01	30		ns
				02,04	20		
				03	15		
Data hold from write end	t_{EHDX}, t_{WHDX}, t_{SLDX}		9,10,11	All	0		ns
Write enable to output in high Z	t_{WLQZ}	See figures 3 and 4 2/ 3/	9,10,11	01		25	ns
				02		20	
				03,04		15	
Output active from end of write	t_{WHQX}	See figures 3 and 4 2/	9,10,11	All	5.0		ns

1/ Test conditions assume signal transition times of 5.0 ns or less. Timing is referenced at input and output levels of 1.5 V. Output loading is equivalent to the specified I_{OL}/I_{OH} with a load capacitance of 30 pF (see figure 4).

2/ If not tested, shall be guaranteed to the limits specified in table I.

3/ Test conditions assume signal transition times of 5.0 ns or less. Transition is measured at steady-state high level -500 mV or steady-state low level +500 mV on the output from 1.5 V level on the input with a load capacitance of 5.0 pF (see figure 4).

4. QUALITY ASSURANCE PROVISIONS

4.1 Sampling and inspection. Sampling and inspection procedures shall be in accordance with MIL-STD-883 (see 3.1 herein).

4.2 Screening. Screening shall be in accordance with method 5004 of MIL-STD-883, and shall be conducted on all devices prior to quality conformance inspection. The following additional criteria shall apply:

a. Burn-in test, method 1015 of MIL-STD-883.

(1) Test condition C or D using the circuit submitted with the certificate of compliance (see 3.6 herein). The test circuit shall be maintained by the manufacturer under document revision level control and shall be made available to the preparing or acquiring activity upon request. The test circuit shall specify the inputs, outputs, biases, and power dissipation, as applicable, in accordance with the intent specified in test method 1015 of MIL-STD-883.

(2) T_A = +125°C, minimum.

b. Interim and final electrical test parameters shall be as specified in table II herein, except interim electrical parameter tests prior to burn-in are optional at the discretion of the manufacturer.

Device types	All
Case outlines	X, Y, and Z
Terminal number	Terminal symbol
1	A
2	A
3	A
4	A
5	A
6	A
7	A
8	A
9	A
10	I/O_1
11	I/O_2
12	I/O_3
13	I/O_4
14	V_{SS}
15	I/O_5
16	I/O_6
17	I/O_7
18	I/O_8
19	I/O_9
20	$\overline{E}$
21	A
22	$\overline{G}$
23	A
24	A
25	A
26	S
27	$\overline{W}$
28	V_{CC}

FIGURE 1. Terminal connections.

$\overline{E}$	S	$\overline{G}$	$\overline{W}$	Mode	I/O
H	X	X	X	Not selected	High Z
X	L	X	X	Not selected	High Z
L	H	H	H	Data out disabled	High Z
L	H	L	H	Read	Data out
L	H	X	L	Write	Data in

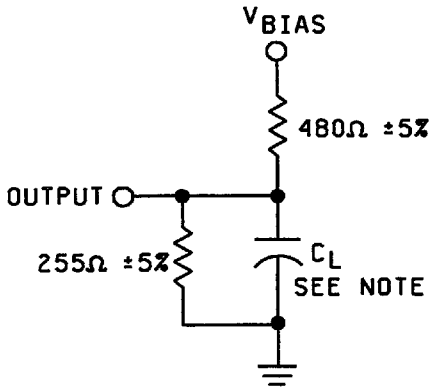
H = Logic 1 state

L = Logic 0 state

X = Don't care

High Z = High impedance state

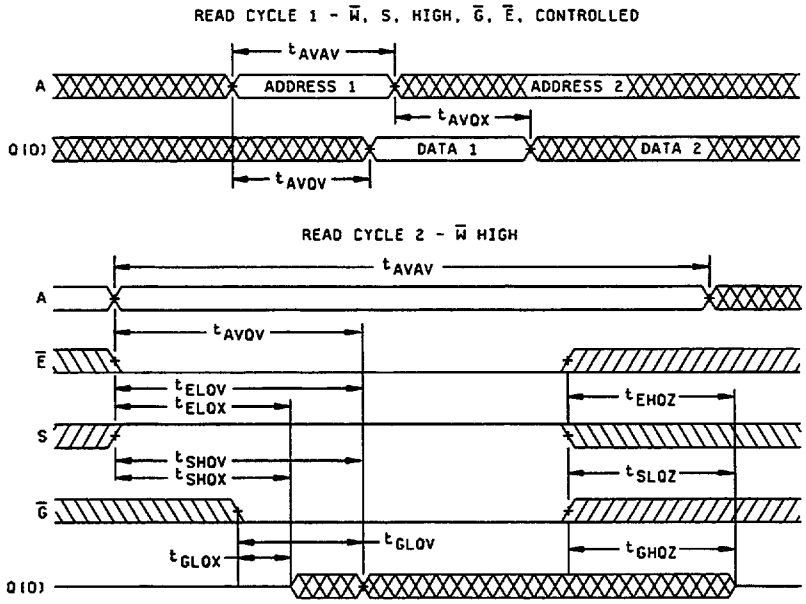
FIGURE 2. Truth table.



NOTES: C_L including scope and jig capacitance (mimimum)
Logic level "0" V_{BIAS} = 5.0 V
Logic level "1" V_{BIAS} = 3.5 V

MEASUREMENT	C_L
tEHQZ, tGHQZ, tSLQZ, and tWLQZ	C_L = 5.0 pF
All others	C_L = 30 pF

FIGURE 3. Output load circuit.



NOTES:

1. $\overline{W}$ is high for READ cycle.
2. Read cycle time is measured from the last valid address to the first transitioning address.
3. Transition is measured ±500 mV from steady state voltage prior to change (t_{EHQZ}, t_{SLQZ}, and t_{GHQZ}).
4. $\overline{E}$ is low, S is high, $\overline{G}$ is low for READ cycle.
5. ADDRESS must be valid prior to, or coincident with, $\overline{E}$ transition low and S transition high.
6. Transitions caused by a chip enable control have similar delays irrespective of whether $\overline{E}$ or S causes them.

FIGURE 4. Timing diagrams.

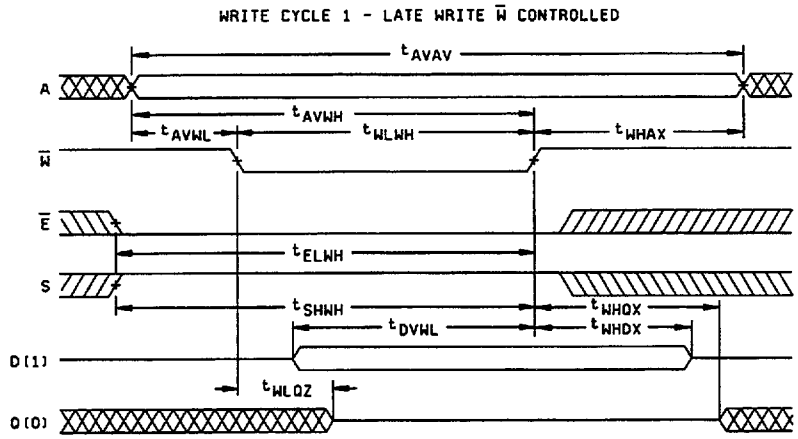
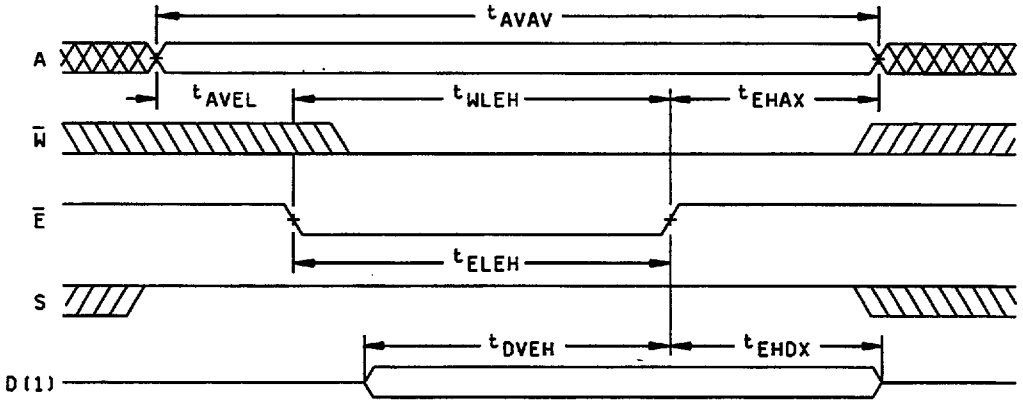
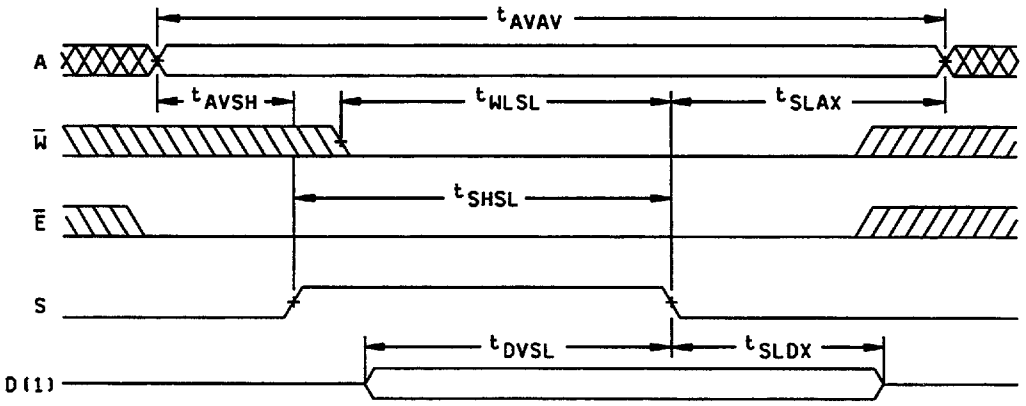


FIGURE 4. Timing diagrams - Continued.

WRITE CYCLE 2 - EARLY WRITE, E CONTROLLED



WRITE CYCLE 3 - EARLY WRITE, S CONTROLLED



NOTES:

1. $\overline{E}$ and $\overline{W}$ must be low, S high, for WRITE cycle.
2. Write cycle time is measured from the last valid address to the first transitioning address.
3. Transition is measured ±500 mV from steady state voltage prior to change.
4. If $\overline{E}$ goes low, or S goes high, simultaneously with $\overline{W}$ low, the output remains in high impedance state.
5. $\overline{G}$ is low for this Write cycle to show tWLQZ and tWHQX.

FIGURE 4. Timing diagrams - Continued.

4.3 Quality conformance inspection. Quality conformance inspection shall be in accordance with method 5005 of MIL-STD-883 including groups A, B, C, and D inspections. The following additional criteria shall apply.

4.3.1 Group A inspection.

a. Tests shall be as specified in table II herein.

b. Subgroups 5 and 6 in table I, method 5005 of MIL-STD-883 shall be omitted.

c. Subgroup 4 (C_{IN} and C_{OUT} measurements) shall be measured only for the initial test and after process or design changes which may affect capacitance. Sample size is 15 devices with no failures, and all input and output terminals tested.

d. Subgroups 7 and 8 shall consist of verifying functionality of the device. These tests form a part of the vendors test tape and shall be maintained and available from the approved sources of supply.

4.3.2 Groups C and D inspections.

a. End-point electrical parameters shall be as specified in table II herein.

b. Steady-state life test conditions, method 1005 of MIL-STD-883.

(1) Test condition C or D using the circuit submitted with the certificate of compliance (see 3.6 herein).

(2) T_A = +125°C, minimum.

(3) Test duration: 1,000 hours, except as permitted by method 1005 of MIL-STD-883.

5. PACKAGING

5.1 Packaging requirements. The requirements for packaging shall be in accordance with MIL-STD-883 (see 3.1 herein).

6. NOTES

6.1 Intended use. Microcircuits conforming to this drawing are intended for use for Government microcircuit applications (original equipment), design applications, and logistics purposes.

6.2 Replaceability. Microcircuits covered by this drawing will replace the same generic device covered by a contractor-prepared specification or drawing.

6.3 Configuration control of SMD's. All proposed changes to existing SMD's will be coordinated with the users of record for the individual documents. This coordination will be accomplished in accordance with MIL-STD-973 using DDForm 1692, Engineering Change Proposal MIL-STD-481 using DD form 1693, Engineering Change Proposal (Short Form).

6.4 Record of users. Military and industrial users shall inform Defense Electronics Supply Center when a system application requires configuration control and the applicable SMD. DESC will maintain a record of users and this list will be used for coordination and distribution of changes to the drawings. Users of drawings covering microelectronics devices (FSC 5962) should contact DESC-EC, telephone (513) 296-6047.

6.5 Comments. Comments on this drawing should be directed to DESC-EC, Dayton, Ohio 45444, or telephone (513) 296-5377.

TABLE IIA. Electrical test requirements. 1/ 2/ 3/ 4/ 5/

Line no.	Test Requirements	Subgroups (in accordance with MIL-STD-883, method 5005, table I)
1	Interim electrical parameters (see 4.2)	
2	Staic burn-in (method 1015)	Required
3	Same as line 1	
4	Dynamic burn-in (method 1015)	Not Required
5	Final electrical paramters	1*,2,3,7*, 8A,8B,9,10, 11
6	Group A test requirements	1,2,3,4**,7, 8A,8B,9,10, 11
7	Group C end-point electrical parameters	2,3,7, 8A,8B
8	Group D end-point electrical parameters	2,3,8A,8B,
9	Group E end-point electrical parameters	1,7,9

1/ Blank spaces indicate tests are not applicable.
2/ Any or all subgroups may be combined when using high-speed testers.
3/ Subgroups 7 and 8 functional tests shall verify the functionality of the device.
4/ * indicates PDA applies to subgroup 1 and 7.
5/ ** see 4.3.1c.

6.7 Approved source of supply. Approved sources of supply are listed in MIL-BUL-103. The vendors listed in MIL-BUL-103 have agreed to this drawing and a certificate of compliance (see 3.6 herein) has been submitted to and accepted by DESC-ECS.