REVISIONS			
LTR	DESCRIPTION	DATE (YR-MO-DA)	APPROVED

REV																				
SHEET																				
REV																				
SHEET	15																			

REV STATUS OF SHEETS	REV														
	SHEET	1	2	3	4	5	6	7	8	9	10	11	12	13	14

PMIC N/A

STANDARDIZED MILITARY DRAWING

THIS DRAWING IS AVAILABLE FOR USE BY ALL DEPARTMENTS AND AGENCIES OF THE DEPARTMENT OF DEFENSE

AMSC N/A

PREPARED BY
Jeffrey D. Bowling

CHECKED BY
Ray Monnin

APPROVED BY

DRAWING APPROVAL DATE
92-10-30

REVISION LEVEL

DEFENSE ELECTRONICS SUPPLY CENTER
DAYTON, OHIO 45444

MICROCIRCUIT, MEMORY, DIGITAL, CMOS, 64K x 4 SRAM WITH SEPARATE I/O, MONOLITHIC SILICON

SIZE	CAGE CODE	5962-89935
A	67268	

SHEET 1 OF 15

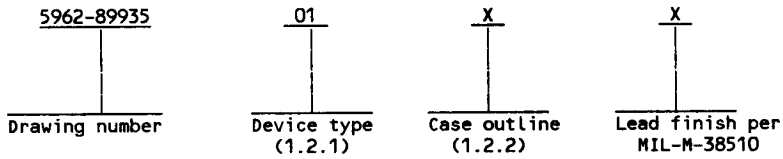
DESC FORM 193
JUL 91

5962-E479

1. SCOPE

1.1 Scope. This drawing describes device requirements for class B microcircuits in accordance with 1.2.1 of MIL-STD-883, "Provisions for the use of MIL-STD-883 in conjunction with compliant non-JAN devices".

1.2 Part or Identifying Number (PIN). The complete PIN shall be as shown in the following example:



1.2.1 Device type(s). The device type(s) shall identify the circuit function as follows:

Device type	Generic number	Circuit function	Access time
01	7C192	64K X 4 SRAM Separate I/O	45 ns
02	7C192	64K X 4 SRAM Separate I/O	35 ns
03	7C192	64K X 4 SRAM Separate I/O	25 ns

1.2.2 Case outline(s). The case outline(s) shall be as designated in MIL-STD-1835 and as follows:

Outline letter	Descriptive designator	Terminals	Package style
X	CDIP3-T28 or GDIP4-T28	28	dual in-line
Y	GDFP2-F28	28	flat pack
Z	CQCC4-N28	28	rectangular leadless chip carrier

1.3 Absolute maximum ratings.

Supply voltage to ground potential	-0.5 V dc to +7.0 V dc
DC voltage applied to outputs in High-Z state	-0.5 V dc to +7.0 V dc
DC Input voltage	-3.0 V dc to +7.0 V dc
DC output current	20 mA
Maximum power dissipation	1.0 W
Lead temperature (soldering, 10 seconds)	+260°C
Thermal resistance, junction-to-case (θ_{JC}):	
Cases X, Y, Z, and U	See MIL-STD-1835
Junction temperature (T_J) 1/	+150°C
Storage temperature range	-65°C to +150°C

1.4 Recommended operating conditions.

Supply voltage (V_{CC})	+4.5 V dc to +5.5 V dc
Ground voltage (GND)	0 V dc
Input high voltage (V_{IH})	2.2 V dc minimum
Input low voltage (V_{IL})	0.8 V dc maximum
Case operating temperature range (T_C)	-55°C to +125°C

1/ Maximum junction temperature may be increased to +175°C during burn-in and steady state life.

2. APPLICABLE DOCUMENTS

2.1 Government specification, standard, and bulletin. Unless otherwise specified, the following specification, standards, and bulletin of the issue listed in that issue of the Department of Defense Index of Specifications and Standards specified in the solicitation, form a part of this drawing to the extent specified herein.

SPECIFICATION

MILITARY

MIL-M-38510 - Microcircuits, General Specification for.

STANDARD

MILITARY

MIL-STD-883 - Test Methods and Procedures for Microelectronics.
MIL-STD-1835 - Microcircuit Case Outlines.

BULLETIN

MILITARY

MIL-BUL-103 - List of Standardized Military Drawings (SMDs).

(Copies of the specification, standard, and bulletin required by manufacturers in connection with specific acquisition functions should be obtained from the contracting activity or as directed by the contracting activity.)

2.2 Non-Government publications. The following documents form a part of this document to the extent specified herein. Unless otherwise specified, the issues of the documents which are DoD adopted are those listed in the issue of the DODISS cited in the solicitation. Unless otherwise specified, the issues of documents not listed in the DODISS are the issues of the documents cited in the solicitation.

ELECTRONICS INDUSTRIES ASSOCIATION (EIA)

JEDEC Standard No. 17 - A Standardized Test Procedure for the Characterization of LATCH-UP in CMOS Integrated Circuits.

(Applications for copies should be addressed to the Electronics Industries Association, 2001 Eye Street, N.W., Washington, DC 20006.)

(Non-Government standards and other publications are normally available from the organizations that prepare or distribute the documents. These documents also may be available in or through libraries or other informational services.)

2.3 Order of precedence. In the event of a conflict between the text of this drawing and the references cited herein, the text of this drawing shall take precedence.

3. REQUIREMENTS

3.1 Item requirements. The individual item requirements shall be in accordance with 1.2.1 of MIL-STD-883, "Provisions for the use of MIL-STD-883 in conjunction with compliant non-JAN devices" and as specified herein.

3.2 Design, construction, and physical dimensions. The design, construction, and physical dimensions shall be as specified in MIL-M-38510 and herein.

3.2.1 Case outline(s). The case outline(s) shall be in accordance with 1.2.2 herein.

3.2.2 Terminal connections. The terminal connections shall be as specified on figure 1.

3.2.3 Truth tables. The truth tables shall be as specified on figure 2.

3.2.4 Functional tests. Various functional tests used to test this device are contained in the appendix. If the test patterns cannot be implemented due to test equipment limitations, alternate test patterns to accomplish the same results shall be maintained under document revision level control by the manufacturer and shall be made available to the preparing activity or acquiring activity upon request.

TABLE I. Electrical performance characteristics.

Test	Symbol	Conditions 1/ $-55°C \le T_C \le +125°C$, $4.5\ V \le V_{CC} \le 5.5\ V$ unless otherwise specified	Group A subgroups	Device types	Limits		Unit
					Min	Max	
Output high voltage	V_{OH}	V_{CC} = 4.5 V, I_{OH} = -4.0 mA V_{IN} = V_{IH}, V_{IL}	1, 2, 3	All	2.4		V
Output low voltage	V_{OL}	V_{CC} = 4.5 V, I_{OL} = 8.0 mA V_{IN} = V_{IH}, V_{IL}	1, 2, 3	All		0.4	V
Input high voltage 2/	V_{IH}		1, 2, 3	All	2.2		V
Input low voltage 2/	V_{IL}		1, 2, 3	All		0.8	V
Input leakage current	I_{IX}	V_{IN} = 5.5 V to GND	1, 2, 3	All	-10	10	uA
Output leakage current	I_{OZ}	V_{CC} = 5.5 V, V_{OUT} = 5.5 V and GND	1, 2, 3	All	-10	10	uA
Operating supply current 3/	I_{CC1}	V_{CC} = 5.5 V, I_{OUT} = 0 mA $\overline{CE}$ = V_{IL}, f = f_{MAX}	1, 2, 3	All		130	mA
Standby power supply current TTL 3/	I_{CC2}	V_{CC} = 5.5 V, $\overline{CE} \ge V_{IH}$, all other inputs $\le V_{IL}$ or $\ge V_{IH}$, I_{OUT} = 0 mA, f = f_{MAX}	1, 2, 3	All		40	mA
Standby power supply current CMOS	I_{CC3}	$\overline{CE} \ge (V_{CC} - 0.3\ V)$, all other inputs ≤ 0.3 V or $\ge (V_{CC} - 0.3\ V)$, V_{CC} = 5.5 V, f = 0	1, 2, 3	All		20	mA
Input capacitance 4/	C_{IN}	V_{CC} = 5.0 V T_A = +25°C, f = 1 MHz (see 4.3.1c)	4	All		10	pF
Output capacitance 4/	C_{OUT}	V_{CC} = 5.0 V T_A = +25°C, f = 1 MHz (see 4.3.1c)	4	All		10	pF
Functional tests		See 4.3.1d	7, 8	All			
Read cycle time	t_{AVAV}		9, 10, 11	01	45		ns
				02	35		
				03	25		
Address access time	t_{AVQV}		9, 10, 11	01		45	ns
				02		35	
				03		25	
Output hold from address change	t_{AVQX}		9, 10, 11	All	3		ns

See footnotes at end of table.

TABLE I. Electrical performance characteristics - Continued.

Test	Symbol	Conditions 1/ $-55°C \le T_C \le +125°C$, $4.5\ V \le V_{CC} \le 5.5\ V$ unless otherwise specified	Group A subgroups	Device types	Limits		Unit
					Min	Max	
Chip enable access time	t_{ELQV}		9, 10, 11	01		45	ns
				02		35	
				03		25	
Chip enable to output active 4/ 5/	t_{ELQX}		9, 10, 11	All	3		ns
Chip select to output inactive 4/ 5/	t_{EHQZ}		9, 10, 11	01		20	ns
				02		15	
				03		13	
Chip enable to power up 4/	t_{ELPU}		9, 10, 11	All	0		ns
Chip enable to power down 4/	t_{EHPD}		9, 10, 11	01		45	ns
				02		35	
				03		25	
Write cycle time	t_{AVAV}		9, 10, 11	01	45		ns
				02	35		
				03	25		
Chip enable to write end	t_{ELWH}		9, 10, 11	01	40		ns
				02	30		
				03	20		
Address setup to end of write	t_{AVWH} t_{AVEH}		9, 10, 11	01	35		ns
				02	25		
				03	20		
Address hold from write end	t_{WHAX} t_{EHAX}		9, 10, 11	All	0		ns
Address setup to write start	t_{AVWL} t_{AVEL}		9, 10, 11	All	0		ns
Write enable pulse width	t_{WLWH} t_{WLEH}		9, 10, 11	01	30		ns
				02	25		
				03	20		

See footnotes at end of table.

TABLE I. Electrical performance characteristics - Continued.

Test	Symbol	Conditions 1/ $-55°C \le T_C \le +125°C$ $4.5\ V \le V_{CC} \le 5.5\ V$ unless otherwise specified	Group A subgroups	Device types	Limits		Unit
					Min	Max	
Data setup to write end	t_{DVWH} t_{DVEH}		9, 10, 11	01	20		ns
				02	17		
				03	15		
Data hold from write end	t_{WHDX} t_{EHDX}		9, 10, 11	All	0		ns
Write enable high to output active 4/ 5/	t_{WHQX}		9, 10, 11	All	0		ns
Write enable low to output inactive 4/ 5/	t_{WLQZ}		9, 10, 11	01		20	ns
				02		15	
				03		13	

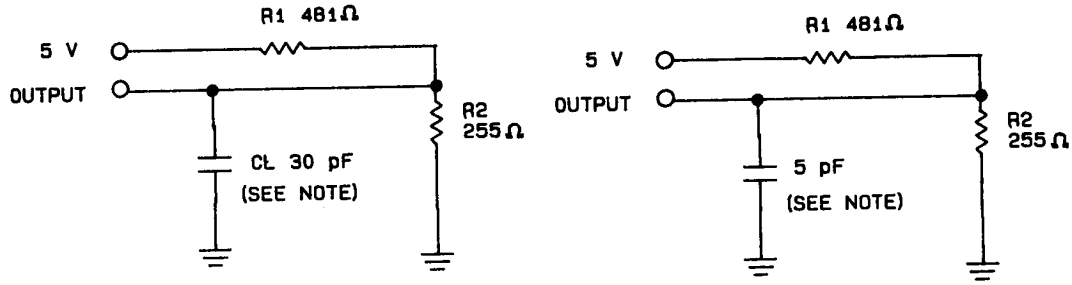
1/ AC measurements assume signal transition times of ≤ 5 ns, input levels of 0 V to 3.0 V, and output loading of 30 pF. Output timing reference level is 1.5 V. See figure 3 (circuit A).
2/ These are absolute values with respect to device ground and all overshoots and undershoots due to system or tester noise are included.
3/ At $f = f_{MAX}$, address and data inputs are cycling at the maximum frequency of $1/t_{AVAV}$.
4/ Tested initially and after any design or process changes that affect that parameter, and therefore shall be guaranteed to the limits specified in table I.
5/ Transition is measured at steady state-high level -500 mV or steady state low level +500 mV on the output from the 1.5 V level on the input, C_L = 5 pF (including scope and jig). See figure 3 (circuit B).

Device types	All
Case outlines	X, Y, and Z
Terminal number	Terminal symbol
1	A
2	A
3	A
4	A
5	A
6	A
7	A
8	A
9	A
10	A
11	I_0
12	I_1
13	$\overline{CE}$
14	GND
15	$\overline{WE}$
16	O_0
17	O_1
18	O_2
19	O_3
20	I_2
21	I_3
22	A
23	A
24	A
25	A
26	A
27	A
28	V_{CC}

FIGURE 1. Terminal connections.

$\overline{CE}$	$\overline{WE}$	Mode	D_{OUT}	Power
H	X	Not selected	High-Z	Standby
L	L	Write	High-Z	Active
L	H	Read	D_{OUT}	Active

FIGURE 2. Truth table.



Circuit A
Output load

Circuit B
Output load

NOTE: Including scope and jig. (minimum values)

AC test conditions

Input pulse levels	GND to 3.0 V
Input rise and fall times (t_r, t_f)	≤ 5 ns
Input timing reference levels	1.5 V
Output reference levels	1.5 V

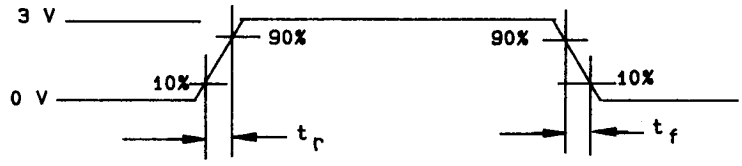
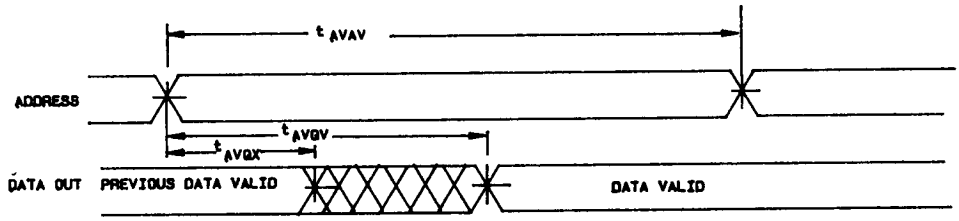
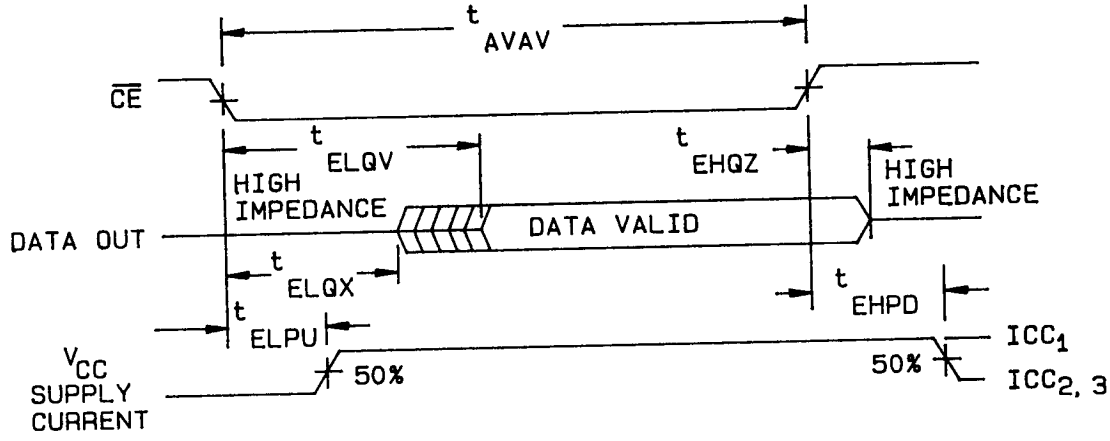


FIGURE 3. Output load circuit and test conditions.

Read cycle no. 1



Read cycle no. 2



NOTES ON READ OPERATION:
1. $\overline{WE}$ is high for read cycles.
2. For read cycle no. 1, device is continuously selected, $\overline{CE} = V_{IL}$.
3. For read cycle no. 2, addresses are valid prior to or coincident with $\overline{CE}$ transition low.
4. At any given temperature and voltage condition, t_{EHQZ} maximum is less than t_{ELQX} minimum.

FIGURE 4. Timing waveforms.

Write cycle no. 1 ($\overline{WE}$ controlled)

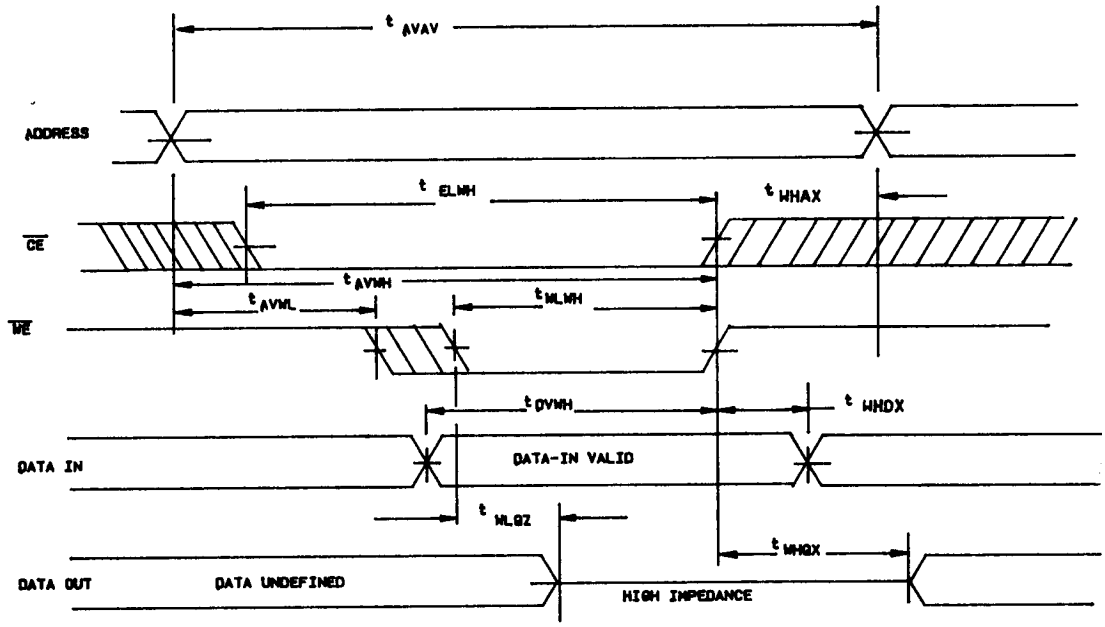
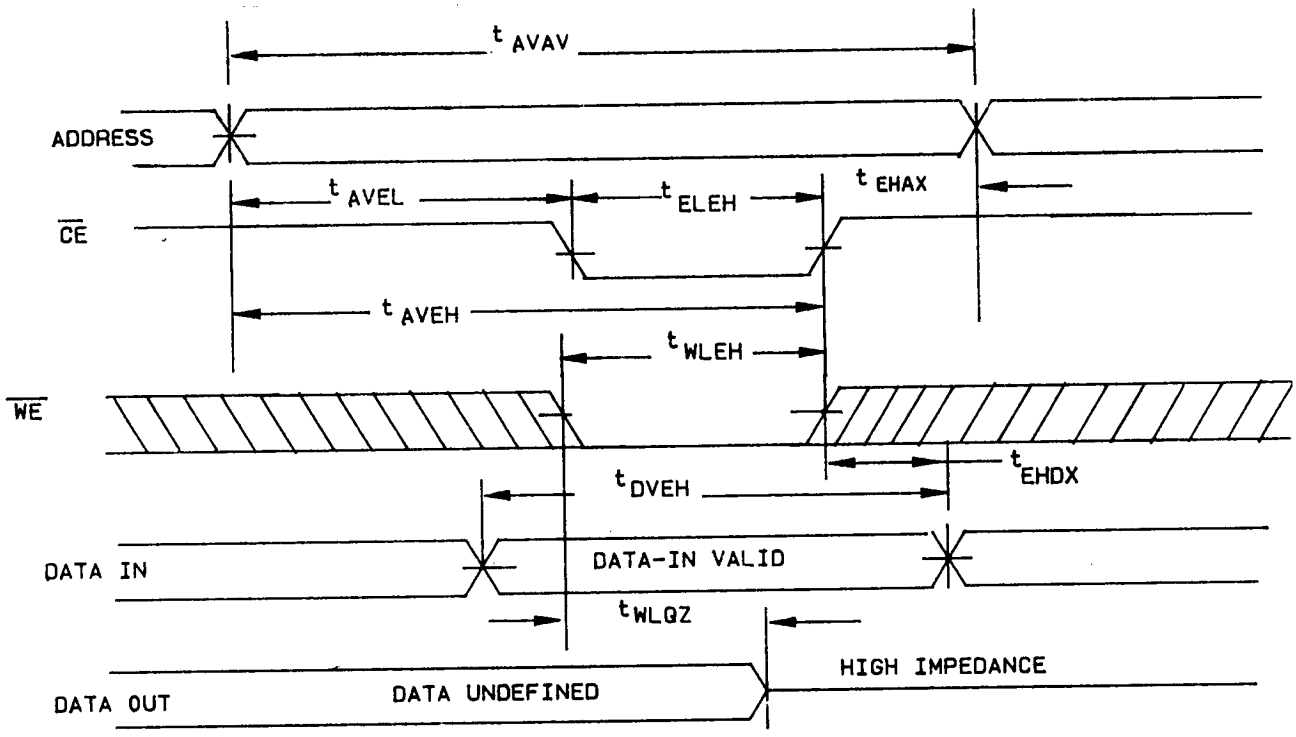


FIGURE 4. Timing waveforms - Continued.

Write cycle no. 2 ($\overline{CE}$ controlled)



NOTES ON WRITE OPERATION:

1. $\overline{CE}$ or $\overline{WE}$ must be high during address transitions.
2. If $\overline{CE}$ switches low coincident with or after $\overline{WE}$ switches low, the outputs will stay in a high impedance state.
3. If $\overline{CE}$ switches high coincident with or before $\overline{WE}$ switches high, the outputs will stay in a high impedance state.
4. A write occurs during the overlap of $\overline{CE}$ low and $\overline{WE}$ low. Both signals must be low to initiate a write and either signal can terminate a write by going high. The data input setup and hold timing should be referenced to the rising edge of the signal that terminates the write.
5. At any given temperature and voltage condition, t_{WLQZ} maximum is less than t_{WHQX} minimum.

FIGURE 4. Timing waveforms - Continued.

3.2.5 Die overcoat. Polyimide and silicone coatings are allowable as an overcoat on the die for alpha particle protection only. Each coated microcircuit inspection lot (see inspection lot as defined in MIL-M-38510) shall be subjected to and pass the internal moisture content test, (see method 1018 of MIL-STD-883). The frequency of the internal water vapor testing may not be decreased unless approved by the preparing activity.

3.3 Electrical performance characteristics. Unless otherwise specified herein, the electrical performance characteristics are as specified in table I and shall apply over the full case operating temperature range.

3.4 Electrical test requirements. The electrical test requirements shall be the subgroups specified in table II. The electrical tests for each subgroup are described in table I.

3.5 Marking. Marking shall be in accordance with MIL-STD-883 (see 3.1 herein). The part shall be marked with the PIN listed in 1.2 herein. In addition, the manufacturer's PIN may also be marked as listed in MIL-BUL-103 (see 6.6 herein).

3.6 Certificate of compliance. A certificate of compliance shall be required from a manufacturer in order to be listed as an approved source of supply in MIL-BUL-103 (see 6.6 herein). The certificate of compliance submitted to DESC-ECS prior to listing as an approved source of supply shall affirm that the manufacturer's product meets the requirements of MIL-STD-883 (see 3.1 herein) and the requirements herein.

3.7 Certificate of conformance. A certificate of conformance as required in MIL-STD-883 (see 3.1 herein) shall be provided with each lot of microcircuits delivered to this drawing.

3.8 Notification of change. Notification of change to DESC-ECS shall be required in accordance with MIL-STD-883 (see 3.1 herein).

3.9 Verification and review. DESC, DESC's agent, and the acquiring activity retain the option to review the manufacturer's facility and applicable required documentation. Offshore documentation shall be made available onshore at the option of the reviewer.

4. QUALITY ASSURANCE PROVISIONS

4.1 Sampling and inspection. Sampling and inspection procedures shall be in accordance with section 4 of MIL-M-38510 to the extent specified in MIL-STD-883 (see 3.1 herein).

4.2 Screening. Screening shall be in accordance with method 5004 of MIL-STD-883, and shall be conducted on all devices prior to quality conformance inspection. The following additional criteria shall apply:

a. Burn-in test, method 1015 of MIL-STD-883.

(1) Test condition D using the circuit submitted with the certificate of compliance (see 3.6 herein).

(2) T_A = +125°C, minimum.

b. Interim and final electrical test parameters shall be as specified in table II herein, except interim electrical parameter tests prior to burn-in are optional at the discretion of the manufacturer.

4.3 Quality conformance inspection. Quality conformance inspection shall be in accordance with method 5005 of MIL-STD-883 including groups A, B, C, and D inspections. The following additional criteria shall apply.

4.3.1 Group A inspection.

a. Tests shall be as specified in table II herein.

b. Subgroups 5 and 6 in table I, method 5005 of MIL-STD-883 shall be omitted.

c. Subgroup 4 (C_{IN} and C_{OUT} measurements) shall be measured only for the initial test and after any process or design changes which may affect input or output capacitance. Sample size is 15 devices with no failures, and all input and output terminals tested.

d. Subgroups 7 and 8 tests shall be sufficient to verify the truth tables.

e. O/V (latch-up) tests shall be measured only for initial qualification and after any design or process changes which may affect the performance of the device. Procedures and circuits shall be maintained under document revision level control by the manufacturer and shall be made available to the preparing activity or acquiring activity upon request. Testing shall be on all pins, on 5 devices with zero failures. Latch-up test shall be considered destructive. JEDEC Standard No. 17 may be used as a guideline when performing O/V testing.

TABLE II. Electrical test requirements.

MIL-STD-883 test requirements	Subgroups (per method 5005, table I)
Interim electrical parameters (method 5004)	---
Final electrical test parameters (method 5004)	1*,2,3,7*,8A,8B, 9,10,11
Group A test requirements (method 5005)	1,2,3,4**,7***, 8A***,8B***,9, 10,11
Groups C and D end-point electrical parameters (method 5005)	2,3,7,8A,8B

* PDA applies to subgroup 1 and 7
** For subgroup 4 see 4.3.1c
*** For subgroups 7 and 8, see 4.3.1d

4.3.2 Groups C and D inspections.

a. End-point electrical parameters shall be as specified in table II herein.

b. Steady-state life test conditions; method 1005 of MIL-STD-883:

(1) Test condition D using the circuit submitted with the certificate of compliance (see 3.6 herein).

(2) T_A = +125°C, minimum.

(3) Test duration: 1,000 hours, except as permitted by method 1005 of MIL-STD-883.

5. PACKAGING

5.1 Packaging requirements. The requirements for packaging shall be in accordance with MIL-M-38510.

6. NOTES

6.1 Intended use. Microcircuits conforming to this drawing are intended for use when military specifications do not exist and qualified military devices that will perform the required function are not available for OEM application. When a military specification exists and the product covered by this drawing has been qualified for listing on QPL-38510, the device specified herein will be inactivated and will not be used for new design. The QPL-38510 product shall be the preferred item for all applications.

6.2 Replaceability. Microcircuits covered by this drawing will replace the same generic device covered by a contractor-prepared specification or drawing.

6.3 Configuration control of SMDs. All proposed changes to existing SMDs will be coordinated with the users of record for the individual documents. This coordination will be accomplished in accordance with MIL-STD-481 using DD Form 1693, Engineering Change Proposal (Short Form).

6.4 Record of users. Military and industrial users shall inform Defense Electronics Supply Center when a system application requires configuration control and the applicable SMD. DESC will maintain a record of users and this list will be used for coordination and distribution of changes to the drawings. Users of drawings covering microelectronics devices (FSC 5962) should contact DESC-ECS, telephone (513) 296-6047.

6.5 Comments. Comments on this drawing should be directed to DESC-ECS, Dayton, Ohio 45444, or telephone (513) 296-5377.

6.6 Approved sources of supply. Approved sources of supply are listed in MIL-BUL-103. Additional sources will be added to MIL-BUL-103 as they become available. The vendors listed in MIL-BUL-103 have agreed to this drawing and a certificate of compliance (see 3.6 herein) has been submitted to and accepted by DESC-ECS.

APPENDIX

FUNCTIONAL ALGORITHMS

10. SCOPE

10.1 Scope. Functional algorithms are test patterns which define the exact sequence of events used to verify proper operation of a random access memory (RAM). Each algorithm serves a specific purpose for the testing of the device. It is understood that all manufacturers do not have the same test equipment; therefore, it becomes the responsibility of each manufacturer to guarantee that the test patterns described herein are followed as closely as possible, or equivalent patterns be used that serve the same purpose. Each manufacturer should demonstrate that this condition will be met. Algorithms shall be applied to the device in a topologically pure fashion. This appendix is a mandatory part of the specification. The information contained herein is intended for compliance.

20. APPLICABLE DOCUMENTS. This section is not applicable to this appendix.

30. ALGORITHMS

30.1 Algorithm A (pattern 1).

30.1.1 Checkerboard, checkerboard-bar.

Step 1. Load memory with a checkerboard data pattern by incrementing from location 0 to maximum.
Step 2. Read memory, verifying the output checkerboard pattern by incrementing from location 0 to maximum.
Step 3. Load memory with a checkerboard-bar pattern by incrementing from location 0 to maximum.
Step 4. Read memory, verifying the output checkerboard-bar pattern by incrementing from location 0 to maximum.

30.2 Algorithm B (pattern 2).

30.2.1 March.

Step 1. Load memory with background data, incrementing from minimum to maximum address locations (All "0's").
Step 2. Read data in location 0.
Step 3. Write complement data to location 0.
Step 4. Read complement data in location 0.
Step 5. Repeat steps 2 through 4 incrementing X-fast sequentially, for each location in the array.
Step 6. Read complement data in maximum address location.
Step 7. Write data to maximum address location.
Step 8. Read data in maximum address location.
Step 9. Repeat steps 6 through 8 decrementing X-fast sequentially for, each location in the array.
Step 10. Read data in location 0.
Step 11. Write complement data to location 0.
Step 12. Read complement data in location 0.
Step 13. Repeat steps 10 through 12 decrementing X-fast sequentially for each location in the array.
Step 14. Read complement data in maximum address location.
Step 15. Write data to maximum address location.
Step 16. Read data in maximum address location.
Step 17. Repeat steps 14 through 16 incrementing X-fast sequentially for each location in the array.
Step 18. Read background data from memory, decrementing X-fast from maximum to minimum address locations.

30.3 Algorithm C (pattern 3).

30.2.1 XY March.

Step 1. Load memory with background data, incrementing from minimum to maximum address locations (All "0's").
Step 2. Read data in location 0.
Step 3. Write complement data to location 0.
Step 4. Read complement data in location 0.
Step 5. Repeat steps 2 through 4 incrementing Y-fast sequentially, for each location in the array.
Step 6. Read complement data in maximum address location.
Step 7. Write data to maximum address location.
Step 8. Read data in maximum address location.
Step 9. Repeat steps 6 through 8 decrementing X-fast sequentially for each location in the array.
Step 10. Read data in location 0.
Step 11. Write complement data to location 0.
Step 12. Read complement data in location 0.
Step 13. Repeat steps 10 through 12 decrementing Y-fast sequentially for each location in the array.
Step 14. Read complement data in maximum address location.
Step 15. Write data to maximum address location.
Step 16. Read data in maximum address location.
Step 17. Repeat steps 14 through 16 incrementing X-fast sequentially for each location in the array.
Step 18. Read background data from memory, decrementing Y-fast from maximum to minimum address locations.

30.4 Algorithm D (pattern 4).

30.4.1 CEDES - CE deselect checkerboard, checkerboard-bar.

Step 1. Load memory with a checkerboard data pattern by incrementing from location 0 to maximum.
Step 2. Deselect device, attempt to load memory with checkerboard-bar data pattern by incrementing from location 0 to maximum.
Step 3. Read memory, verifying the output checkerboard pattern by incrementing from location 0 to maximum.
Step 4. Load memory with a checkerboard-bar pattern by incrementing from location 0 to maximum.
Step 5. Deselect device, attempt to load memory with checkerboard data pattern by incrementing from location 0 to maximum.
Step 6. Read memory, verifying the output checkerboard-bar pattern by incrementing from location 0 to maximum.