REVISIONS			
LTR	DESCRIPTION	DATE (YR-MO-DA)	APPROVED
A	Redrawn with changes. Converted drawing to one part-one part number SMD format. Added package, outline letters Z and U. Added devices 03 and 04.	93-09-14	M. A. Frye
B	Added case outline T. Made format changes, editorial changes throughout.	93-11-19	M. A. Frye
C	Added case outlines M, N, and 9. Editorial changes throughout.	94-06-06	M. A. Frye

REV	C	C																		
SHEET	35	36																		
REV	B	B	C	C	C	C	C	C	C	C	C	C	C	C	C	C	C	C	C	C
SHEET	15	16	17	18	19	20	21	22	23	24	25	26	27	28	29	30	31	32	33	34

REV STATUS OF SHEETS	REV	C	C	C	B	B	B	B	B	B	B	B	B	B	B
	SHEET	1	2	3	4	5	6	7	8	9	10	11	12	13	14

PMIC N/A

STANDARDIZED MILITARY DRAWING

THIS DRAWING IS AVAILABLE FOR USE BY ALL DEPARTMENTS AND AGENCIES OF THE DEPARTMENT OF DEFENSE

AMSC N/A

PREPARED BY
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DRAWING APPROVAL DATE
92-07-29

REVISION LEVEL C

DEFENSE ELECTRONICS SUPPLY CENTER
DAYTON, OHIO 45444

MICROCIRCUIT, MEMORY, DIGITAL, CMOS 2000 GATE PROGRAMMABLE LOGIC ARRAY, MONOLITHIC SILICON

SIZE	CAGE CODE	5962-89948
A	67268	

SHEET OF 36

DESC FORM 193
JUL 91

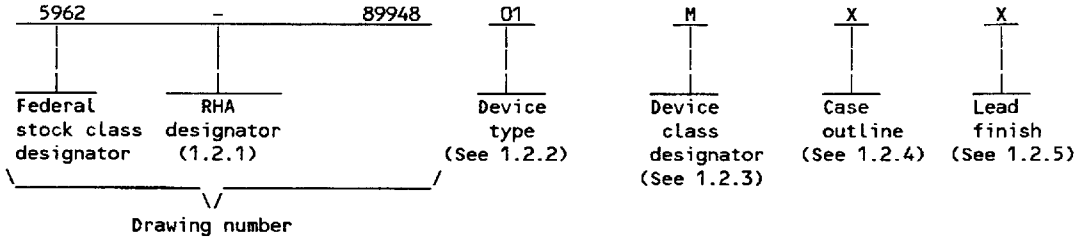
5962-E183-94

DISTRIBUTION STATEMENT A. Approved for public release; distribution is unlimited.

1. SCOPE

1.1 Scope. This drawing forms a part of a one part - one part number documentation system (see 6.6 herein). Two product assurance classes consisting of military high reliability (device classes Q and M) and space application (device class V), and a choice of case outlines and lead finishes are available and are reflected in the Part or Identifying Number (PIN). Device class M microcircuits represent non-JAN class B microcircuits in accordance with 1.2.1 of MIL-STD-883, "Provisions for the use of MIL-STD-883 in conjunction with compliant non-JAN devices". When available, a choice of Radiation Hardness Assurance (RHA) levels are reflected in the PIN.

1.2 PIN. The PIN shall be as shown in the following example:



1.2.1 RHA designator. Device class M RHA marked devices shall meet the MIL-I-38535 appendix A specified RHA levels and shall be marked with the appropriate RHA designator. Device classes Q and V RHA marked devices shall meet the MIL-I-38535 specified RHA levels and shall be marked with the appropriate RHA designator. A dash (-) indicates a non-RHA device.

1.2.2 Device type(s). The device type(s) shall identify the circuit function as follows:

Device type	Generic number	Circuit function	Toggle Speed
01	3020-50	8x8 2000 gate programmable array	50 MHz
02	3020-70	8x8 2000 gate programmable array	70 MHz
03	3020-100	8x8 2000 gate programmable array	100 MHz
04	3020-125	8x8 2000 gate programmable array	125 MHz

1.2.3 Device class designator. The device class designator shall be a single letter identifying the product assurance level as follows:

Device class	Device requirements documentation
M	Vendor self-certification to the requirements for non-JAN class B microcircuits in accordance with 1.2.1 of MIL-STD-883
Q or V	Certification and qualification to MIL-I-38535

1.2.4 Case outline(s). The case outlines shall be as designated in MIL-STD-1835 and as follows:

Outline letter	Descriptive designator	Terminals	Package style
X	CMGA15-PN	84 1/	Pin grid array package
Y	See figure 1	100	Quad flat package
Z	CMGA3-PN	84 1/	Pin grid array package
U	CQCC1-F100	100	Unformed-lead chip carrier 2/
T	See figure 1	100	Quad flat package
M	See figure 1	100	Quad flat package
N	See figure 1	100	Quad flat package
9	See figure 1	100	Quad flat package

1.2.5 Lead finish. The lead finish shall be as specified in MIL-STD-883 (see 3.1 herein) for class M or MIL-I-38535 for classes Q and V. Finish letter "X" shall not be marked on the microcircuit or its packaging. The "X" designation is for use in specifications when lead finishes A, B, and C are considered acceptable and interchangeable without preference.

1/ 84 = actual number of pins used, not maximum listed in MIL-STD-1835
2/ Pin 1 is the middle pin on the side with center justified identifier mark. Mark may be a notch, dot, or triangle.

1.3 Absolute maximum ratings. 3/

Supply voltage range to ground potential (V_{CC})	-0.5 V dc to +7.0 V dc
DC input voltage range	-0.5 V dc to V_{CC} +0.5 V dc
Voltage applied to three-state output(V_{TS})	-0.5 V dc to V_{CC} +0.5 V dc
Lead temperature (soldering, 10 seconds)	+260°C
Thermal resistance, junction-to-case (Θ_{JC}):	
Case outline X, Z, and U	See MIL-STD-1835
Case outlines Y, T, M, N, and 9	10°C/W 4/
Junction temperature (T_J)	+150°C 5/
Storage temperature range	-65°C to +150°C

1.4 Recommended operating conditions. 6/

Case operating temperature Range(T_C)	-55°C to +125°C
Supply voltage relative to ground(V_{CC})	+4.5 V dc minimum to +5.5 V dc maximum
Ground voltage (GND) or (V_{SS})	0 V dc

1.5 Digital logic testing for device classes Q and V.

Fault coverage measurement of manufacturing logic tests in accordance with MIL-I-38535	95 percent

2. APPLICABLE DOCUMENTS

2.1 Government specification, standards, bulletin, and handbook. Unless otherwise specified, the following specification, standards, bulletin, and handbook of the issue listed in that issue of the Department of Defense Index of Specifications and Standards specified in the solicitation, form a part of this drawing to the extent specified herein.

SPECIFICATION

MILITARY

MIL-I-38535 - Integrated Circuits, Manufacturing, General Specification for.

STANDARDS

MILITARY

MIL-STD-883 - Test Methods and Procedures for Microelectronics.
MIL-STD-973 - Configuration Management.
MIL-STD-1835 - Microcircuit Case Outlines.

BULLETIN

MILITARY

MIL-BUL-103 - List of Standardized Military Drawings (SMD's).

HANDBOOK

MILITARY

MIL-HDBK-780 - Standardized Military Drawings.

(Copies of the specification, standards, bulletin, and handbook required by manufacturers in connection with specific acquisition functions should be obtained from the contracting activity or as directed by the contracting activity.)

3/ Stresses above the absolute maximum rating may cause permanent damage to the device. Extended operation at the maximum levels may degrade performance and affect reliability.
4/ When a thermal resistance for this case is specified in MIL-STD-1835 that value shall supersede the value indicated herein.
5/ Maximum junction temperature shall not be exceeded except for allowable short duration burn-in screening conditions in accordance with method 5004 of MIL-STD-883.
6/ All voltage values in this drawing are with respect to V_{SS}.

2.2 Non-Government publications. The following documents form a part of this document to the extent specified herein. Unless otherwise specified, the issues of the documents which are DoD adopted are those listed in the issue of the DODISS cited in the solicitation. Unless otherwise specified, the issues of documents not listed in the DODISS are the issues of the documents cited in the solicitation.

AMERICAN SOCIETY FOR TESTING AND MATERIALS (ASTM)

ASTM Standard F1192-88 - Standard Guide for the Measurement of Single Event Phenomena from Heavy Ion Irradiation of Semiconductor Devices.

(Applications for copies of ASTM publications should be addressed to the American Society for Testing and Materials, 1916 Race Street, Philadelphia, PA 19103.)

ELECTRONICS INDUSTRIES ASSOCIATION (EIA)

JEDEC Standard No. 17 - A Standardized Test Procedure for the Characterization of Latch-up in CMOS Integrated Circuits.

(Applications for copies should be addressed to the Electronics Industries Association, 2001 Pennsylvania Street, N.W., Washington, DC 20006.)

(Non-Government standards and other publications are normally available from the organizations that prepare or distribute the documents. These documents also may be available in or through libraries or other informational services.)

2.3 Order of precedence. In the event of a conflict between the text of this drawing and the references cited herein, the text of this drawing shall take precedence.

3. REQUIREMENTS

3.1 Item requirements. The individual item requirements for device class M shall be in accordance with 1.2.1 of MIL-STD-883, "Provisions for the use of MIL-STD-883 in conjunction with compliant non-JAN devices" and as specified herein. The individual item requirements for device classes Q and V shall be in accordance with MIL-I-38535, the device manufacturer's Quality Management (QM) plan, and as specified herein.

3.2 Design, construction, and physical dimensions. The design, construction, and physical dimensions shall be as specified in MIL-STD-883 (see 3.1 herein) for device class M and MIL-I-38535 for device classes Q and V and herein.

3.2.1 Case outline(s). The case outline(s) shall be in accordance with figure 1 and 1.2.4 herein.

3.2.2 Terminal connections. The terminal connections shall be as specified on figure 2.

3.2.3 Logic block diagram. The logic block diagram shall be as specified in figure 3.

3.2.4 Radiation exposure circuit. The radiation exposure circuit will be provided when RHA product becomes available.

3.3 Electrical performance characteristics and postirradiation parameter limits. Unless otherwise specified herein, the electrical performance characteristics and postirradiation parameter limits are as specified in table I and shall apply over the full case operating temperature range.

3.4 Electrical test requirements. The electrical test requirements shall be the subgroups specified in table IIA. The electrical tests for each subgroup are defined in table I.

3.5 Marking. The part shall be marked with the PIN listed in 1.2 herein. Marking for device class M shall be in accordance with MIL-STD-883 (see 3.1 herein). In addition, the manufacturer's PIN may also be marked as listed in MIL-BUL-103. Marking for device classes Q and V shall be in accordance with MIL-I-38535.

3.5.1 Certification/compliance mark. The compliance mark for device class M shall be a "C" as required in MIL-STD-883 (see 3.1 herein). The certification mark for device classes Q and V shall be a "QML" or "Q" as required in MIL-I-38535.

3.6 Certificate of compliance. For device class M, a certificate of compliance shall be required from a manufacturer in order to be listed as an approved source of supply in MIL-BUL-103 (see 6.8.2 herein). For device classes Q and V, a certificate of compliance shall be required from a QML-38535 listed manufacturer in order to supply to the requirements of this drawing (see 6.8.1 herein). The certificate of compliance submitted to DESC-EC prior to listing as an approved source of supply for this drawing shall affirm that the manufacturer's product meets, for device class M, the requirements of MIL-STD-883 (see 3.1 herein), or for device classes Q and V, the requirements of MIL-I-38535 and the requirements herein.

3.7 Certificate of conformance. A certificate of conformance as required for device class M in MIL-STD-883 (see 3.1 herein) or for device classes Q and V in MIL-I-38535 shall be provided with each lot of microcircuits delivered to this drawing.

3.8 Notification of change for device class M. For device class M, notification to DESC-EC of change of product (see 6.2 herein) involving devices acquired to this drawing is required for any change as defined in MIL-STD-973.

3.9 Verification and review for device class M. For device class M, DESC, DESC's agent, and the acquiring activity retain the option to review the manufacturer's facility and applicable required documentation. Offshore documentation shall be made available onshore at the option of the reviewer.

3.10 Microcircuit group assignment for device class M. Device class M devices covered by this drawing shall be in microcircuit group number 42 (see MIL-I-38535, appendix A).

3.11 Operational notes. Additional information shall be provided by the device manufacturer (see 6.7 herein).

4. QUALITY ASSURANCE PROVISIONS

4.1 Sampling and inspection. For device class M, sampling and inspection procedures shall be in accordance with MIL-STD-883 (see 3.1 herein). For device classes Q and V, sampling and inspection procedures shall be in accordance with MIL-I-38535 and the device manufacturer's QM plan.

4.2 Screening. For device class M, screening shall be in accordance with method 5004 of MIL-STD-883, and shall be conducted on all devices prior to quality conformance inspection. For device classes Q and V, screening shall be in accordance with MIL-I-38535, and shall be conducted on all devices prior to qualification and technology conformance inspection.

4.2.1 Additional criteria for device classes M.

a. Delete the sequence specified as initial (pre-burn-in) electrical parameters through interim (post-burn-in) electrical parameters of method 5004 and substitute lines 1 through 6 of table IIA herein.

b. For device class M, the test circuit shall be maintained by the manufacturer under document revision level control and shall be made available to the preparing or acquiring activity upon request. For device class M the test circuit shall specify the inputs, outputs, biases, and power dissipation, as applicable, in accordance with the intent specified in test method 1015.

c. Interim and final electrical test parameters shall be as specified in table IIA herein.

TABLE I. Electrical performance characteristics.

Test	Symbol	Conditions $4.5\ V \le V_{CC} \le 5.5\ V$ $-55°C \le T_C \le +125°C$ unless otherwise specified	Group A subgroups	Device type	Limits		Unit
					Min	Max	
High level output voltage	V_{OH}	V_{CC} = 4.5 V, V_{IL} = 0.8 V, I_{OH} = -4.0 mA, V_{IH} = 2.0 V	1,2,3	All	3.7		V
		V_{CC} = 4.5 V and 5.5 V, V_{IL} = 0.9 V and 1.1 V, V_{IH} = 3.15 V and 3.85 V, I_{OH} = -4.0 mA					
Low level output voltage	V_{OL}	V_{CC} = 5.5 V, I_{OL} = 4.0 mA V_{IL} = 0.8 V, V_{IH} = 2.0 V	1,2,3	All		0.4	V
		V_{CC} = 4.5 V and 5.5 V, V_{IL} = 0.9 V and 1.1 V, V_{IH} = 3.15 V and 3.85 V, I_{OL} = 4.0 mA					
Operating power supply current	I_{CC}	V_{CC} = 5.5 V 1/	1,2,3	01		245	mA
				02		250	
				03		260	
				04		270	
Quiescent power supply current	I_{CCO}	CMOS inputs, $V_{CC} = V_{IN}$ = 5.5 V	1,2,3	All		1.0	mA
Quiescent power supply current	I_{CCO}	TTL inputs, $V_{CC} = V_{IN}$ = 5.5 V	1,2,3	All		15	mA
Power-down supply current	I_{CCPD}	$\overline{PWRDWN}$ = 0 V, $V_{CC} = V_{IN}$ = 5.5 V	1,2,3	All		0.5	mA
Input leakage current	I_{IL}	V_{CC} = 5.5 V, V_{IN} = 0 V and 5.5 V	1,2,3	All	-20	20	µA
Output leakage current	I_{OL}	V_{CC} = 5.5 V, V_{IN} = 0 V and 5.5 V	1,2,3	All	-20	20	µA
Horizontal long line, pull-up current	I_{RLL}	V_{CC} = 5.5 V, V_{IN} = 0 V and 5.5 V	1,2,3	All		2.5	mA

See footnotes at end of table.

TABLE I. Electrical performance characteristics - Continued.

Test	Symbol	Conditions $4.5\ V \le V_{CC} \le 5.5\ V$, $-55°C \le T_C \le +125°C$ unless otherwise specified	Group A subgroups	Device type	Limits		Unit
					Min	Max	
High level input voltage	V_{IHT}	TTL inputs	1,2,3	All	2.0		V
Low level input voltage	V_{ILT}	TTL inputs	1,2,3	All		0.8	V
High level input voltage	V_{IHC}	CMOS inputs	1,2,3	All	0.7 V_{CC}		V
Low level input voltage	V_{ILC}	CMOS inputs	1,2,3	All		0.2 V_{CC}	V
Power down ($\overline{PWRDWN}$) voltage 2/	V_{PD}		1,2,3	All	3.5		V
Input capacitance except XTL1 and XTL2	C_{IN}	See 4.4.1e	4	All		10	pF
Input capacitance XTL1 and XTL2	C_{IN}	See 4.4.1e	4	All		15	pF
Output capacitance	C_{OUT}	See 4.4.1e	4	All		10	pF
Functional test		See 4.4.1c	7,8A,8B	All			
Interconnect + t_{PID} + $8(t_{ILO})$ + t_{OP}	t_{B1}	Measured on 8 columns	9,10,11	01		136	ns
				02		87	
				03		66	
				04		52	
t_{CKO} + t_{ICK} + t_{CKI} + interconnect	t_{B2}	Tested on all CLB's	9,10,11	01		32	ns
				02		21	
				03		18	
				04		15	

See footnotes at end of table.

TABLE I. Electrical performance characteristics - Continued.

Test	Symbol	Conditions $4.5\ V \le V_{CC} \le 5.5\ V$, $-55°C \le T_C \le +125°C$ unless otherwise specified	Group A subgroups	Device type	Limits		Unit
					Min	Max	
Interconnect + $t_{CKO} + t_{QLO} + t_{ILO} + t_{DICK}$	t_{B3}	Tested on all CLB's	9,10,11	01		53	ns
				02		34	
				03		26	
				04		22	
$t_{ILO} + t_{ECCK}$ + interconnect	t_{B4}	Tested on all CLB's	9,10,11	01		35	ns
				02		23	
				03		18	
				04		15	
$t_{OKPO} + t_{OPS} - t_{OPF} + t_{PICK}$	t_{B5}	Tested on all CLB's	9,10,11	01		73	ns
				02		53	
				03		44	
				04		40	
Interconnect + $t_{CKO} + t_{QLO} + t_{PUS} + t_{ICK}$	t_{B6}	One long line pull-up	9,10,11	01		73	ns
				02		48	
				03		34	
				04		30	
Interconnect + $t_{CKO} + t_{QLO} + t_{PUS} + t_{ICK}$	t_{B7}	Other long line pull-up	9,10,11	01		83	ns
				02		55	
				03		41	
				04		35	
Interconnect + $t_{CKO} + t_{QLO} + t_{IO} + t_{ICK}$	t_{B8}	No pull-up, lower long lines	9,10,11	01		47	ns
				02		31	
				03		24	
				04		21	
Interconnect + $t_{CKO} + t_{QLO} + t_{ICK} + t_{IO}$	t_{B9}	No pull-up, upper long lines	9,10,11	01		57	ns
				02		38	
				03		31	
				04		26	

See footnotes at end of table.

TABLE I. Electrical performance characteristics - Continued.

Test	Symbol	Conditions $4.5\ V \le V_{CC} \le 5.5\ V$, $-55°C \le T_C \le +125°C$ unless otherwise specified	Group A subgroups	Device type	Limits Min	Limits Max	Unit
Logic input to output (combinatorial)	t_{ILO}	See figure 4	3/	01		14	ns
				02		9.0	
				03		7	
				04		5.5	
Reset input to output	t_{RIO}		3/	01		15	ns
				02		8.0	
				03		7	
				04		6	
Reset direct width	t_{RPW}		3/	01	12		ns
				02	8.0		
				03	7		
				04	6		
Master reset pin to CLB output (X and Y)	t_{MRQ}		3/	01		40	ns
				02		34	
				03		19	
				04		17	
K clock input to CLB output	t_{CKO}		3/	01		12	ns
				02		8.0	
				03		6	
				04		5	
Clock K to outputs X or Y when Q is returned thru function generators F or G to drive X or y	t_{QLO}		3/	01		25	ns
				02		13	
				03		10	
				04		8	

See footnotes at end of table.

TABLE I. Electrical performance characteristics - Continued.

Test	Symbol	Conditions $4.5\ V \le V_{CC} \le 5.5\ V$, $-55°C \le T_C \le +125°C$ unless otherwise specified	Group A subgroups	Device type	Limits Min	Limits Max	Unit
K clock logic-input setup	t_{ICK}	See figure 4	3/	01	12		ns
				02	8.0		
				03	7		
				04	5.5		
K clock logic-input hold	t_{CKI}		3/	All	1.0		ns
Logic input setup to K clock	t_{DICK}		3/	01	8.0		ns
				02	5.0		
				03	4		
				04	3		
Logic input hold from K clock	t_{CKDI}		3/	01	6.0		ns
				02	4.0		
				03	2		
				04	1.5		
Logic input setup to enable clock	t_{ECCK}		3/	01	10		ns
				02	7.0		
				03	5		
				04	4.5		
Logic input hold to enable clock	t_{CKEC}		3/	All	2.5		ns
Clock (high) 4/	t_{CH}		3/	01	9.0		ns
				02	5.0		
				03	4		
				04	3		

See footnotes at end of table.

TABLE I. Electrical performance characteristics - Continued.

Test	Symbol	Conditions $4.5\ V \le V_{CC} \le 5.5\ V$, $-55°C \le T_C \le +125°C$ unless otherwise specified	Group A subgroups	Device type	Limits Min	Limits Max	Unit
Clock (low) 4/	t_{CL}	See figure 4	3/	01	9.0		ns
				02	7.0		
				03	4		
				04	3		
Pad (package pin) to input direct	t_{PID}		3/	01		10.0	ns
				02		6.0	
				03		4	
				04		3	
Fast (cmos only) input pad through clock buffer to any CLB or IOB clock input.	t_{PGCC}		3/	01		8.5	ns
				02		6.5	
				03,04		6.0	
I/O clock to I/O RI input (FF)	t_{IKRI}		3/	01		11	ns
				02		5.5	
				03		4	
				04		3	
I/O clock to pad-input setup	t_{PICK}		3/	01	30		ns
				02	20		
				03	17		
				04	16		
I/O clock to pad-input hold	t_{IKPI}		3/	All	1.0		ns
I/O clock to pad (fast)	t_{OKPO}		3/	01		18	ns
				02		13	
				03		10	
				04		9	

See footnotes at end of table.

TABLE I. Electrical performance characteristics - Continued.

Test	Symbol	Conditions $4.5\ V \le V_{CC} \le 5.5\ V$, $-55°C \le T_C \le +125°C$ unless otherwise specified	Group A subgroups	Device type	Limits		Unit
					Min	Max	
I/O clock to pad-output setup	t_{OOK}	See figure 4	3/	01	15		ns
				02	10		
				03	9		
				04	8		
I/O clock to pad-output hold	t_{OKO}		3/	All	1		ns
I/O clock (high) 5/	t_{IOH}		3/	01	9.0		ns
				02	5.0		
				03	4		
				04	3		
I/O clock (low) 5/	t_{IOL}		3/	01	9.0		ns
				02	5.0		
				03	4		
				04	3		
Output (enabled fast) to pad	t_{OPF}		3/	01		15	ns
				02		9.0	
				03		6	
				04		5	
Output (enabled slow) to pad	t_{OPS}		3/	01		40	ns
				02		33	
				03		24	
				04		20	
Three-state to pad begin high impedance (fast)	t_{TSHZ}		3/	01		14	ns
				02		12	
				03		10	
				04		9	

See footnotes at end of table.

TABLE I. Electrical performance characteristics - Continued.

Test	Symbol	Conditions $4.5\ V \le V_{CC} \le 5.5\ V$, $-55°C \le T_C \le +125°C$ unless otherwise specified	Group A subgroups	Device type	Limits Min	Limits Max	Unit
Three-state to pad end high impedance (fast)	t_{TSON}	See figure 4	3/	01		20	ns
				02		14	
				03		12	
				04		11	
Master $\overline{RESET}$ to input RI	t_{RRI}		3/	01		35	ns
				02		23	
				03,04		20	
Master $\overline{RESET}$ to output (FF)	t_{RPO}		3/	01		50	ns
				02		33	
				03		28	
				04		26	
Bidirectional buffer delay	t_{BIDI}		3/	01		4.0	ns
				02		2.0	
				03		1.8	
				04		1.7	
TBUF data input to output	t_{IO}		3/	01		8.0	ns
				02		5.0	
				03		4.7	
				04		4.5	
TBUF three-state to output active and valid (single pull-up)	t_{ON}		3/	All		14	ns
double pull-up						15	
TBUF three-state to output inactive (single pull-up)	t_{PUS}		3/	01		34	ns
				02,03		22	
				04		17	

See footnotes at end of table.

TABLE I. Electrical performance characteristics - Continued.

Test	Symbol	Conditions $4.5\ V \le V_{CC} \le 5.5\ V$ $-55°C \le T_C \le +125°C$ unless otherwise specified	Group A subgroups	Device type	Limits		Unit
					Min	Max	
TBUF three-state to output inactive (pair of pull-ups)	t_{PUF}	See figure 4	3/	01		17	ns
				02,03,04		11	

1/ Tested initially and after any design or process change that may affect this parameter and guaranteed to the limits specified in table I with the following conditions:
Global clock at 16MHz for device 01, and 25 MHz for devices 02, 03, and 04.
5 outputs at 5 MHz
15 outputs at 1 MHz
Alternate clock at 10 MHz
20 configurable logic blocks (CLB) at 5 MHz
30 CLBs at 1 MHz
10 horizontal long lines at 5 MHz
10 vertical long lines at 1 MHz
15 inputs at 5 MHz
3 inputs at 10 MHz

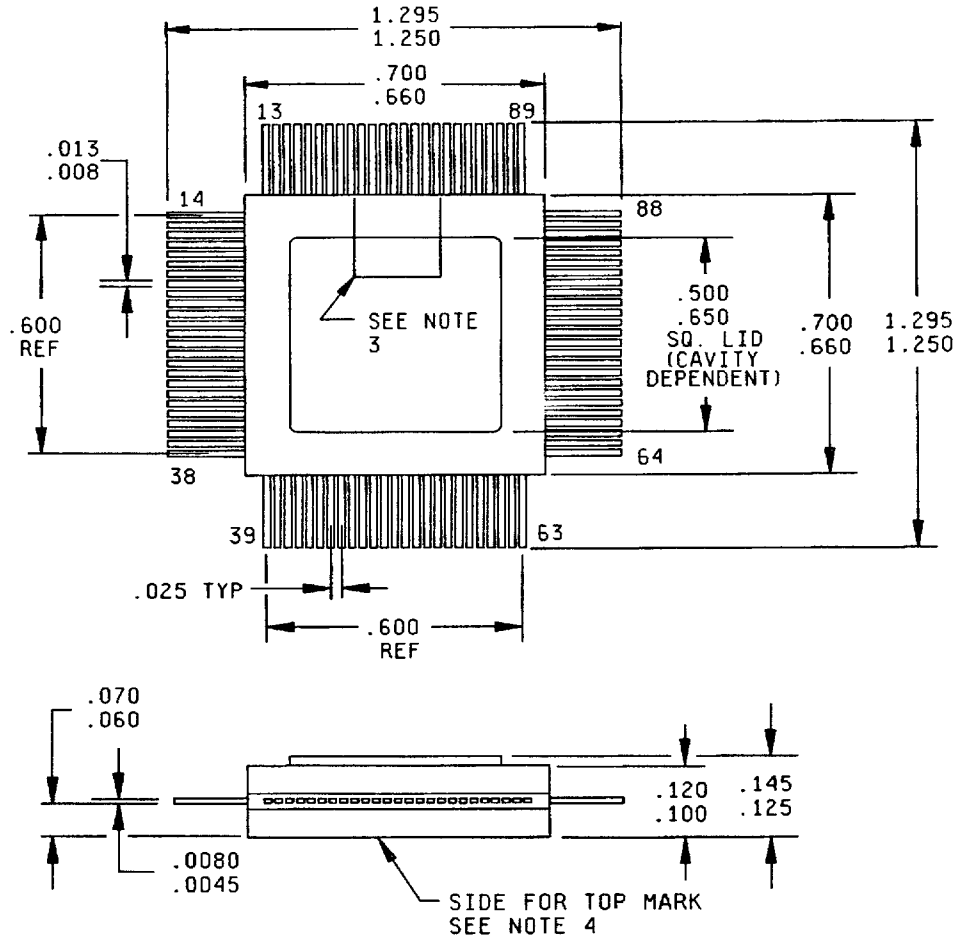
2/ $\overline{\text{PWRDWN}}$ transitions must occur during operational V_{CC} levels.

3/ Parameter is not directly tested. Devices are first 100 percent functionally tested. Benchmark patterns (t_{B1-9}) are then used to determine the compliance of this parameter. Characterization data are taken at initial device testing, prior to the introduction of significant changes, and at least twice yearly to monitor correlation between benchmark patterns and this parameter (class M only).

4/ Minimum CLOCK widths for the auxiliary buffer are 1.25 times the t_{CH} and t_{CL}.

5/ These parameters are for clock pulses internal to the chip. Externally applied clock, increases value by 20 percent.

Case Y

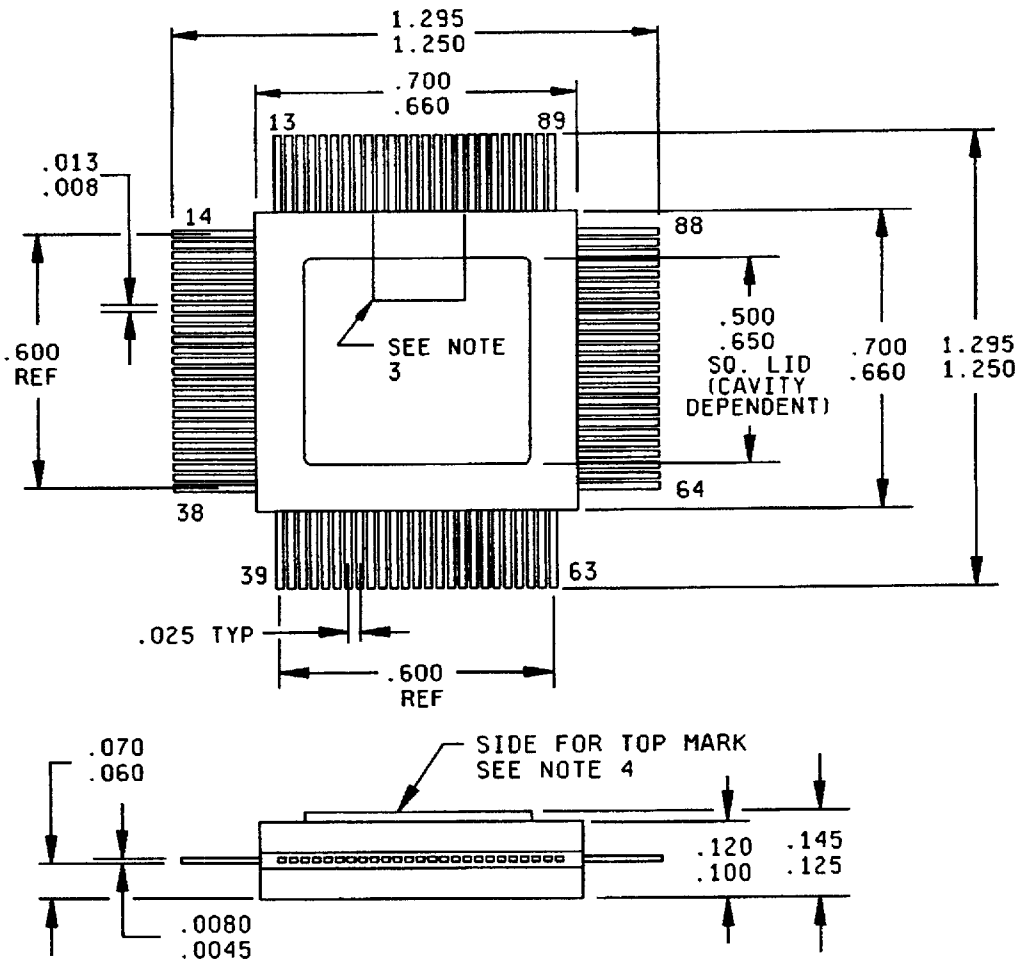


Inches	mm	Inches	mm
.0045	0.114	.125	3.18
.008	0.20	.145	3.68
.013	0.33	.500	12.70
.025	0.64	.600	15.24
.060	1.52	.650	16.51
.070	1.78	.660	16.76
.100	2.54	.700	17.78
.120	3.05	1.250	31.75
		1.295	32.89

NOTES:
1. Dimensions are in inches.
2. The US goverment preferred system of measurement is the metric SI system. However, this item was originally designed using inch-pound units of measurement. In the event of conflict between the metric and inch-pound units, the inch-pound units shall take precedence.
3. Pin 1 identifier location. Pin 1 is the middle pin on the side with center justified identifier mark. May be a notch, dot, or triangle.
4. Top side mark location, product mark is located on the nonlid side of package; i.e., lid side facing down. When mounted in this position, the pin out is clockwise.

FIGURE 1. Case outline.

Case T

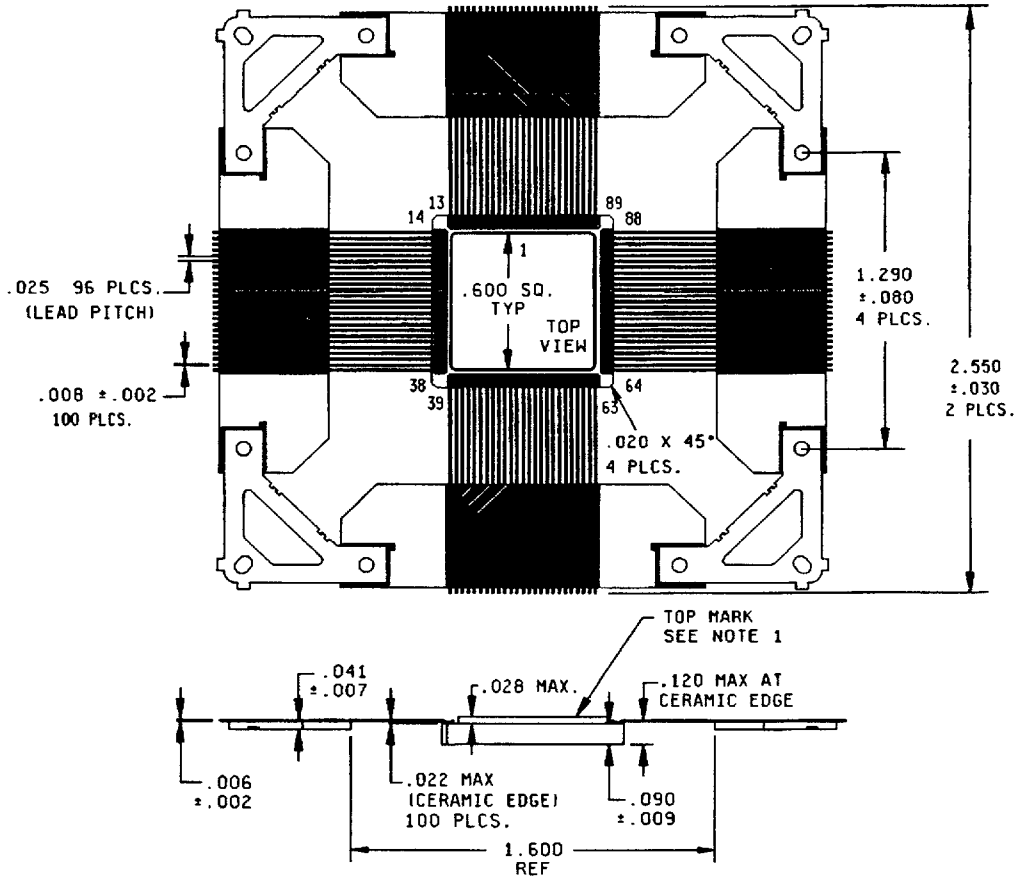


Inches	mm	Inches	mm
.0045	0.114	.125	3.18
.008	0.20	.145	3.68
.013	0.33	.500	12.70
.025	0.64	.600	15.24
.060	1.52	.650	16.51
.070	1.78	.660	16.76
.100	2.54	.700	17.78
.120	3.05	1.250	31.75
		1.295	32.89

NOTES:
1. Dimensions are in inches.
2. The US goverment preferred system of measurement is the metric SI system. However, this item was originally designed using inch-pound units of measurement. In the event of conflict between the metric and inch-pound units, the inch-pound units shall take precedence.
3. Pin 1 identifier location. Pin 1 is the middle pin on the side center justified identifier mark. May be a notch, dot, or triangle.
4. Top side mark location, product mark is located on the lid side of package; i.e., lid side facing up. When mounted in this position, the pin out is counterclockwise

FIGURE 1. Case outline - Continued.

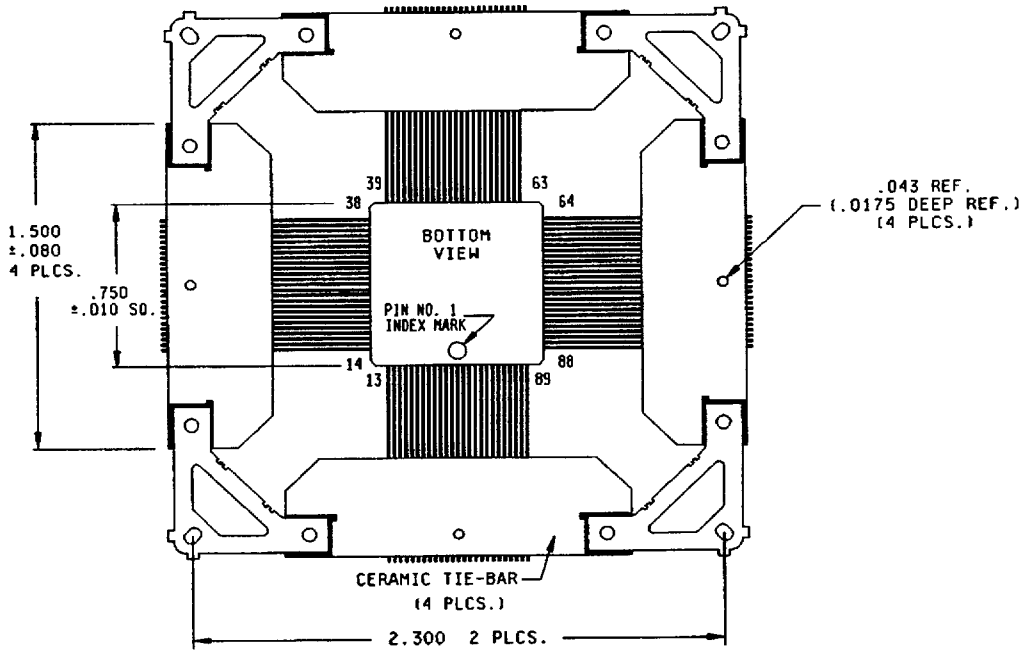
Case M



NOTES:

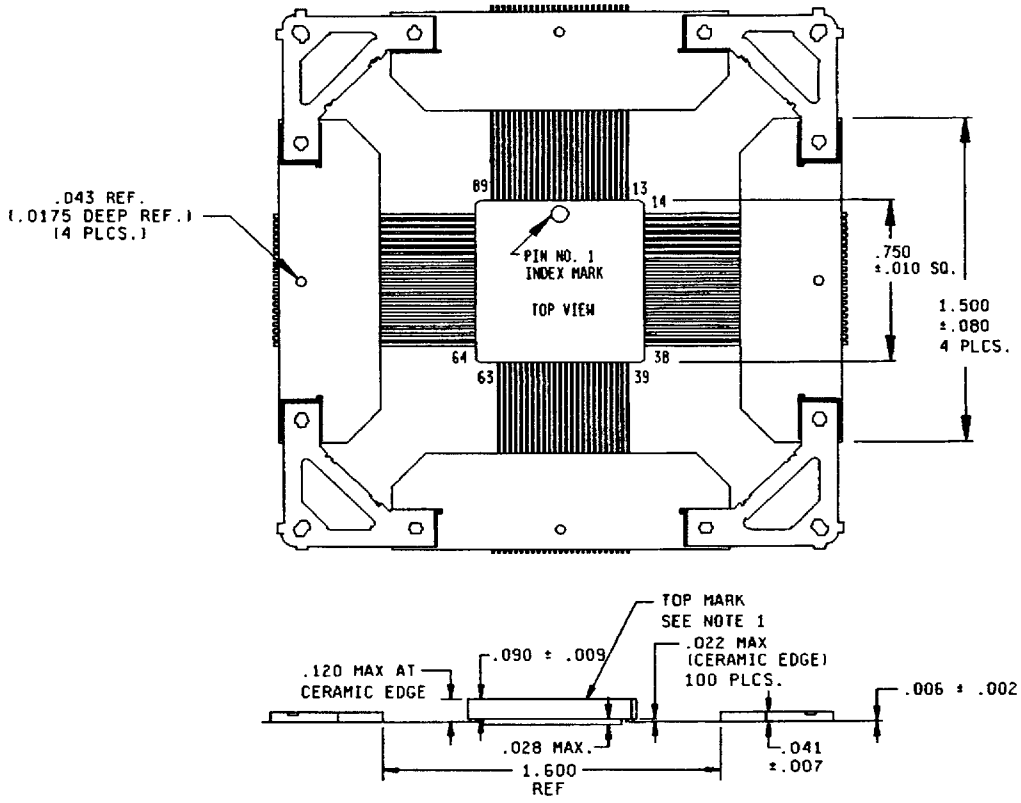
1. Top side mark location, product mark is located on the lid side of package; i.e., lid side facing up. When mounted in this position, the pin out is counterclockwise
2. Dimensions are in inches.
3. The US goverment preferred system of measurement is the metric SI system. However, this item was originally designed using inch-pound units of measurement. In the event of conflict between the metric and inch-pound units, the inch-pound units shall take precedence.
4. Pin 1 identifier location. Pin 1 is the middle pin on the side with center justified identifier mark. May be a notch, dot, or triangle.
5. The leads of this package style shall be protected from mechanical distortion and damage such that dimensions pertaining to relative lead/body "true positions" and lead "coplanarity" are always maintained until the next higher level package attachment process is complete. Package lead protection mechanisms (tie bars) are shown on the drawing for reference only. When microcircuit devices contained in this package style are shipped for use in Government equipment, or shipped directly to the Government as spare parts or mechanical qualification samples, lead "true position" and "coplanarity" protection shall be in place.

FIGURE 1. Case outline - Continued.



Inches	mm	Inches	mm
.002	0.05	.025	0.64
.006	0.15	.028	0.71
.008	0.20	.030	0.76
.009	0.23	.090	2.29
.010	0.25	.120	3.05
.020	0.51	.600	15.24
.022	0.56	.750	19.05
		2.550	64.77

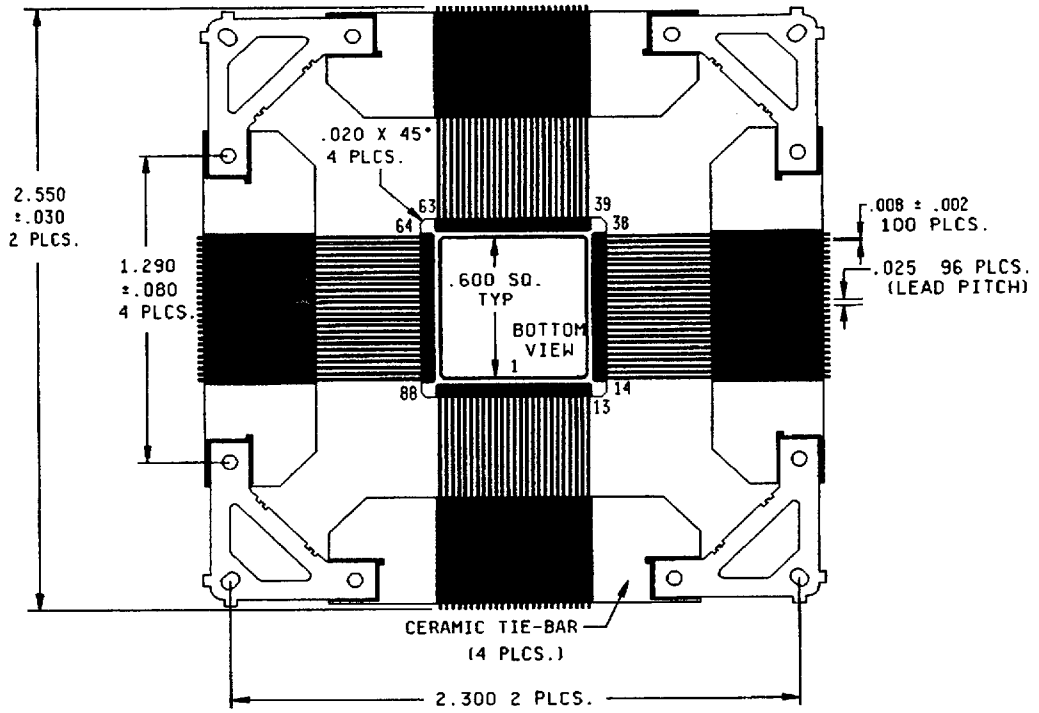
FIGURE 1. Case outline - Continued.



NOTES:

1. Top side mark location, product mark is located on the lid side of package; i.e., lid side facing up. When mounted in this position, the pin out is counterclockwise
2. Dimensions are in inches.
3. The US goverment preferred system of measurement is the metric SI system. However, this item was originally designed using inch-pound units of measurement. In the event of conflict between the metric and inch-pound units, the inch-pound units shall take precedence.
4. Pin 1 identifier location. Pin 1 is the middle pin on the side with center justified identifier mark. May be a notch, dot, or triangle.
5. The leads of this package style shall be protected from mechanical distortion and damage such that dimensions pertaining to relative lead/body "true positions" and lead "coplanarity" are always maintained until the next higher level package attachment process is complete. Package lead protection mechanisms (tie bars) are shown on the drawing for reference only. When microcircuit devices contained in this package style are shipped for use in Government equipment, or shipped directly to the Government as spare parts or mechanical qualification samples, lead "true position" and "coplanarity" protection shall be in place.

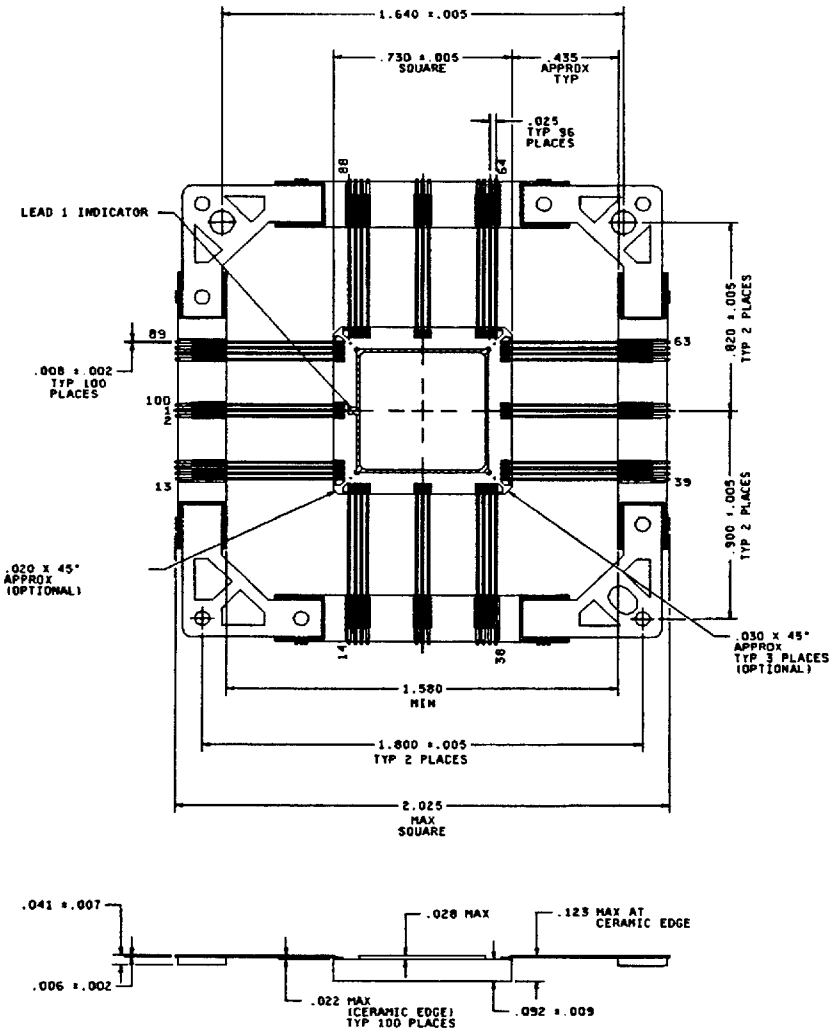
FIGURE 1. Case outline - Continued.



Inches	mm	Inches	mm
.002	0.05	.025	0.64
.006	0.15	.028	0.71
.008	0.20	.030	0.76
.009	0.23	.090	2.29
.010	0.25	.120	3.05
.020	0.51	.600	15.24
.022	0.56	.750	19.05
		2.550	64.77

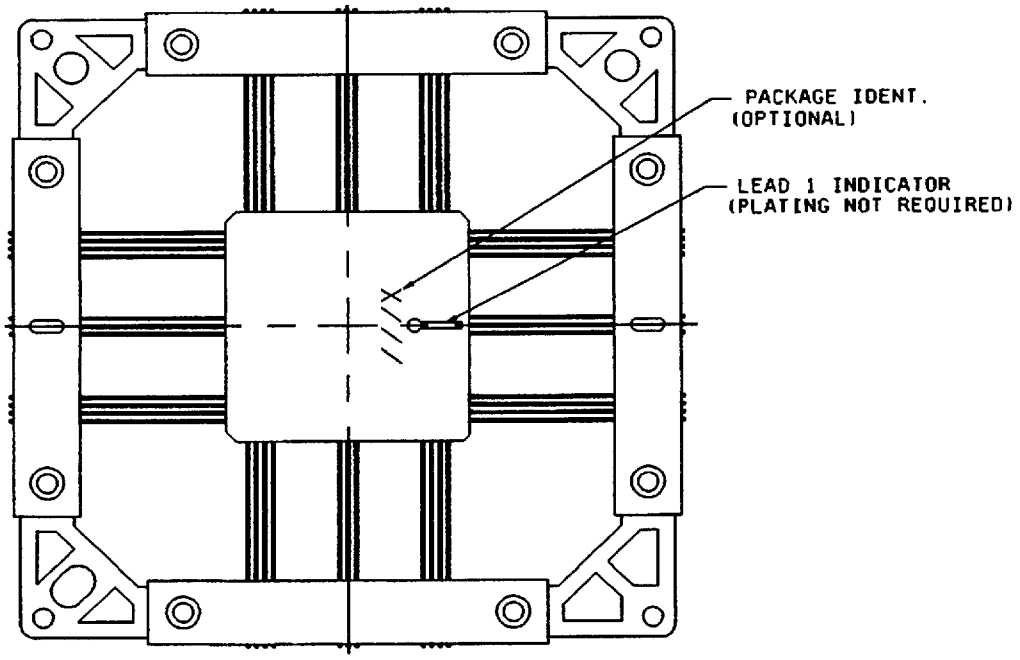
FIGURE 1. Case outline - Continued.

Case 9



Inches	mm	Inches	mm
.002	.05	.041	1.04
.005	.13	.092	2.34
.006	.15	.123	3.12
.007	.18	.435	11.05
.008	.20	.730	18.54
.020	.51	.820	20.83
.022	.56	.900	22.86
.025	.64	1.580	40.13
.028	.71	1.640	41.68
.030	.76	1.800	45.72
		2.025	51.44

FIGURE 1. Case outline - Continued.



NOTES:

1. Dimensions are in inches.
2. The US goverment preferred system of measurement is the metric SI system. However, this item was originally designed using inch-pound units of measurement. In the event of conflict between the metric and inch-pound units, the inch-pound units shall take precedence.
3. Pin 1 identifier location. Pin 1 is the middle pin on the side with center justified identifier mark. May be a notch, dot, or triangle or other metallized feature.
4. Top side mark location, product mark is located on the lid side of package; i.e., lid side facing up. When mounted in this position, the pin out is counterclockwise
5. The leads of this package style shall be protected from mechanical distortion and damage such that dimensions pertaining to relative lead/body "true positions" and lead "coplanarity" are always maintained until the next higher level package attachment process is complete. Package lead protection mechanisms (tie bars) are shown on the drawing for reference only. When microcircuit devices contained in this package style are shipped for use in Government equipment, or shipped directly to the Government as spare parts or mechanical qualification samples, lead "true position" and "coplanarity" protection shall be in place.

FIGURE 1. Case outline - Continued.

Case outline X and Z

Device types	All	Device types	All	Device types	All
Terminal number	Terminal symbol	Terminal number	Terminal symbol	Terminal number	Terminal symbol
A1	A9-I/O	C10	DOUT-I/O	J1	I/O
A2	A8-I/O	C11	RCLK-I/O	J2	M1-RDATA
A3	A11-I/O	D1	I/O	J5	I/O
A4	I/O	D2	I/O	J6	GND
A5	A6-I/O	D10	WRT-D1-I/O	J7	I/O
A6	A13-I/O	D11	NC	J10	DONE-PG
A7	A14-I/O	E1	I/O	J11	XTL1-I/O-BCLKIN
A8	NC	E2	I/O	K1	I/O
A9	A3-I/O	E3	I/O	K2	M2-I/O
A10	A2-I/O	E9	I/O	K3	HDC-I/O
A11	CCLK	E10	D2-I/O	K4	I/O
B1	NC	E11	CS1-I/O	K5	I/O
B2	PWRDWN	F1	I/O	K6	INIT-I/O
B3	A10-I/O	F2	I/O	K7	I/O
B4	NC	F3	V_{CC}	K8	I/O
B5	A12-I/O	F9	V_{CC}	K9	I/O
B6	A15-I/O	F10	D5-I/O	K10	MASTER RESET
B7	A4-I/O	F11	D3-I/O	K11	D7-I/O
B8	NC	G1	I/O	L1	MO-RTRIG
B9	CS2-A1-I/O	G2	I/O	L2	I/O
B10	WS-A0-I/O	G3	I/O	L3	LDC-I/O
B11	DIN-D0-I/O	G9	I/O	L4	NC
C1	I/O	G10	CS0-I/O	L5	NC
C2	TCLKIN-I/O	G11	D4-I/O	L6	I/O
C3	INDEX PIN	H1	I/O	L7	I/O
C5	A7-I/O	H2	I/O	L8	I/O
C6	GND	H10	D6-I/O	L9	NC
C7	A5-I/O	H11	I/O	L10	NC
				L11	XT2-I/O

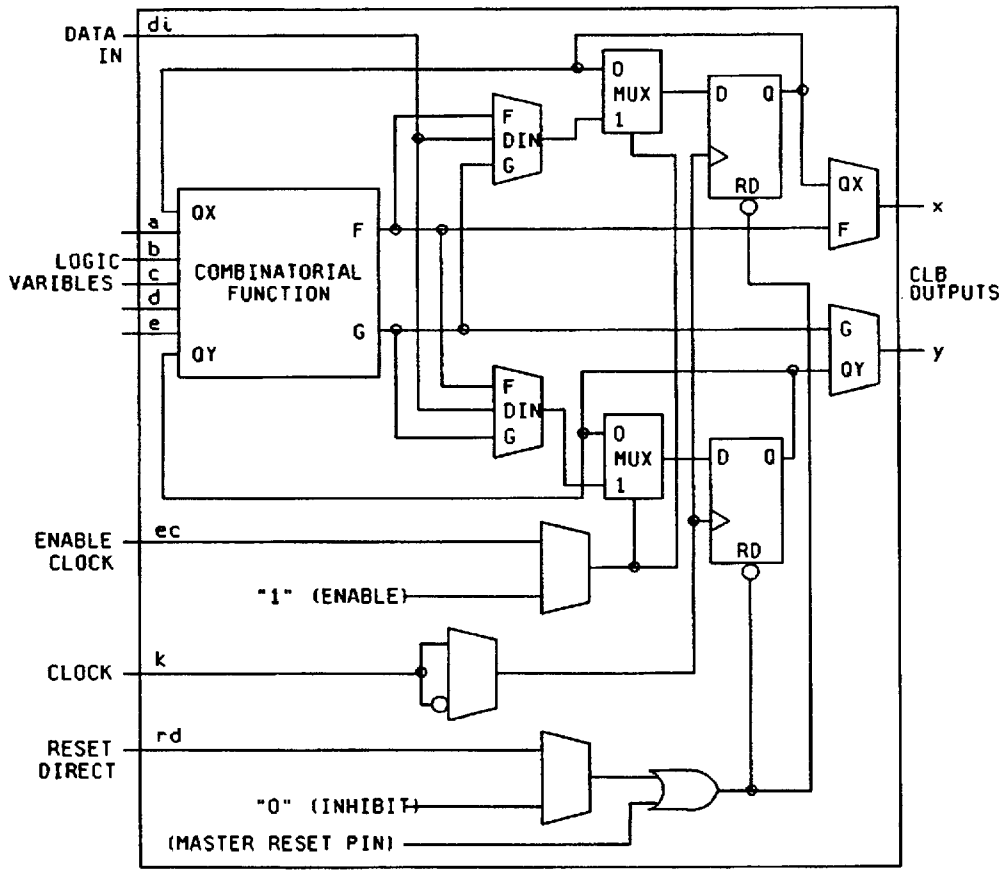
FIGURE 2. Terminal connections.

Case outline Y, U, T, M, N, and 9

Device types	All	Device types	All	Device types	All
Terminal number	Terminal symbol	Terminal number	Terminal symbol	Terminal number	Terminal symbol
1	GND	35	NC	68	D6-I/O
2	A13	36	NC	69	NC
3	A6	37	M1-RDATA	70	NC
4	A12	38	NC	71	I/O
5	A7	39	M0-RTRIG	72	D5-I/O
6	NC	40	NC	73	CSO
7	NC	41	M2	74	D4-I/O
8	A11	42	HDC	75	I/O
9	A8	43	I/O	76	V_{CC}
10	A10	44	LDC	77	D3-I/O
11	A9	45	NC	78	CS1
12	NC	46	NC	79	D2-I/O
13	NC	47	I/O	80	I/O
14	PWRDWN	48	I/O	81	NC
15	TCLKIN-I/O	49	I/O	82	NC
16	NC	50	INIT	83	D1-I/O
17	NC	51	GND	84	RCLK-RDY/BUSY
18	NC	52	I/O	85	DIN-D0-I/O
19	I/O	53	I/O	86	DOUT-I/O
20	I/O	54	I/O	87	CCLK
21	I/O	55	I/O	88	NC
22	I/O	56	I/O	89	NC
23	I/O	57	I/O	90	WS-A0
24	I/O	58	I/O	91	CS2-A1
25	I/O	59	NC	92	NC
26	V_{CC}	60	NC	93	A2
27	I/O	61	XTL2-I/O	94	A3
28	I/O	62	NC	95	NC
29	I/O	63	RESET	96	NC
30	I/O	64	NC	97	A15
31	I/O	65	DONE-PG	98	A4
32	I/O	66	D7-I/O	99	A14
33	I/O	67	BCLKIN-XTL1-I/O	100	A5
34	I/O				

FIGURE 2. Terminal connections - Continued.

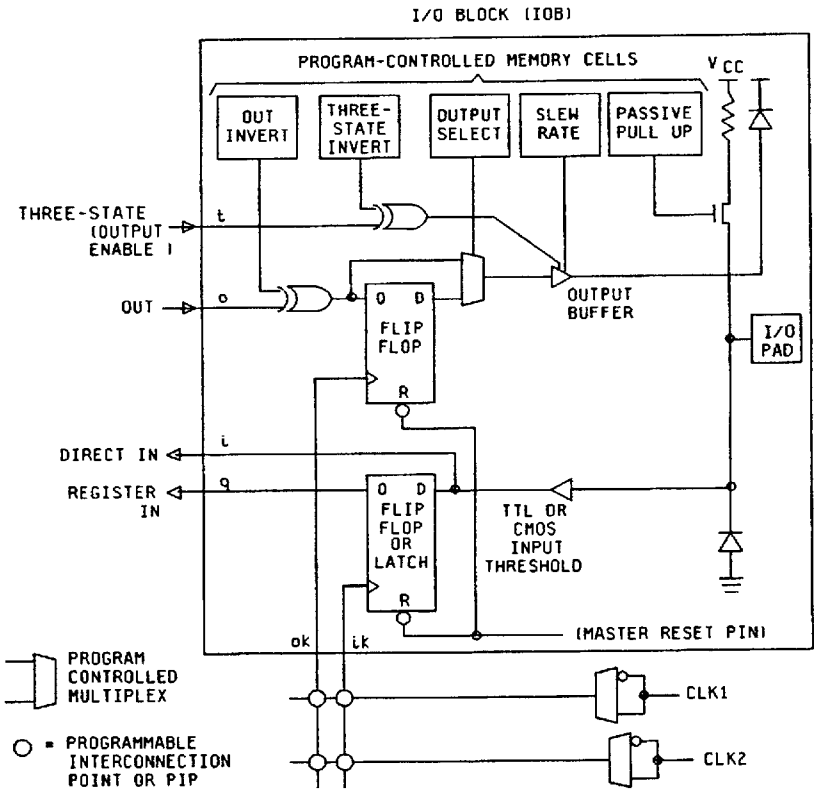
CONFIGURABLE LOGIC BLOCK (CLB)



NOTE: Each CLB includes a combinatorial logic section, two flip-flops, and a program memory controlled multiplexer selection of function.

It has: Five logic variable inputs: a, b, c, d, and e
A direct data input: di
An enable clock: ec
A clock (invertible): k
An asynchronous reset: rd
Two outputs: x and y

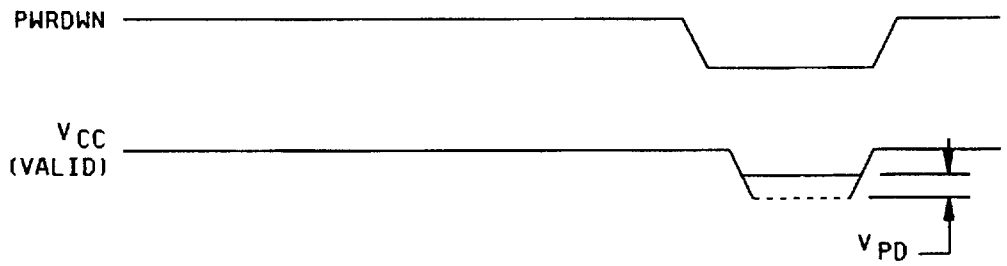
FIGURE 3. Logic block diagrams.



NOTE: The IOB includes input and output storage elements and I/O options selected by configuration memory cells. A choice of two clocks is available on each die edge. The polarity of each clock line (not each flip-flop or latch) is programmable. A clock line that triggers the flip-flop on the rising edge is an active low latch enable (latch transparent) signal and vice versa. Passive pull-up can only be enabled on inputs, not on outputs. All user inputs are programmed for TTL or CMOS thresholds.

FIGURE 3. Logic block diagrams - Continued.

GENERAL LOGIC CELL ARRAY (LCA) SWITCHING CHARACTERISTICS



NOTE: All timings except t_{TSHZ} and t_{TSON} are measured at 1.5 V levels wit[illegible]pF minimum output load. For input signals, rise and fall times are less than 6.0 ns, with low amplit[illegible] 0 V, and high amplitude = 3.0 V.

FIGURE 4. Timing diagrams and s[illegible]ching characteristics.

CONFIGURABLE LOGIC BLOCK (CLB) SWITCHING CHARACTERISTICS

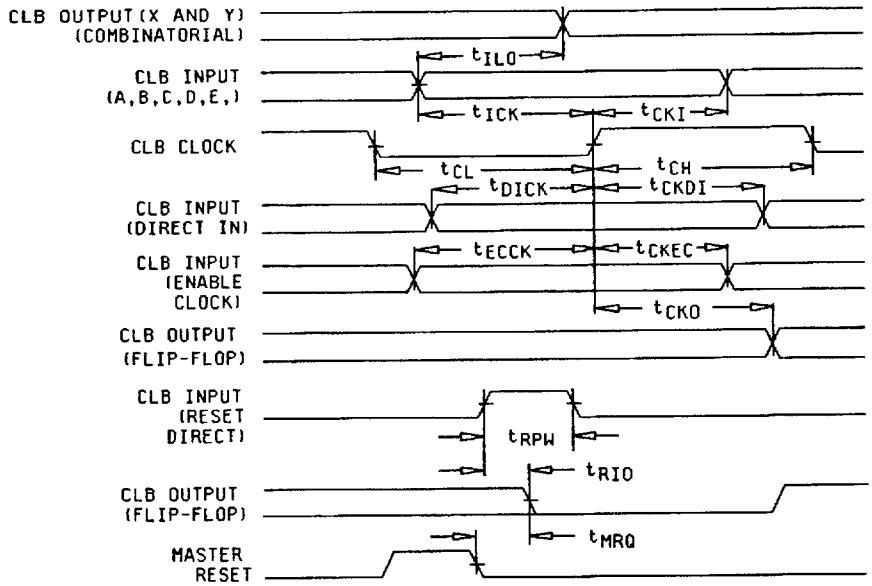
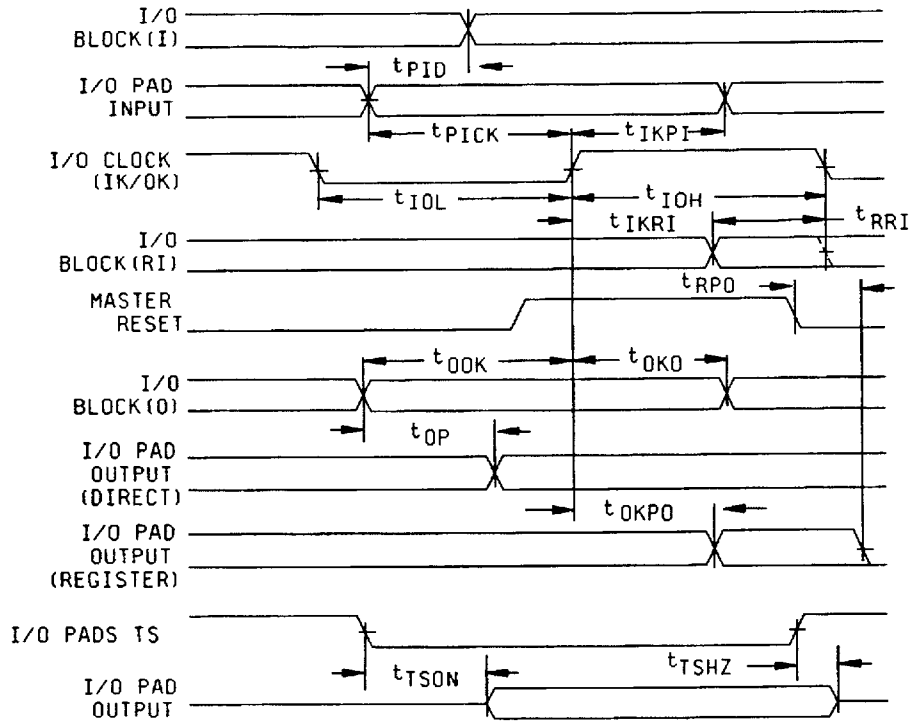


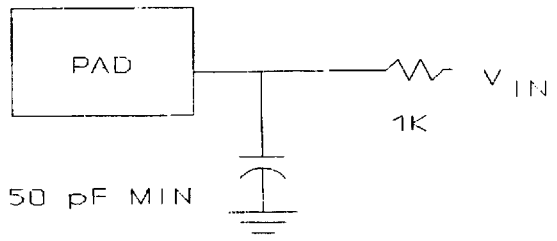
FIGURE 4. Timing diagrams and switching characteristics - Continued.

I/O BLOCK (IOB) SWITCHING CHARACTERISTICS

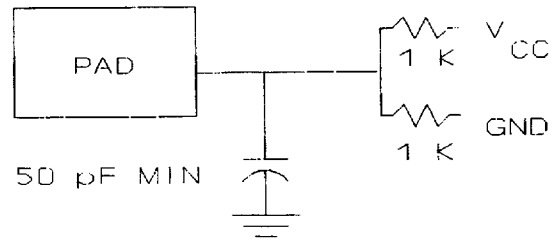


NOTE: t_{TSHZ} is determined when the output shifts 10 percent (of the output voltage swing) from V_{OL} level or V_{OH} level. See figure 5, circuit B herein for circuit used. t_{TSON} is measured at 0.5 V_{CC} level with V_{IN} = 0.0 V for three-state to active High, and V_{IN} = V_{CC} for three-state to active low. See figure 5, circuit A herein for circuit used.

FIGURE 4. Timing diagrams and switching characteristics - Continued.



Circuit A



Circuit B

FIGURE 5. Load circuits.

TABLE IIA. Electrical test requirements. 1/ 2/ 3/ 4/ 5/ 6/ 7/

Line no.	Test requirements	Subgroups (in accordance with MIL-STD-883, method 5005, table I)	Subgroups (in accordance with MIL-I-38535, table III)	
		Device class M	Device class Q	Device class V
1	Interim electrical parameters (see 4.2)		1,7,9	1,7,9
2	Static burn-in (method 1015)	Required	Required	Required
3	Same as line 1			1*,7* Δ
4	Dynamic burn-in (method 1015)	Not required	Not required	Not required
5	Final electrical parameters	1*,2,3,7*, 8A,8B,9,10, 11	1*,2,3,7*, 8A,8B,9,10, 11	1*,2,3,7*, 8A,8B,9, 10,11
6	Group A test requirements	1,2,3,4**,7, 8A,8B,9,10, 11	1,2,3,4**,7, 8A,8B,9,10, 11	1,2,3,4**,7, 8A,8B,9,10, 11
7	Group C end-point electrical parameters	2,3,7, 8A,8B	1,2,3,7, 8A,8B Δ	1,2,3,7, 8A,8B,9, 10,11 Δ
8	Group D end-point electrical parameters	2,3, 8A,8B	2,3, 8A,8B	2,3, 8A,8B
9	Group E end-point electrical parameters	1,7,9	1,7,9	1,7,9

1/ Blank spaces indicate tests are not applicable.
2/ Any or all subgroups may be combined when using high-speed testers.
3/ Subgroups 7 and 8 functional tests shall verify the truth table.
4/ * indicates PDA applies to subgroup 1 and 7.
5/ ** see 4.4.1e.
6/ Δ indicates delta limit (see table IIB) shall be required where specified, and the delta values shall be computed with reference to the previous interim electrical parameters (see line 1).
7/ See 4.4.1d.

TABLE IIB. Delta limits at +25°C.

Parameter 1/	Device types
	All
I_{CCO} standby	±300 μA
I_{IL}, I_{OL}	±2 nA

1/ The above parameter shall be recorded before and after the required burn-in and life tests to determine the delta Δ

4.2.2 Additional criteria for device classes Q and V.

a. The burn-in test duration, test condition and test temperature or approved alternatives shall be as specified in the device manufacturer's QM plan in accordance with MIL-I-38535. The burn-in test circuit shall be maintained under document revision level control of the device manufacturer's Technology Review Board (TRB) in accordance with MIL-I-38535 and shall be made available to the acquiring or preparing activity upon request. The test circuit shall specify the inputs, outputs, biases, and power dissipation, as applicable, in accordance with the intent specified in test method 1015.

b. Interim and final electrical test parameters shall be as specified in table IIA herein.

c. Additional screening for device class V beyond the requirements of device class Q shall be as specified in appendix B of MIL-I-38535.

4.3 Qualification inspection for device classes Q and V. Qualification inspection for device classes Q and V shall be in accordance with MIL-I-38535. Inspections to be performed shall be those specified in MIL-I-38535 and herein for groups A, B, C, D, and E inspections (see 4.4.1 through 4.4.4).

4.4 Conformance inspection. Quality conformance inspection for device class M shall be in accordance with MIL-STD-883 (see 3.1 herein) and as specified herein. Inspections to be performed for device class M shall be those specified in method 5005 of MIL-STD-883 and herein for groups A, B, C, D, and E inspections (see 4.4.1 through 4.4.4). Technology conformance inspection for classes Q and V shall be in accordance with MIL-I-38535 including groups A, B, C, D, and E inspections and as specified herein except where option 2 of MIL-I-38535 permits alternate in-line control testing.

4.4.1 Group A inspection.

a. Tests shall be as specified in table IIA herein.

b. Subgroups 5 and 6 of table I of method 5005 of MIL-STD-883 shall be omitted.

c. For device class M subgroups 7 and 8 tests shall consist of verifying functionality of the device. These tests form a part of the vendors test tape and shall be maintained and available upon request. For device classes Q and V subgroups 7 and 8 shall include verifying the functionality of the device; these tests shall have been fault graded in accordance with MIL-STD-883, test method 5012 (see 1.5 herein).

d. O/V (latch-up) tests shall be measured only for initial qualification and after any design or process changes which may affect the performance of the device. For device class M procedures and circuits shall be maintained under document revision level control by the manufacturer and shall be made available to the preparing activity or acquiring activity upon request. For device classes Q and V, the procedures and circuits shall be shall be under the control of the device manufacturer's technical review board (TRB) in accordance with MIL-I-38535 and shall be made available to the preparing activity or acquiring activity upon request. Testing shall be on all pins, on 5 devices with zero failures. Latch-up test shall be considered destructive. Information contained in JEDEC standard number 17 may be used for reference.

e. Subgroup 4 (C_{IN} and C_{OUT} measurements) shall be measured only for initial qualification and after any process or design changes which may affect input or output capacitance. Capacitance shall be measured between the designated terminal and GND at a frequency of 1 MHz. Sample size is five devices with no failures, and all input and output terminals tested.

4.4.2 Group C inspection. The group C inspection end-point electrical parameters shall be as specified in table IIA herein. Delta limits shall apply only to subgroup 1 of group C inspection and shall consist of tests specified in table IIB herein.

4.4.2.1 Additional criteria for device classes M . Steady-state life test conditions, method 1005 of MIL-STD-883:

a. Test condition D. For device class M, the test circuit shall be maintained by the manufacturer under document revision level control and shall be made available to the preparing or acquiring activity upon request. For device classes M the test circuit shall specify the inputs, outputs, biases, and power dissipation, as applicable, in accordance with the intent specified in test method 1005.
b. T_A = +125°C, minimum.

c. Test duration: 1,000 hours, except as permitted by method 1005 of MIL-STD-883.

4.4.2.2 Additional criteria for device classes Q and V. The steady-state life test duration, test condition and test temperature, or approved alternatives shall be as specified in the device manufacturer's QM plan in accordance with MIL-I-38535. The test circuit shall be maintained under document revision level control by the device manufacturer's TRB in accordance with MIL-I-38535 and shall be made available to the acquiring or preparing activity upon request. The test circuit shall specify the inputs, outputs, biases, and power dissipation, as applicable, in accordance with the intent specified in test method 1005.

4.4.3 Group D inspection. The group D inspection end-point electrical parameters shall be as specified in table IIA herein.

4.4.4 Group E inspection. Group E inspection is required only for parts intended to be marked as radiation hardness assured (see 3.5 herein). RHA levels for device classes Q and V shall be M, D, R, and H and for device class M shall be M and D.

a. End-point electrical parameters shall be as specified in table IIA herein.

b. For device classes M the devices shall be subjected to radiation hardness assured tests as specified in MIL-I-38535, appendix A, for the RHA level being tested. For device classes Q and V, the devices or test vehicle shall be subjected to radiation hardness assured tests as specified in MIL-I-38535 for the RHA level being tested. All device classes must meet the postirradiation end-point electrical parameter limits as defined in table I at T_A = +25°C ±5°C, after exposure, to the subgroups specified in table IIA herein.

c. When specified in the purchase order or contract, a copy of the RHA delta limits shall be supplied.

4.5 Delta measurements for device classes Q and V. Delta measurements, as specified in table IIA, shall be made and recorded before and after the required burn-in screens and steady-state life tests to determine delta compliance. The electrical parameters to be measured, with associated delta limits are listed in table IIB. The device manufacturer may, at his option, either perform delta measurements or within 24 hours after life test perform final electrical parameter tests, subgroups 1, 7, and 9.

5. PACKAGING

5.1 Packaging requirements. The requirements for packaging shall be in accordance with MIL-STD-883 (see 3.1 herein) for device class M and MIL-I-38535 for device classes Q and V.

6. NOTES

(This section contains information of a general or explanatory nature that may be helpful, but is not mandatory.)

6.1 Intended use. Microcircuits conforming to this drawing are intended for use for Government microcircuit applications (original equipment), design applications, and logistics purposes.

6.1.1 Replaceability. Microcircuits covered by this drawing will replace the same generic device covered by a contractor-prepared specification or drawing.

6.1.2 Substitutability. Device class Q devices will replace device class M devices.

6.2 Configuration control of SMD's. All proposed changes to existing SMD's will be coordinated with the users of record for the individual documents. This coordination will be accomplished in accordance with MIL-STD-973 using DD Form 1692, Engineering Change Proposal.

6.3 Record of users. Military and industrial users shall inform Defense Electronics Supply Center when a system application requires configuration control and which SMD's are applicable to that system. DESC will maintain a record of users and this list will be used for coordination and distribution of changes to the drawings. Users of drawings covering microelectronic devices (FSC 5962) should contact DESC-EC, telephone (513) 296-6047.

6.4 Comments. Comments on this drawing should be directed to DESC-EC, Dayton, Ohio 45444-5270, or telephone (513) 296-5377.

6.5 Symbols, definitions, and functional descriptions.

PWRDWN	POWER-DOWN.
MO	MODE 0.
RTRIG	READ TRIGGER.
M1	MODE 1.
RDATA	READ DATA.
M2	MODE 2.
HDC	HIGH DURING CONFIGURATION.
LDC	LOW DURING CONFIGURATION
RESET	RESET
DONE	DONE
PG	PROGRAM
B CLKIN	BCLKIN
XTL1	EXTERNAL CRYSTAL
XTL2	EXTERNAL CRYSTAL
CCLK	CONFIGURATION CLOCK
DOUT	DATA OUT
DIN	DATA IN
CSO	CHIP SELECT, WRITE.
CS1	CHIP SELECT, WRITE.
CS2	CHIP SELECT, WRITE.
WS	CHIP SELECT, WRITE.
RCLK	READ CLOCK.
RDY/BUSY	During peripheral parallel mode configuration, this pin indicates when the chip is ready for another byte of data to be written into it. After configuration is complete, this pin becomes a user programmed I/O pin.
TCLKIN	TCLKIN
INIT	INIT
D0-D7	DATA
A0-A15	ADDRESS
I/O	INPUT/OUTPUT(DEDICATED).
V_{CC}	+5.0 V SUPPLY VOLTAGE.
GND	GROUND

6.6 One part - one part number system. The one part - one part number system described below has been developed to allow for transitions between identical generic devices covered by the three major microcircuit requirements documents (MIL-H-38534, MIL-I-38535, and 1.2.1 of MIL-STD-883) without the necessity for the generation of unique PIN's. The three military requirements documents represent different class levels, and previously when a device manufacturer upgraded military product from one class level to another, the benefits of the upgraded product were unavailable to the Original Equipment Manufacturer (OEM), that was contractually locked into the original unique PIN. By establishing a one part number system covering all three documents, the OEM can acquire to the highest class level available for a given generic device to meet system needs without modifying the original contract parts selection criteria.

Military documentation format	Example PIN under new system	Manufacturing source listing	Document listing
New MIL-H-38534 Standardized Military Drawings	5962-XXXXXZZ(H or K)YY	QML-38534	MIL-BUL-103
New MIL-I-38535 Standardized Military Drawings	5962-XXXXXZZ(Q or V)YY	QML-38535	MIL-BUL-103
New 1.2.1 of MIL-STD-883 Standardized Military Drawings	5962-XXXXXZZ(M)YY	MIL-BUL-103	MIL-BUL-103

6.7 Additional operating data.

a. Power on delay is 2^{14} cycles from the non-master mode. This provides 11 to 33 ms of wait time.

b. Power on delay is 2^{16} cycles for the master mode. This provides 43 to 130 ms of wait time.

c. Clear is 375 cycles ±25 cycles and may take as long as 250 to 750 μs.

d. During normal power up, V_{CC} must rise from 2.0 V to V_{CC} minimum in less than 10 ms. If this does not occur, configuration must be delayed by using RESET.

6.8 Sources of supply.

6.8.1 Sources of supply for device classes Q and V. Sources of supply for device classes Q and V are listed in QML-38535. The vendors listed in QML-38535 have submitted a certificate of compliance (see 3.6 herein) to DESC-EC and have agreed to this drawing.

6.8.2 Approved sources of supply for device class M. Approved sources of supply for class M are listed in MIL-BUL-103. The vendors listed in MIL-BUL-103 have agreed to this drawing and a certificate of compliance (see 3.6 herein) has been submitted to and accepted by DESC-EC.

APPENDIX

10. SCOPE

10.1 Scope. This appendix contains the PIN substitution information to support the one part-one part number system. SMD 5962-89948XXM supersedes SMD 5962-89948. For new designs, after the date of this document the NEW PIN shall be used in lieu of the OLD PIN. For exsisting designs prior to the date of this document the NEW PIN can be used in lieu of the OLD PIN. This appendix is a mandatory part of the specification. The information contained herein is intended for compliance. The PIN substitution data shall be as follows.

20. APPLICABLE DOCUMENTS This section is not applicable to this appendix.

30. SUBSTITUTION DATA

New PIN	Old PIN
5962-8994801MXX	5962-8994801XX
5962-8994801MYX	5962-8994801YX
5962-8994801MZX	not originally available
5962-8994801MUX	not originally available
5962-8994801MTX	not originally available
5962-8994801MMX	not originally available
5962-8994801MNX	not originally available
5962-8994801M9X	not originally available
5962-8994802MXX	5962-8994802XX
5962-8994802MYX	5962-8994802YX
5962-8994802MZX	not originally available
5962-8994802MUX	not originally available
5962-8994802MTX	not originally available
5962-8994802MMX	not originally available
5962-8994802MNX	not originally available
5962-8994802M9X	not originally available
5962-8994803MXX	not originally available
5962-8994803MYX	not originally available
5962-8994803MZX	not originally available
5962-8994803MUX	not originally available
5962-8994803MTX	not originally available
5962-8994803MMX	not originally available
5962-8994803MNX	not originally available
5962-8994803M9X	not originally available
5962-8994804MXX	not originally available
5962-8994804MYX	not originally available
5962-8994804MZX	not originally available
5962-8994804MUX	not originally available
5962-8994804MTX	not originally available
5962-8994804MMX	not originally available
5962-8994804MNX	not originally available
5962-8994804M9X	not originally available