REVISIONS			
LTR	DESCRIPTION	DATE (YR-MO-DA)	APPROVED
A	Update table I. Changes to timing waveforms. Add package Z. Editorial changes throughout.	92-11-05	M.L. Poelking
B	Add device types 02 and 03. Editorial changes throughout.	94-06-17	M.L. Poelking

THE ORIGINAL FIRST PAGE OF THIS DRAWING HAS BEEN REPLACED

REV																			
SHEET																			
REV	B	B	B	B	B	B	B	B	B	B	B								
SHEET	15	16	17	18	19	20	21	22	23	24	25								

REV STATUS OF SHEETS	REV	B	B	B	B	B	B	B	B	B	B	B	B	B	B
	SHEET	1	2	3	4	5	6	7	8	9	10	11	12	13	14

PMIC N/A

STANDARDIZED MILITARY DRAWING

THIS DRAWING IS AVAILABLE FOR USE BY ALL DEPARTMENTS AND AGENCIES OF THE DEPARTMENT OF DEFENSE

AMSC N/A

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DRAWING APPROVAL DATE
90-09-11

REVISION LEVEL
B

DEFENSE ELECTRONICS SUPPLY CENTER
DAYTON, OHIO 45444

MICROCIRCUIT, DIGITAL, CMOS, 16-BIT CASCADABLE ALU, MONOLITHIC SILICON

SIZE	CAGE CODE	5962-89959
A	67268	

SHEET 1 OF 25

DESC FORM 193
JUL 91

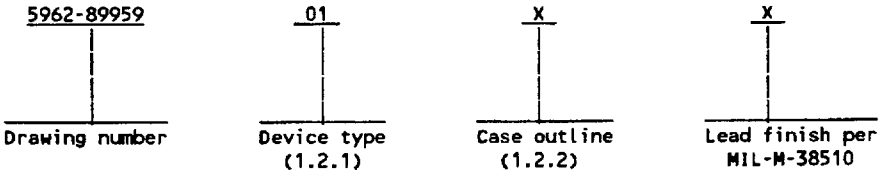
5962-E290-94

DISTRIBUTION STATEMENT A. Approved for public release; distribution is unlimited.

1. SCOPE

1.1 Scope. This drawing describes device requirements for class B microcircuits in accordance with 1.2.1 of MIL-STD-883, "Provisions for the use of MIL-STD-883 in conjunction with compliant non-JAN devices".

1.2 Part or Identifying Number (PIN). The complete PIN shall be as shown in the following example:



1.2.1 Device type(s). The device type(s) shall identify the circuit function as follows:

Device type	Generic number	Circuit function
01	L4C381-45 ns	16-bit cascadable ALU
02	L4C381-30 ns	16-bit cascadable ALU
03	L4C381-25 ns	16-bit cascadable ALU

1.2.2 Case outline(s). The case outline(s) shall be as designated in MIL-STD-1835 and as follows:

Outline letter	Descriptive designator	Terminals	Package style
X	CMGA15-P68	68	Pin grid array
Y	CQCC1-N68	68	Square chip carrier package
Z	CMGA3-P68	68	Pin grid array

1.2.3 Lead finish. The lead finish shall be as specified in MIL-STD-883 (see 3.1 herein). Finish letter "X" shall not be marked on the microcircuit or its packaging. The "X" designation is for use in specifications when lead finishes A, B, and C are considered acceptable and interchangeable without preference.

1.3 Absolute maximum ratings.

Storage temperature range	-65°C to +150°C
Maximum power dissipation (P_D) 1/	420 mW
V_{CC} supply voltage with respect to ground range	-0.5 V dc to +7.0 V dc
Input signal with respect to ground range	-3.0 V dc to +7.0 V dc
Signal applied to high impedance outputs range	-3.0 V dc to +7.0 V dc
Current into low outputs	25 mA
Lead temperature (soldering, 10 seconds)	+300°C
Junction temperature (T_J)	+175°C
Thermal resistance, junction-to-case (Θ_{JC})	See MIL-STD-1835

1.4 Recommended operating conditions.

Supply voltage rance (V_{CC})	4.5 V dc to 5.5 V dc
Case operating temperature range (T_C)	-55°C to +125°C

1/ Must withstand the added P_D due to short circuit test; e.g., I_{OS}.

2. APPLICABLE DOCUMENTS

2.1 Government specification, standards, and bulletin. Unless otherwise specified, the following specification, standards, and bulletin of the issue listed in that issue of the Department of Defense Index of Specifications and Standards specified in the solicitation, form a part of this drawing to the extent specified herein.

SPECIFICATION

MILITARY

MIL-I-38535 - Integrated Circuits (Microcircuits) Manufacturing, General Specification for.

STANDARDS

MILITARY

MIL-STD-883 - Test Methods and Procedures for Microelectronics.
MIL-STD-1835 - Microcircuit Case Outlines.

BULLETIN

MILITARY

MIL-BUL-103 - List of Standardized Military Drawings (SMD's).

(Copies of the specification, standards, and bulletin required by manufacturers in connection with specific acquisition functions should be obtained from the contracting activity or as directed by the contracting activity.)

2.2 Order of precedence. In the event of a conflict between the text of this drawing and the references cited herein, the text of this drawing shall take precedence.

3. REQUIREMENTS

3.1 Item requirements. The individual item requirements shall be in accordance with 1.2.1 of MIL-STD-883, "Provisions for the use of MIL-STD-883 in conjunction with compliant non-JAN devices" and as specified herein. Product built to this drawing that is produced by a Qualified Manufacturer Listing (QML) certified and qualified manufacturer or a manufacturer who has been granted transitional certification to MIL-I-38535 may be processed as QML product in accordance with the manufacturers approved program plan and qualifying activity approval in accordance with MIL-I-38535. This QML flow as documented in the Quality Management (QM) plan may make modifications to the requirements herein. These modifications shall not affect form, fit, or function of the device. These modifications shall not affect the PIN as described herein. A "Q" or "QML" certification mark in accordance with MIL-I-38535 is required to identify when the QML flow option is used.

3.2 Design, construction, and physical dimensions. The design, construction, and physical dimensions shall be as specified in MIL-STD-883 (see 3.1 herein) and herein.

3.2.1 Case outline(s). The case outline(s) shall be in accordance with 1.2.2 herein.

3.2.2 Terminal connections. The terminal connections shall be as specified on figure 1.

3.2.3 Functional block diagram. The functional block diagram shall be as specified on figure 2.

3.2.4 Truth table. The truth table shall be as specified on figure 3.

3.2.5 Switching waveforms and test circuit. The switching waveforms and test circuit shall be as specified on figure 4.

3.3 Electrical performance characteristics. Unless otherwise specified herein, the electrical performance characteristics are as specified in table I and shall apply over the full case operating temperature range.

3.4 Electrical test requirements. The electrical test requirements shall be the subgroups specified in table II. The electrical tests for each subgroup are described in table I.

TABLE I. Electrical performance characteristics.

Test	Symbol	Conditions 1/ $-55°C \le T_C \le +125°C$ $4.5\ V \le V_{CC} \le 5.5\ V$ unless otherwise specified	Group A subgroups	Devices type	Limits		Unit
					Min	Max	
Output high voltage	V_{OH}	I_{OH} = -2 mA, V_{CC} = 4.5 V	1, 2, 3	All	2.4		V
Output low voltage	V_{OL}	I_{OL} = 8.0 mA, V_{CC} = 4.5 V				0.5	
Input high voltage	V_{IH}				2.0		
Input low voltage	V_{IL}				0.0		
Input current	I_{IX}	V_{CC} = 5.5 V				±20	µA
Output leakage current	I_{OZ}	V_{CC} = 5.5 V				±20	
Dynamic supply current	I_{CC1}	V_{CC} = 5.5 V 2/				30	mA
Quiesent supply current	I_{CC2}	V_{CC} = 5.5 V 3/				1.5	
Input capacitance	C_{IN}	f=1.0 MHz, V_{CC} = 5.0 V See 4.3.1c; V_{IN} = 0 V	4	All		5	pF
		V_{OUT} = 0 V				8	
Functional test		V_{CC} = 4.5 V, 5.5 V See 4.3.1d	7, 8				
Clock to F0-F15	1	FTAB = 0, FTF = 0, C_L = 30 pF, V_{CC} = 4.5 V, See figure 4	9, 10, 11	01		28	ns
				02		26	
				03		14	
Clock_to P, G	2			01		34	
				02		28	
				03		24	
Clock to OVF, ZERO	3			01		50	
				02		34	
				03		24	
Clock to C16	4			01		34	
				02		28	
				03		24	
C0 to OVF, ZERO	5	FTAB = 0, FTF = 0, C_L = 30 pF, V_{CC} = 4.5 V, See figure 4	9, 10, 11	01		32	ns
				02		22	
				03		18	
C0 to C16	6			01		23	
				02		22	
				03		18	

See footnotes at end of table.

TABLE I. Electrical performance characteristics - Continued.

Test	Symbol	Conditions 1/ $-55°C \le T_C \le +125°C$ $4.5\ V \le V_{CC} \le 5.5\ V$ unless otherwise specified	Group A subgroups	Devices type	Limits		Unit
					Min	Max	
S0-S2, OSA, OSB to P, G	7	FTAB = 0, FTF = 0, C_L = 30 pF, V_{CC} = 4.5 V, See figure 4	9, 10, 11	01		38	ns
				02		28	
				03		22	
S0-S2, OSA, OSB to OVF ZERO	8			01		38	
				02		28	
				03		24	
S0-S2, OSA, OSB to C16	9			01		38	
				02		28	
				03		22	
Clock to F0-F15	10	FTAB = 0, FTF = 1, C_L = 30 pF, V_{CC} = 4.5 V, See figure 4	9, 10, 11	01		56	
				02		34	
				03		25	
Clock to P, G	11			01		34	
				02		28	
				03		24	
Clock to OVF, ZERO	12			01		50	
				02		34	
				03		24	
Clock to C16	13			01		34	
				02		28	
				03		24	
Co to F0-F15	14			01		32	
				02		26	
				03		21	
C0 to OVF, ZERO	15			01		32	
				02		22	
				03		18	
C0 to C16	16			01		23	
				02		22	
				03		18	

See footnotes at end of table.

TABLE I. Electrical performance characteristics - Continued.

Test	Symbol	Conditions 1/ $-55°C \le T_C \le +125°C$ $4.5\ V \le V_{CC} \le 5.5\ V$ unless otherwise specified	Group A subgroups	Devices type	Limits		Unit
					Min	Max	
S0-S2, OSA, OSB to F0-F15	17	FTAB = 0, FTF = 1, C_L = 30 pF, V_{CC} = 4.5 V, See figure 4	9, 10, 11	01		46	ns
				02		30	
				03		25	
S0-S2, OSA, OSB to P, G	18			01		38	
				02		28	
				03		22	
S0-S2, OSA, OSB to OVF, ZERO	19			01		38	
				02		28	
				03		24	
S0-S2, OSA, OSB to C16	20			01		38	
				02		28	
				03		22	
A0-A15, B0-B15 to P, G	21	FTAB = 1, FTF = 0, C_L = 30 pF, V_{CC} = 4.5, See figure 4		01		32	
				02		28	
				03		20	
A0-A15, B0-B15 to OVF, ZERO	22			01		46	
				02		28	
				03		25	
A0-A15, B0-B15 to C16	23			01		36	
				02		28	
				03		22	
Clock to F0-F15	24			01		28	
				02		26	
				03		14	
C0 to OVF, ZERO	25			01		32	
				02		22	
				03		18	

See footnotes at end of table.

TABLE I. Electrical performance characteristics - Continued.

Test	Symbol	Conditions 1/ $-55°C \le T_C \le +125°C$ $4.5\ V \le V_{CC} \le 5.5\ V$ unless otherwise specified	Group A subgroups	Devices type	Limits		Unit
					Min	Max	
C0 to C16	26	FTAB = 1, FTF = 0, C_L = 30 pF, V_{CC} = 4.5 V, See figure 4	9, 10, 11	01		23	ns
				02		22	
				03		18	
S0-S2, OSA, OSB to P, G	27			01		38	
				02		28	
				03		22	
S0-S2, OSA, OSB to OVF, ZERO	28			01		38	
				02		28	
				03		24	
S0-S2, OSA, OSB to C16	29			01		38	
				02		28	
				03		22	
A0-A15, B0-B15 to F0-F15	30	FTAB = 1, FTF = 1, C_L = 30 pF, V_{CC} = 4.5 V, See figure 4	9, 10, 11	01		45	ns
				02		30	
				03		25	
A0-A15, B0-B15 to $\overline{P}$, $\overline{G}$	31			01		32	
				02		28	
				03		20	
A0-A15, B0-B15 to OVF, ZERO	32			01		46	
				02		28	
				03		25	
A0-A15, B0-B15 to C16	33			01		36	
				02		28	
				03		22	
C0 to F0-F15	34			01		32	
				02		26	
				03		21	
C0 to OVF, ZERO	35			01		32	
				02		22	
				03		18	

See footnotes at end of table.

TABLE I. Electrical performance characteristics - Continued.

Test	Symbol	Conditions 1/ $-55°C \le T_C \le +125°C$ $4.5\ V \le V_{CC} \le 5.5\ V$ unless otherwise specified	Group A subgroups	Devices type	Limits		Unit
					Min	Max	
C0 to C16	36	FTAB = 1, FTF = 1, C_L = 30 pF, V_{CC} = 4.5 V, See figure 4	9, 10, 11	01		23	ns
				02		22	
				03		18	
S0-S2, OSA, OSB to F0-F15	37			01		46	
				02		30	
				03		25	
S0-S2, OSA, OSB to P, G	38			01		38	
				02		28	
				03		22	
S0-S2, OSA, OSB to OVF, ZERO	39			01		38	
				02		28	
				03		24	
S0-S2, OSA, OSB to C16	40			01		38	
				02		28	
				03		22	
Clock (OSA,OSB = 0) to F0-F15	65			01		56	
				02		34	
				03		25	
Clock (OSA,OSB = 0) to P, G	41			01		34	ns
				02		28	
				03		24	
Clock (OSA,OSB = 0) to OVF, ZERO	42	FTAB = 1, FTF = 1, C_L = 30 pF, V_{CC} = 4.5 V, See figure 4	9, 10, 11	01		50	ns
				02		34	
				03		24	
Clock (OSA,OSB = 0) to C16	43			01		34	
				02		28	
				03		24	

See footnotes at end of table.

TABLE I. Electrical performance characteristics - Continued.

Test	Symbol	Conditions 1/ $-55°C \le T_C \le +125°C$ $4.5\ V \le V_{CC} \le 5.5\ V$ unless otherwise specified	Group A subgroups	Devices type	Limits		Unit
					Min	Max	
A0-A15,B0-B15 set-up time	44	FTAB = 0, C_L = 30 p,F V_{CC} = 4.5 V, See figure 4	9, 10, 11	01, 02	8		ns
				03	7		
A0-A15,B0-B15 hold time	45			01, 02	3		
				03	0		
A0-A15,B0-B15 set-up time	46	FTAB = 1, C_L = 30 pF, V_{CC} = 4.5 V, See figure 4		01	33		
				02	20		
				03	14		
A0-A15,B0-B15 hold time	47			01, 02	3		
				03	0		
$\overline{ENA}$, $\overline{ENB}$ set-up time	48	FTAB = 0, C_L = 30 pF, V_{CC} = 4.5 V, See figure 4		01, 02	10		
				03	7		
$\overline{ENA}$, $\overline{ENB}$ hold time	49			01, 02	2		
				03	0		
$\overline{ENF}$ set-up time	50	C_L = 30 pF, V_{CC} = 4.5 V, See figure 4		01, 02	10		
				03	7		
$\overline{ENF}$ hold time	51			01, 02	2		
				03	0		
C0 set-up time	52	FTAB = 0, V_{CC} = 4.5 V, See figure 4		01	20		
				02	12		
				03	14		
C0 hold time	53			All	0		
C0 set-up time	54	FTAB = 1, V_{CC} = 4.5 V, See figure 4		01	20		
				02	12		
				03	14		
C0 hold time	55			All	0		
S0-S2,OSA,OSB set-up time	56	FTAB = 0, V_{CC} = 4.5 V, See figure 4		01	36		
				02	20		
				03	19		
S0-S2,OSA,OSB hold time	57			All	0		

See footnotes at end of table.

TABLE I. Electrical performance characteristics - Continued.

Test	Symbol	Conditions 1/ $-55°C \le T_C \le +125°C$ $4.5\ V \le V_{CC} \le 5.5\ V$ unless otherwise specified	Group A subgroups	Devices type	Limits		Unit
					Min	Max	
S0-S2,OSA,OSB set-up time	58	FTAB = 0, V_{CC} = 4.5 V, See figure 4	9, 10, 11	01	36		ns
				02	20		
				03	19		
S0-S2,OSA,OSB hold time	59	FTAB = 1, V_{CC} = 4.5 V, See figure 4		All	0		
Minimum cycle time	60	V_{CC} = 4.5 V, See figure 4		01	38		
				02	26		
				03	20		
High going pulse	61			01	15		
				02	12		
				03	8		
Low going pulse	62			01	15		
				02	12		
				03	8		
Three-state enable time	63			01		20	
				02		18	
				03		14	
Three-state disable test	64	V_{CC} = 4.5 V, See figure 4 5/		01		20	
				02		18	
				03		14	

1/ Test conditions assume signal transition times of 5 ns or less, timing reference levels of 1.5 V, input pulse levels of 0 to 3.0 V and output loading of the specified I_{OL} and I_{OH} and 30 pF. Input voltages should be adjusted to compensate for inductive ground and V_{CC} noise to maintain required device input levels relative to devices supply pins. All test must be performed using worst-case test conditions, unless otherwise specified.

2/ For test purposes, not more than one output should be tested at a time. Duration of the short circuit should not exceed 1 second. Guaranteed if not tested to the specified limits.

3/ Tested with all outputs changing every cycle and no load at a 5 MHz clock rate.

4/ Tested with all inputs within 0.1 V of V_{CC} or ground, no load.

5/ Tested with I_{OL} = 10 mA, I_{OH} = 10 mA.

3.5 Marking. Marking shall be in accordance with MIL-STD-883 (see 3.1 herein). The part shall be marked with the PIN listed in 1.2 herein. In addition, the manufacturer's PIN may also be marked as listed in MIL-BUL-103 (see 6.6 herein).

3.6 Certificate of compliance. A certificate of compliance shall be required from a manufacturer in order to be listed as an approved source of supply in MIL-BUL-103 (see 6.6 herein). The certificate of compliance submitted to DESC-EC prior to listing as an approved source of supply shall affirm that the manufacturer's product meets the requirements of MIL-STD-883 (see 3.1 herein) and the requirements herein.

3.7 Certificate of conformance. A certificate of conformance as required in MIL-STD-883 (see 3.1 herein) shall be provided with each lot of microcircuits delivered to this drawing.

3.8 Notification of change. Notification of change to DESC-EC shall be required in accordance with MIL-STD-883 (see 3.1 herein).

3.9 Verification and review. DESC, DESC's agent, and the acquiring activity retain the option to review the manufacturer's facility and applicable required documentation. Offshore documentation shall be made available onshore at the option of the reviewer.

4. QUALITY ASSURANCE PROVISIONS

4.1 Sampling and inspection. Sampling and inspection procedures shall be in accordance with MIL-STD-883 (see 3.1 herein).

4.2 Screening. Screening shall be in accordance with method 5004 of MIL-STD-883, and shall be conducted on all devices prior to quality conformance inspection. The following additional criteria shall apply:

a. Burn-in test, method 1015 of MIL-STD-883.

(1) Test condition B. The test circuit shall be maintained by the manufacturer under document revision level control and shall be made available to the preparing or acquiring activity upon request. The test circuit shall specify the inputs, outputs, biases, and power dissipation, as applicable, in accordance with the intent specified in test method 1015 of MIL-STD-883.

(2) T_A = +125°C, minimum.

b. Interim and final electrical test parameters shall be as specified in table II herein, except interim electrical parameter tests prior to burn-in are optional at the discretion of the manufacturer.

Device types	01, 02, and 03	Device types	01, 02, and 03	Device types	01, 02, and 03
Case outlines	X and Z	Case outlines	X and Z	Case outlines	X and Z
Terminal number	Terminal symbol	Terminal number	Terminal symbol	Terminal number	Terminal symbol
A1	---	C1	A12	E1	CLK
A2	A8	C2	A11	E2	A15
A3	A7	C3	---	E3	---
A4	A5	C4	---	E4	---
A5	A3	C5	---	E5	---
A6	A1	C6	---	E6	---
A7	B15	C7	---	E7	---
A8	B13	C8	---	E8	---
A9	B11	C9	---	E9	---
A10	B9	C10	B5	E10	B1
A11	---	C11	B6	E11	B2
B1	A10	D1	A14	F1	GND
B2	A9	D2	A13	F2	V_{CC}
B3	A6	D3	---	F3	---
B4	A4	D4	---	F4	---
B5	A2	D5	---	F5	---
B6	A0	D6	---	F6	---
B7	B14	D7	---	F7	---
B8	B12	D8	---	F8	---
B9	B10	D9	---	F9	---
B10	B8	D10	B3	F10	$\overline{ENA}$
B11	B7	D11	B4	F11	B0

FIGURE 1. Terminal connections.

Device types	01, 02, and 03	Device types	01, 02, and 03	Device types	01, 02, and 03
Case outlines	X and Z	Case outlines	X and Z	Case outlines	X and Z
Terminal number	Terminal symbol	Terminal number	Terminal symbol	Terminal number	Terminal symbol
G1	$\overline{P}$	J1	$\overline{ENF}$	L1	---
G2	C16	J2	OVF	L2	F15
G3	---	J3	---	L3	F13
G4	---	J4	---	L4	F11
G5	---	J5	---	L5	F9
G6	---	J6	---	L6	F7
G7	---	J7	---	L7	F5
G8	---	J8	---	L8	F3
G9	---	J9	---	L9	F1
G10	FTAB	J10	S1	L10	F0
G11	$\overline{ENB}$	J11	S2	L11	—
H1	ZERO	K1	FTF		
H2	$\overline{G}$	K2	$\overline{OE}$		
H3	---	K3	F14		
H4	---	K4	F12		
H5	---	K5	F10		
H6	---	K6	F8		
H7	---	K7	F6		
H8	---	K8	F4		
H9	---	K9	F2		
H10	OSA	K10	C0		
H11	OSB	K11	S0		

FIGURE 1. Terminal connections - Continued.

Device types	01, 02, and 03	Device types	01, 02, and 03	Device types	01, 02, and 03
Case outline	Y	Case outline	Y	Case outline	Y
Terminal number	Terminal symbol	Terminal number	Terminal symbol	Terminal number	Terminal symbol
1	A0	24	OVF	47	S2
2	A1	25	$\overline{ENF}$	48	OSA
3	A2	26	FTF	49	OSB
4	A3	27	$\overline{OE}$	50	FTAB
5	A4	28	F15	51	$\overline{ENB}$
6	A5	29	F14	52	$\overline{ENA}$
7	A6	30	F13	53	B0
8	A7	31	F12	54	B1
9	A8	32	F11	55	B2
10	A9	33	F10	56	B3
11	A10	34	F9	57	B4
12	A11	35	F8	58	B5
13	A12	36	F7	59	B6
14	A13	37	F6	60	B7
15	A14	38	F5	61	B8
16	A15	39	F4	62	B9
17	CLK	40	F3	63	B10
18	V_{CC}	41	F2	64	B11
19	GND	42	F1	65	B12
20	C16	43	F0	66	B13
21	$\overline{P}$	44	C0	67	B14
22	$\overline{G}$	45	S0	68	B15
23	ZERO	46	S1		

FIGURE 1. Terminal connections - Continued.

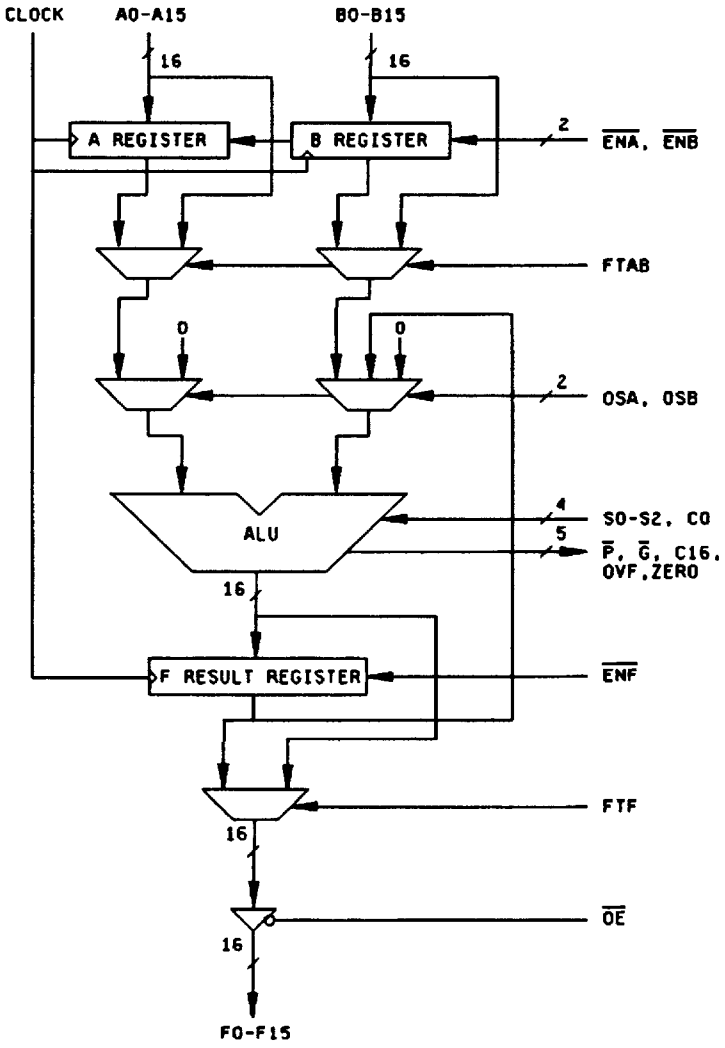


FIGURE 2. Functional block diagram.

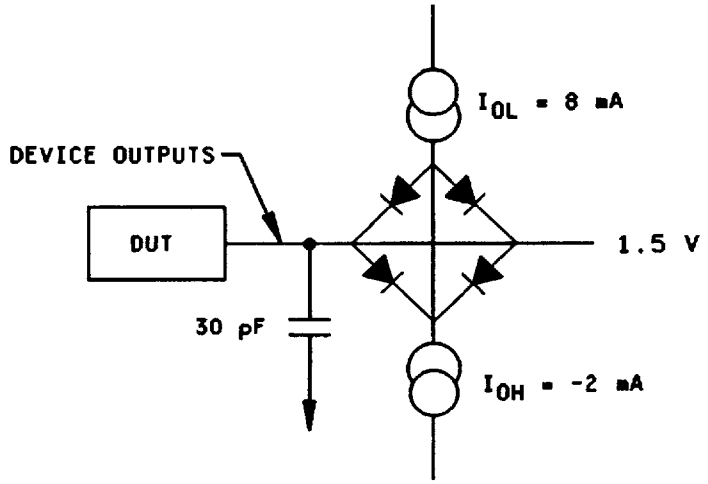
STANDARDIZED MILITARY DRAWING DEFENSE ELECTRONICS SUPPLY CENTER DAYTON, OHIO 45444	SIZE A		5962-89959
		REVISION LEVEL B	SHEET 15

ALU functions			
S2	S1	S0	Functions
0	0	0	Clear (F = 00 ... 0)
0	0	1	Not (A) + B
0	1	0	A + Not (B)
0	1	1	A + B
1	0	0	A Xor B
1	0	1	A or B
1	1	0	A and B
1	1	1	Preset (F = 11 ... 1)

Operand selection control			
OSB	OSA	Operand B	Operand A
0	0	F	A
0	1	0	A
1	0	B	0
1	1	B	A

F = F result register
0 = Operand force to zero

FIGURE 3. Truth tables.



TEST CIRCUIT

NOTE: 30 pF including scope probe and test socket.

FIGURE 4. Switching waveforms and test circuit.

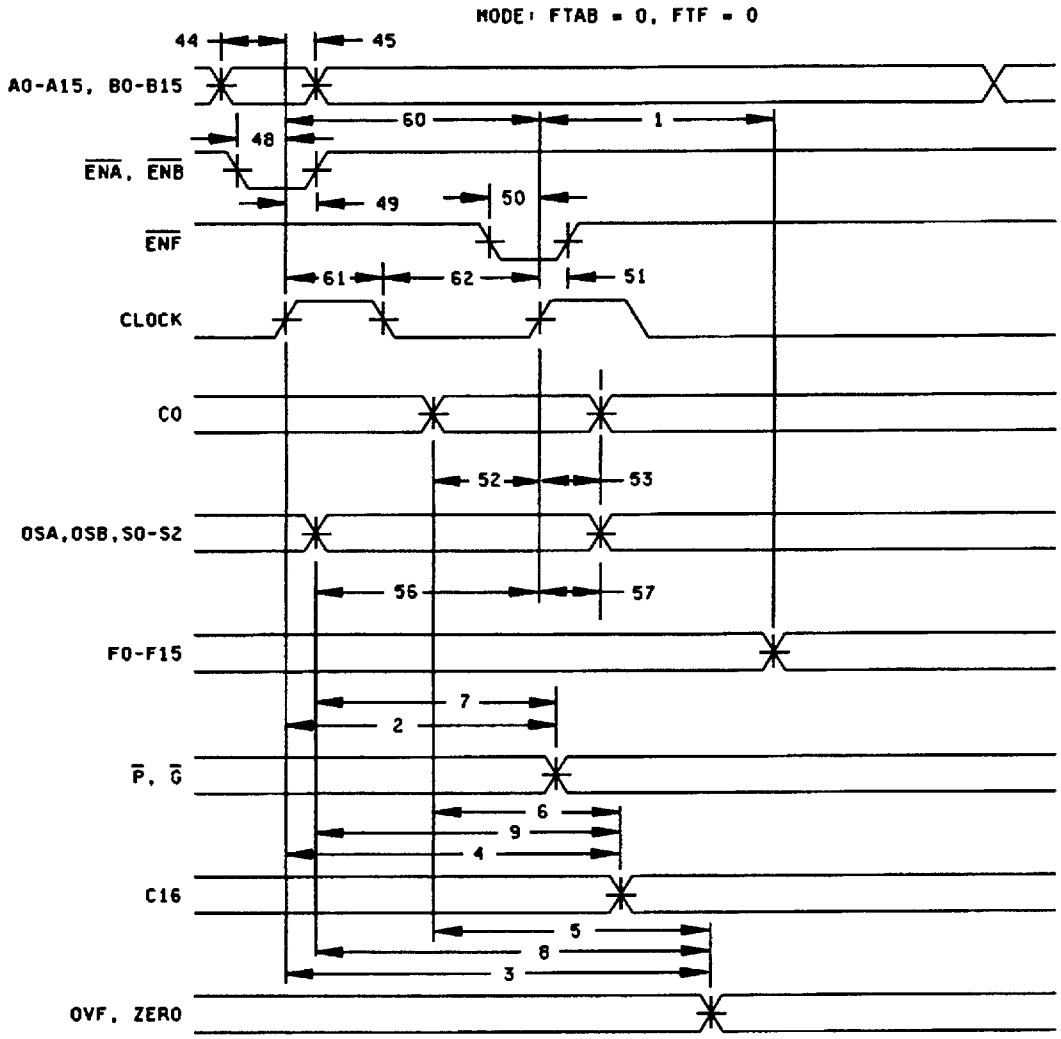


FIGURE 4. Switching waveforms and test circuit - Continued.

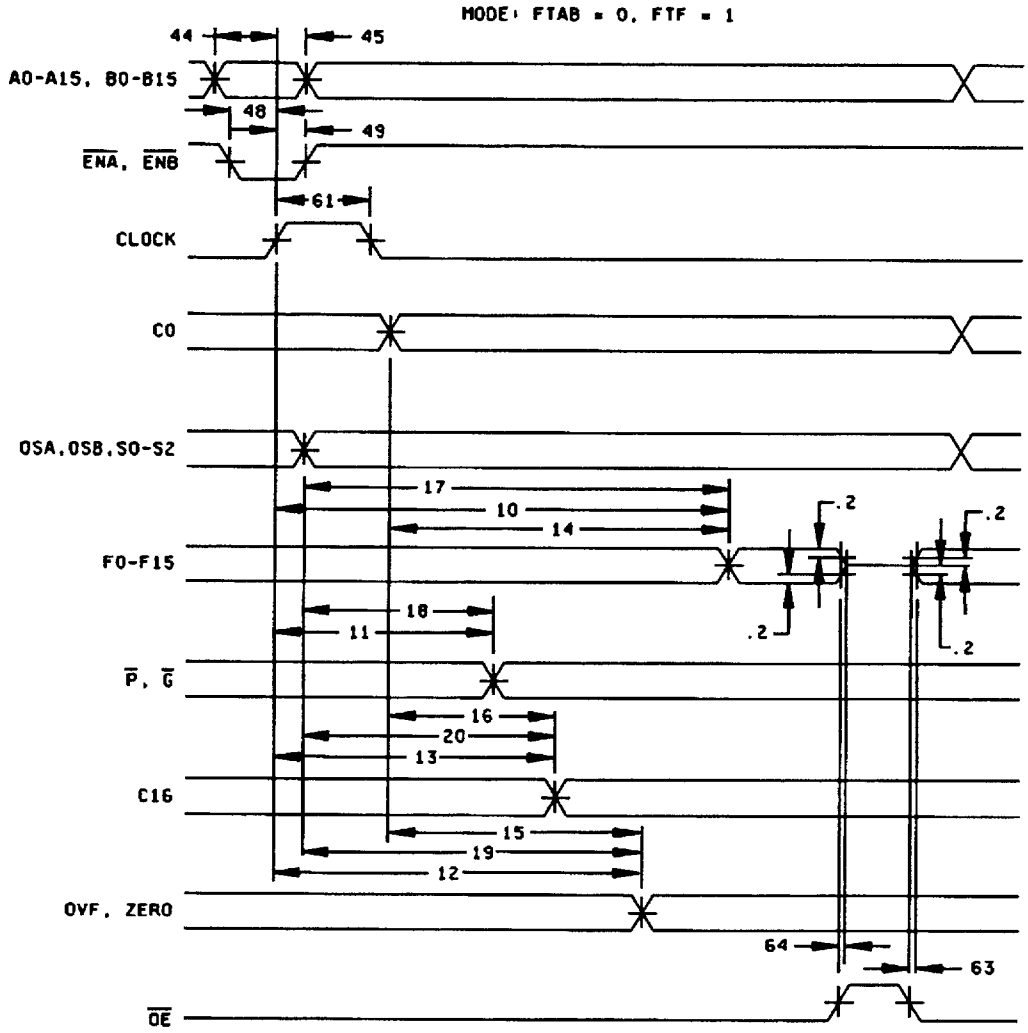


FIGURE 4. Switching waveforms and test circuit - Continued.

STANDARDIZED MILITARY DRAWING DEFENSE ELECTRONICS SUPPLY CENTER DAYTON, OHIO 45444	SIZE A		5962-89959
		REVISION LEVEL B	SHEET 19

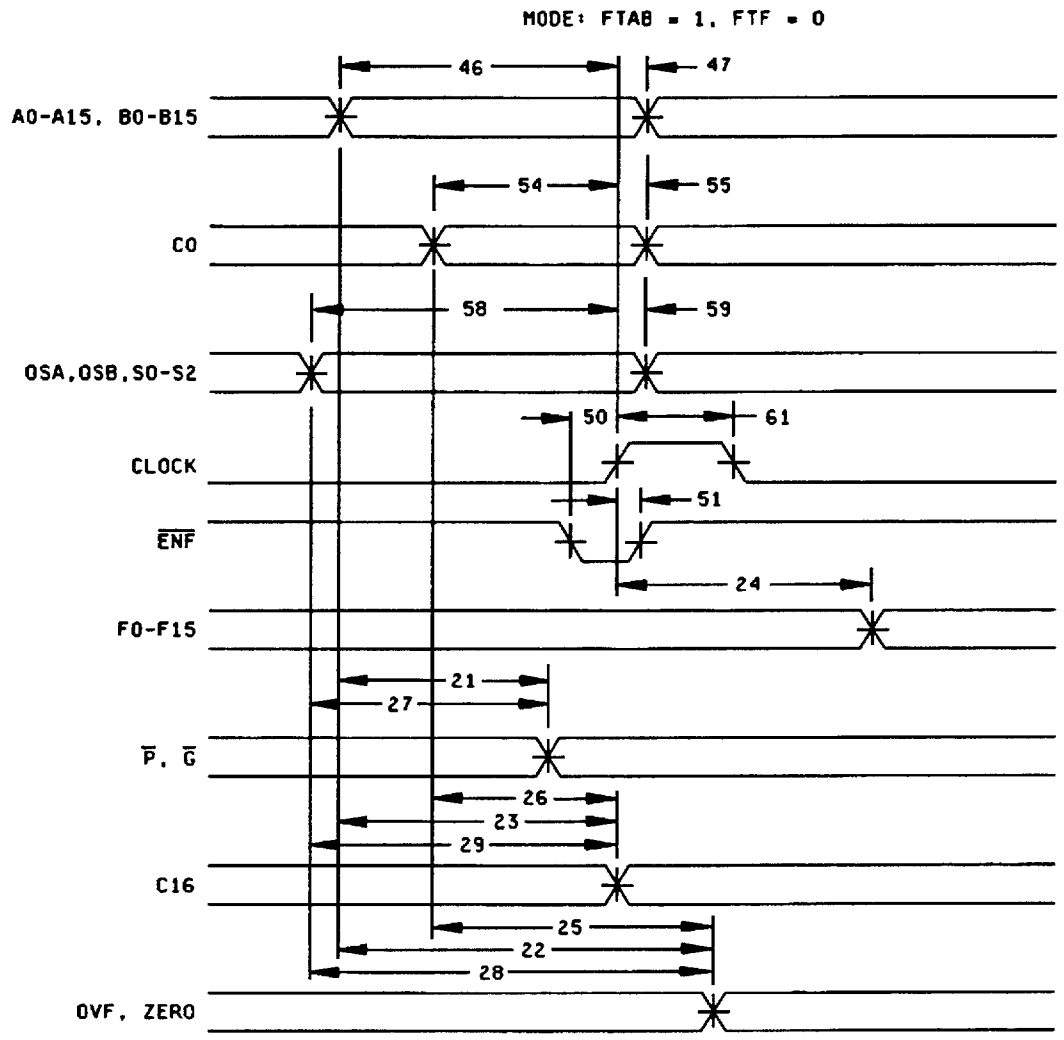


FIGURE 4. Switching waveforms and test circuit - Continued.

STANDARDIZED MILITARY DRAWING DEFENSE ELECTRONICS SUPPLY CENTER DAYTON, OHIO 45444	SIZE A		5962-89959
		REVISION LEVEL B	SHEET 20

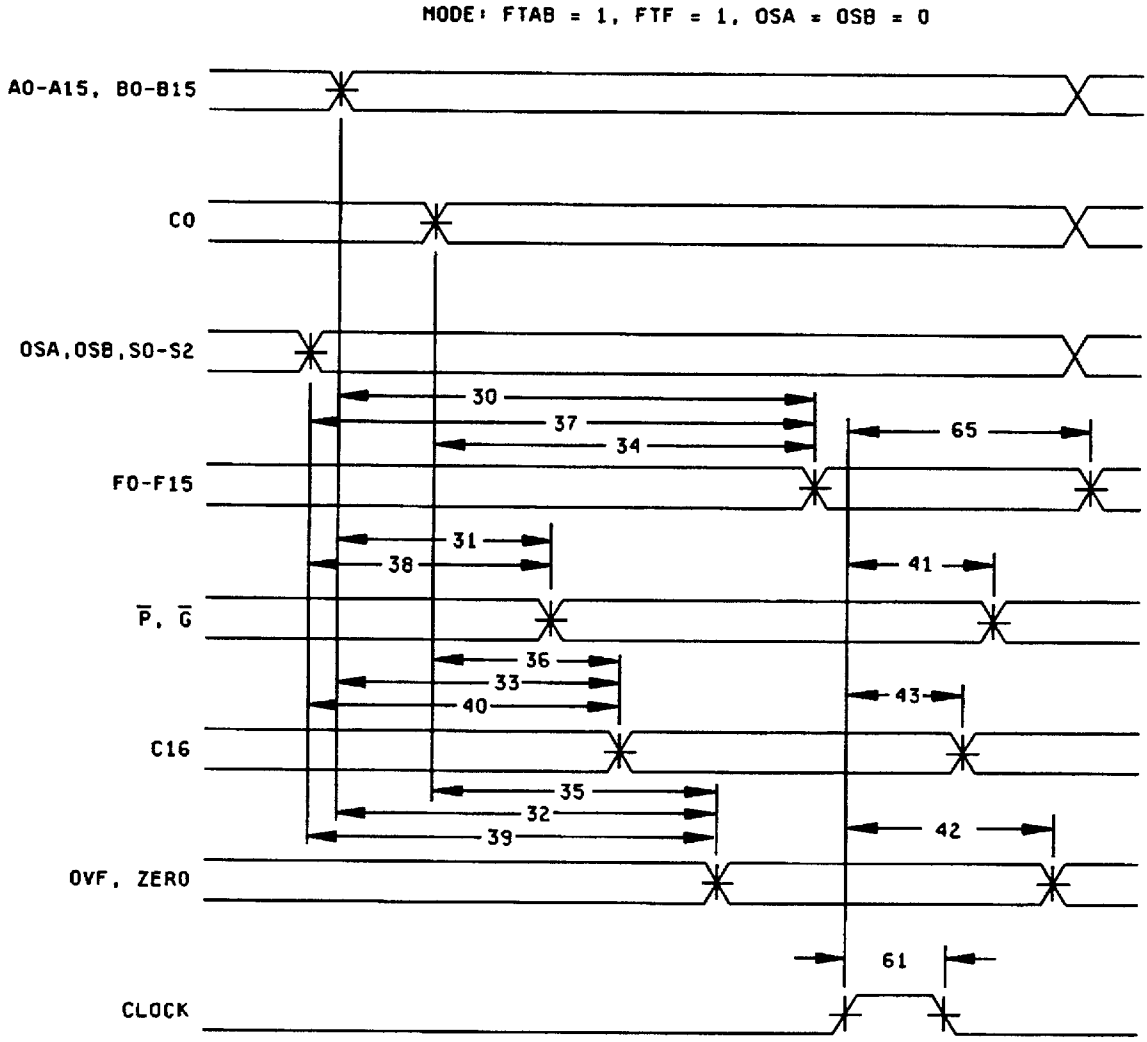


FIGURE 4. Switching waveforms and test circuit - Continued.

STANDARDIZED MILITARY DRAWING DEFENSE ELECTRONICS SUPPLY CENTER DAYTON, OHIO 45444	SIZE A		5962-89959
		REVISION LEVEL B	SHEET 21

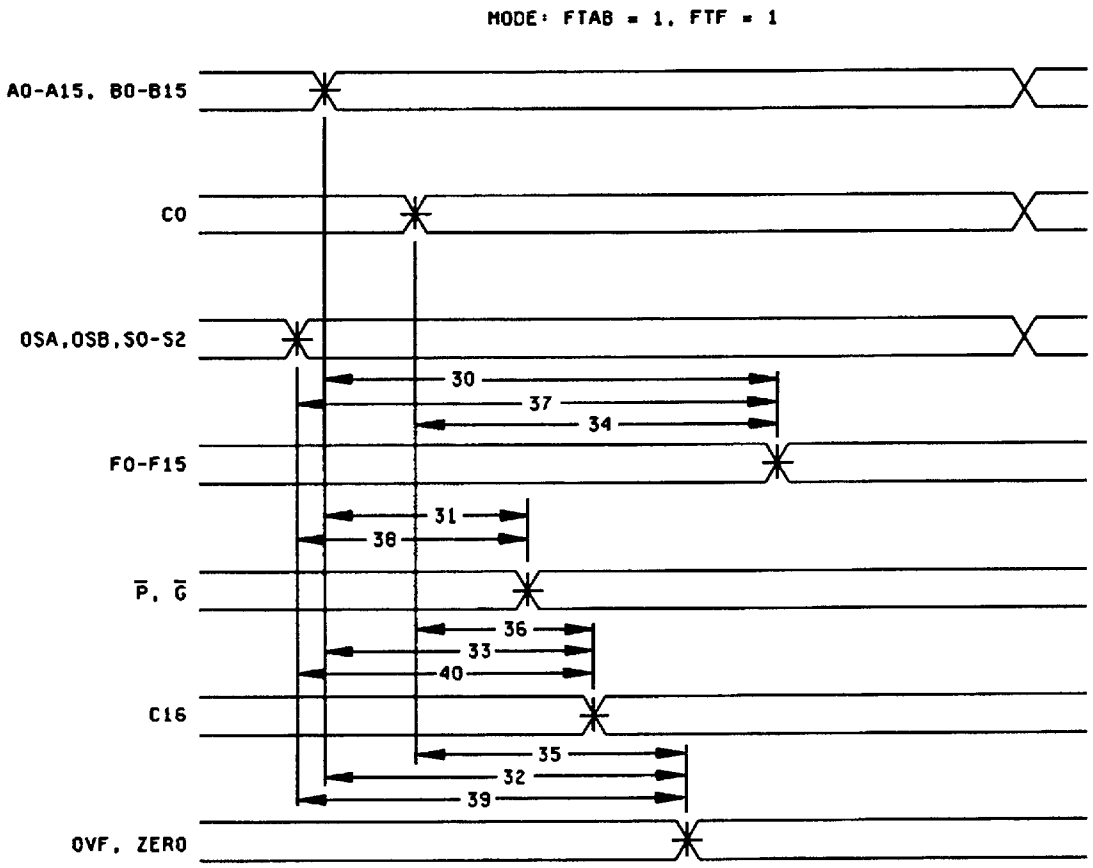


FIGURE 4. Switching waveforms and test circuit - Continued.

TABLE II. Electrical test requirements.

MIL-STD-883 test requirements	Subgroups (in accordance with method 5005, table I)
Interim electrical parameters (method 5004)	---
Final electrical test parameters (method 5004)	1*, 2, 3, 7, 8, 9, 10, 11
Group A test requirements (method 5005)	1, 2, 3, 4, 7, 8, 9, 10, 11
Groups C and D end-point electrical parameters (method 5005)	2, 8A, 10

* PDA applies to subgroup 1.

4.3 Quality conformance inspection. Quality conformance inspection shall be in accordance with method 5005 of MIL-STD-883 including groups A, B, C, and D inspections. The following additional criteria shall apply.

4.3.1 Group A inspection.

a. Tests shall be as specified in table II herein.

b. Subgroups 5 and 6 in table I, method 5005 of MIL-STD-883 shall be omitted.

c. Subgroup 4 (C_{IN} measurement) shall be measured only for the initial test and after process or design changes which may affect input capacitance.

d. Subgroups 7 and 8 shall include verification of the truth table.

4.3.2 Groups C and D inspections.

a. End-point electrical parameters shall be as specified in table II herein.

b. Steady-state life test conditions, method 1005 of MIL-STD-883.

(1) Test condition B. The test circuit shall be maintained by the manufacturer under document revision level control and shall be made available to the preparing or acquiring activity upon request. The test circuit shall specify the inputs, outputs, biases, and power dissipation, as applicable, in accordance with the intent specified in test method 1005 of MIL-STD-883.

(2) T_A = +125°C, minimum.

(3) Test duration: 1,000 hours, except as permitted by method 1005 of MIL-STD-883.

5. PACKAGING

5.1 Packaging requirements. The requirements for packaging shall be in accordance with MIL-STD-883 (see 3.1 herein).

6. NOTES

6.1 Intended use. Microcircuits conforming to this drawing are intended for use for Government microcircuit applications (original equipment), design applications, and logistics purposes.

6.2 Replaceability. Microcircuits covered by this drawing will replace the same generic device covered by a contractor-prepared specification or drawing.

6.3 Configuration control of SMD's. All proposed changes to existing SMD's will be coordinated with the users of record for the individual documents. This coordination will be accomplished in accordance with MIL-STD-973 using DD Form 1692, Engineering Change Proposal .

6.4 Record of users. Military and industrial users shall inform Defense Electronics Supply Center when a system application requires configuration control and the applicable SMD. DESC will maintain a record of users and this list will be used for coordination and distribution of changes to the drawings. Users of drawings covering microelectronics devices (FSC 5962) should contact DESC-EC, telephone (513) 296-6047.

6.5 Comments. Comments on this drawing should be directed to DESC-EC, Dayton, Ohio 45444-5270, or telephone (513) 296-5377.

6.6 Pin functions. Microcircuits conforming to this drawing shall have pin functions as specified below.

Pin name	Functions
A0-A15	"A" data input bus. The 16-bit "A" input data bus to the ALU.
B0-B15	"B" data input bus. The 16-bit "B" input data bus to the ALU.
F0-F15	"F" data output bus. The 16-bit "F" output data bus from the ALU.
CO	Carry input. This input is used in arithmetic operations.
C16	Carry out. Output flag that provides the carry information from an arithmetic operation.
$\overline{P}$	Carry propagate output. Output flag that provides the propagate information from an arithmetic operation. Used in cascaded systems.
$\overline{G}$	Carry generate output. Output flag that provides the carry generate information from an arithmetic operation. Used in cascaded systems.
OVF	Overflow output. Output flag that provides ALU result overflow information from an arithmetic operation.
ZERO	Zero output. Output flag that provides ALU result overflow information from an arithmetic operation.
$\overline{ENA}$	"A" register enable input. Control input used to either load or hold data into the "A" register.
$\overline{ENB}$	"B" register enable input. Control input used to either load or hold data into the "B" register.
FTAB	Feedthrough "AB" input. Control input used to select whether the input registers are bypassed or not.
$\overline{ENF}$	"F" register enable output. Control input used to either load or hold data into the "F" register.
FTF	Feedthrough "F" input. Control input used to select whether the output register is bypassed or not.
OSA, OSB	Operand select inputs. Selects input data to the ALU on the "A" and "B" ports.
S0-S2	Instruction select inputs. Controls which operation the ALU will perform.
$\overline{OE}$	Output enable input. Controls the "F" output bus by enabling and disabling the outputs.
CLK	Clock input. The master clock input for all device registers.
V_{CC}, GND	Power supply.

6.7 Approved sources of supply. Approved sources of supply are listed in MIL-BUL-103. The vendors listed in MIL-BUL-103 have agreed to this drawing and a certificate of compliance (see 3.6 herein) has been submitted to and accepted by DESC-EC.