REVISIONS

LTR	DESCRIPTION	DATE (YR-MO-DA)	APPROVED
A	Changes in accordance with NOR 5962-R060-92	91-11-25	M. L. Poelking
B	Changes in accordance with NOR 5962-R006-93	92-11-05	M. L. Poelking
C	Add device type 03. Update boilerplate. Editorial changes throughout.	92-12-10	M. L. Poelking
D	Add device type 04. Update boilerplate. Editorial changes throughout.	96-07-09	M. L. Poelking
E	Add case outlines T and M. Changes to boilerplate. Editorial changes throughout.	96-10-03	M. L. Poelking
F	Changes in accordance with NOR 5962-R296-97.	97-06-06	M. L. Poelking
G	Add device type 05. Editorial changes throughout.- LTG	97-12-01	M. L. Poelking

REV	G	G	G	G	G	G	G	G	G	G	G	G	G	G	G	G	G			
SHEET	35	36	37	38	39	40	41	42	43	44	45	46	47	48	49	50	51			
REV	G	G	G	G	G	G	G	G	G	G	G	G	G	G	G	G	G	G	G	G
SHEET	15	16	17	18	19	20	21	22	23	24	25	26	27	28	29	30	31	32	33	34

REV STATUS OF SHEETS	REV	G	G	G	G	G	G	G	G	G	G	G	G	G	G	G
	SHEET	1	2	3	4	5	6	7	8	9	10	11	12	13	14	

PMIC N/A

STANDARD MICROCIRCUIT DRAWING

THIS DRAWING IS AVAILABLE FOR USE BY ALL DEPARTMENTS AND AGENCIES OF THE DEPARTMENT OF DEFENSE

AMSC N/A

PREPARED BY
Christopher A. Rauch

CHECKED BY
Tim H. Noh

APPROVED BY
Don M. Cool

DRAWING APPROVAL DATE
91-09-13

REVISION LEVEL
G

DEFENSE SUPPLY CENTER COLUMBUS
COLUMBUS, OHIO 43216

MICROCIRCUIT, DIGITAL, CMOS, DIGITAL SIGNAL PROCESSOR, MONOLITHIC SILICON

SIZE	CAGE CODE	
A	67268	5962-90526

SHEET 1 OF 51

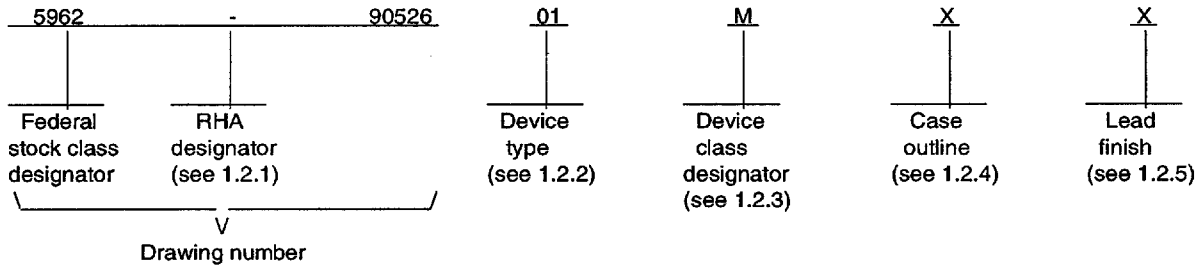
DSCC FORM 2233
APR 97

5962-E054-98

1. SCOPE

1.1 Scope. This drawing documents two product assurance class levels consisting of high reliability (device classes Q and M) and Appendix F of MIL-PRF-38535, "General provisions for TAB microcircuits" and space application (device class V). A choice of case outlines and lead finishes are available and are reflected in the Part or Identifying Number (PIN). When available, a choice of Radiation Hardness Assurance (RHA) levels are reflected in the PIN.

1.2 PIN. The PIN is as shown in the following example:



1.2.1 RHA designator. Device classes Q and V RHA marked devices meet the MIL-PRF-38535 specified RHA levels and are marked with the appropriate RHA designator. Device class M RHA marked devices meet the MIL-PRF-38535, appendix A specified RHA levels and are marked with the appropriate RHA designator. A dash (-) indicates a non-RHA device.

1.2.2 Device type(s). The device type(s) identify the circuit function as follows:

Device type	Generic number	Circuit function
01	320C30	Digital signal processor, 28 MHz
02	320C30	Digital signal processor, 25 MHz
03	320C30	Digital signal processor, 33 MHz
04	320C30	Digital signal processor, 40 MHz
05	320C30	Digital signal processor, 50 MHz

1.2.3 Device class designator. The device class designator is a single letter identifying the product assurance level as follows:

Device class	Device requirements documentation
M	Vendor self-certification to the requirements for MIL-STD-883 compliant, non-JAN class level B microcircuits in accordance with MIL-PRF-38535, appendix A and Appendix F of MIL-PRF-38535.
Q or V	Certification and qualification to MIL-PRF-38535 and Appendix F of MIL-PRF-38535.

1.2.4 Case outline(s). The case outline(s) are as designated in MIL-STD-1835 and as follows:

Outline letter	Descriptive designator	Terminals	Package style
U	See figure 1	196	Quad flat package with non-conductive tiebar
X	CMGA7-P181	181	Pin grid array
Y 1/	See figure 1	196	Leadless chip carrier
Z 1/	See figure 1	196	Quad flat package
T	See figure 1	203	Environmentally protected tape automated bond
M	See figure 1	196	Tape automated bond

1/ Not available from an approved source of supply.

1.2.5 Lead finish. The lead finish is as specified in MIL-PRF-38535 and Appendix Fof MIL-PRF-38535, for device classes Q and V or MIL-PRF-38535, appendix A and Appendix F of MIL-PRF-38535 for device class M.

1.3 Absolute maximum ratings. 2/

Supply voltage range (V_{DD}) 3/	-0.3 V dc to 7.0 V dc
Input voltage range	-0.3 V dc to 7.0 V dc
Output voltage range	-0.3 V dc to 7.0 V dc
Continuous power dissipation 4/	3.15 W
Storage temperature range	-55° C to +150° C
Thermal resistance, junction to case (Θ_{JC}):	
Case X	See MIL-STD-1835.
Case U	1.5° C/W
Maximum die temperature rise for the die at 100%	
Cases T and M	0.09° C/W
Thermal resistance, junction to ambient (Θ_{JA}):	
Case U	29° C/W

1.4 Recommended operating conditions.

Supply voltages (V_{DD}):	
Device type 01, 04 and 05	4.75 V dc min to 5.25 V dc max
Device type 02 and 03	4.5 V dc min to 5.5 V dc max
Supply voltages (CVSS, etc.)(V_{SS})	0 V dc nominal
High level input voltage (V_{IH}) 5/	2.1 V dc min to V_{DD} +0.3 V dc max
Low level input voltage (V_{IL}) 5/	-0.3 V dc min to 0.8 V dc max
High level output current (I_{OH})	-300 µA max
Low level output current (I_{OL})	2 mA max
CLKIN high level input voltage (V_{TH}) 5/	3.0 V dc Min to V_{DD} +0.3 V dc max
Operating case temperature (T_C)	-55° C min to +125° C max

1.5 Digital logic testing for device classes Q and V.

Fault coverage measurement of manufacturing logic tests (MIL-STD-883, test method 5012)	XX percent 6/

2. APPLICABLE DOCUMENTS

2.1 Government specification, standards, and handbooks. The following specification, standards, and handbooks form a part of this drawing to the extent specified herein. Unless otherwise specified, the issues of these documents are those listed in the issue of the Department of Defense Index of Specifications and Standards (DoDISS) and supplement thereto, cited in the solicitation.

SPECIFICATION

MILITARY

MIL-PRF-38535 - Integrated Circuits, Manufacturing, General Specification for.

2/ Stresses above the absolute maximum rating may cause permanent damage to the device. Extended operation at the maximum levels may degrade performance and affect reliability.
3/ All voltage values are with respect to V_{SS}.
4/ Actual operating power will be less. This value was obtained under specially produced worst-case test conditions, which are not sustained during normal device operation. These conditions consist of continous parallel writes of a checkerboard pattern to both primary and expansion buses at the maximum rate possible.
5/ V_{IH} max, V_{IL} min, and V_{TH} max are guaranteed from characterization but not tested.
6/ Values will be added when they become available.

STANDARDS

MILITARY

MIL-STD-883 - Test Methods and Procedures for Microelectronics.
MIL-STD-973 - Configuration Management.
MIL-STD-1835 - Microcircuit Case Outlines.

HANDBOOKS

MILITARY

MIL-HDBK-103 - List of Standard Microcircuit Drawings (SMD's).
MIL-HDBK-780 - Standard Microcircuit Drawings.

(Unless otherwise indicated, copies of the specification, standards, and handbooks are available from the Standardization Document Order Desk, 700 Robbins Avenue, Building 4D, Philadelphia, PA 19111-5094.)

2.2 Order of precedence. In the event of a conflict between the text of this drawing and the references cited herein, the text of this drawing takes precedence. Nothing in this document, however, supersedes applicable laws and regulations unless a specific exemption has been obtained.

3. REQUIREMENTS

3.1 Item requirements. The individual item requirements for device classes Q and V shall be in accordance with MIL-PRF-38535, and Appendix Fof MIL-PRF-38535 "General provisions for TAB microcircuits", and as specified herein or as modified in the device manufacturer's Quality Management (QM) plan. The modification in the QM plan shall not affect the form, fit, or function as described herein. The individual item requirements for device class M shall be in accordance with MIL-PRF-38535, appendix A for non-JAN class level B devices and as specified herein.

3.2 Design, construction, and physical dimensions. The design, construction, and physical dimensions shall be as specified in MIL-PRF-38535, Appendix Fof MIL-PRF-38535 and herein for device classes Q and V or MIL-PRF-38535, appendix A, Appendix F of MIL-PRF-38535 and herein for device class M.

3.2.1 Case outline(s). The case outline(s) shall be in accordance with 1.2.4 herein and figure 1.

3.2.2 Terminal connections. The terminal connections shall be as specified on figure 2.

3.2.3 Functional block diagram. The functional block diagram shall be as specified on figure 3.

3.2.4 Switching waveforms and test circuit. The switching waveforms and test circuit shall be as specified on figure 4.

3.3 Electrical performance characteristics and postirradiation parameter limits. Unless otherwise specified herein, the electrical performance characteristics and postirradiation parameter limits are as specified in table I and shall apply over the full case operating temperature range.

3.4 Electrical test requirements. The electrical test requirements shall be the subgroups specified in table II. The electrical tests for each subgroup are defined in table I.

3.5 Marking. The part shall be marked with the PIN listed in 1.2 herein. In addition, the manufacturer's PIN may also be marked as listed in MIL-HDBK-103. For packages where marking of the entire SMD PIN number is not feasible due to space limitations, the manufacturer has the option of not marking the "5962-" on the device. For RHA product using this option, the RHA designator shall still be marked. Marking for device classes Q and V shall be in accordance with MIL-PRF-38535 and Appendix F of MIL-PRF-38535 (see 3.1 herein). Marking for device class M shall be in accordance with MIL-PRF-38535, appendix A and Appendix F of MIL-PRF-38535.

3.5.1 Certification/compliance mark. The certification mark for device classes Q and V shall be a "QML" or "Q" as required in MIL-PRF-38535. The compliance mark for device class M shall be a "C" as required in MIL-PRF-38535, appendix A.

3.6 Certificate of compliance. For device classes Q and V, a certificate of compliance shall be required from a QML-38535 listed manufacturer in order to supply to the requirements of this drawing (see 6.6.1 herein). For device class M, a certificate of compliance shall be required from a manufacturer in order to be listed as an approved source of supply in MIL-HDBK-103 (see 6.6.2 herein). The certificate of compliance submitted to DSCC-VA prior to listing as an approved source of supply for this drawing shall affirm that the manufacturer's product meets, for device classes Q and V, the requirements of MIL-PRF-38535, Appendix F of MIL-PRF-38535 (see 3.1 herein) and herein or for device class M, the requirements of MIL-PRF-38535, appendix A, Appendix F of MIL-PRF-38535 and herein.

3.7 Certificate of conformance. A certificate of conformance as required for device classes Q and V in MIL-PRF-38535 or for device class M in MIL-PRF-38535, appendix A shall be provided with each lot of microcircuits delivered to this drawing.

3.8 Notification of change for device class M. For device class M, notification to DSCC-VA of change of product (see 6.2 herein) involving devices acquired to this drawing is required for any change as defined in MIL-STD-973.

3.9 Verification and review for device class M. For device class M, DSCC, DSCC's agent, and the acquiring activity retain the option to review the manufacturer's facility and applicable required documentation. Offshore documentation shall be made available onshore at the option of the reviewer.

3.10 Microcircuit group assignment for device class M. Device class M devices covered by this drawing shall be in microcircuit group number 105 (see MIL-PRF-38535, appendix A).

3.11 ROM coding processing option. If ROM coding is to be utilized by the user, an altered item drawing (AID) must be supplied to the vendor. It is recommended that users insure the vendor perform subgroups 7 and 9 after programming to verify the specific program configuration.

TABLE I. Electrical performance characteristics.

Test	Symbol	Conditions $-55°C \le T_C \le +125°C$ 1/ unless otherwise specified	Group A subgroups	Device type	Limits		Unit
					Min	Max	
High level output voltage	V_{OH}	V_{DD} = minimum I_{OH} = -300 µA	1,2,3	All	2.4		V
Low level output voltage 2/	V_{OL}	V_{DD} = minimum I_{OL} = 2 mA				0.6	
Three-state current	I_Z	V_{DD} = maximum			-20	20	µA
Input current	I_I	V_I = 0.0 V to V_{DD} maximum			-10	10	
Input current with internal pull-ups 3/	I_{IP}				-400	20	
Input current, (X2/CLKIN)	I_{IC}	V_I = 0.0 V to 5.5 V			-50	50	
Supply current 4/	I_{CC}	V_{DD} = maximum, f_x = 28 MHz	1	01		600	mA
		f_x = 25 MHz		02		600	
		f_x = 33 MHz		03		600	
		f_x = 40 Mhz		04		600	
		f_x = 50 Mhz		05		600	
Input capacitance 5/	C_{IN}	See 4.4.1b	4	All		15	pF
Output capacitance 5/	C_{OUT}					20	
X2/CLKIN capacitance 5/	C_X					25	

See footnotes at end of table.

TABLE I. Electrical performance characteristics - Continued.

Test	Symbol	Conditions $-55°C \le T_C \le +125°C$ 1/ unless otherwise specified		Group A subgroups	Device type	Limits		Unit
						Min	Max	
Functional testing		See 4.4.1d		7,8	All			
Fall time, CLKIN 5/	t_{F1}	See figure 4 X2/CLKIN timing		9,10,11	All		5	ns
Pulse duration, CLKIN low	t_{W1}		t_{C1} = 35 ns		01	12.5		
			t_{C1} = 40 ns		02	14		
			t_{C1} = 30 ns		03	10.5		
			t_{C1} = 25 ns		04	9		
			t_{c1} = 20 ns		05	7		
Pulse duration, CLKIN high	t_{W2}		t_{C1} = 35 ns		01	12.5		
			t_{C1} = 40 ns		02	14		
			t_{C1} = 30 ns		03	10.5		
			t_{C1} = 25 ns		04	9		
			t_{c1} = 20 ns		05	7		
Rise time, CLKIN 5/	t_{R1}				All		5	
Cycle time, CLKIN	t_{C1}				01	35	303	
					02	40	303	
					03	30	303	
					04	25	303	
					05	20	303	
Fall time, H1/H3	t_{F2}	See figure 4 H1/H3 timing			01,03 04,05		3	
					02		4	
Pulse duration, H1/H3 low	t_{W3}		P = t_{C1}		01-03	P-6		
					04,05	P-5		
Pulse duration, H1/H3 high	t_{W4}				01-03	P-7		
					04,05	P-6		
Rise time, H1/H3	t_{R2}				01-03		4	
					04,05		3	
Delay time, from H1(H3) low to H3(H1) high 6/	t_{D1}				01-03	0	5	
					04,05	0	4	
Cycle time, H1/H3	t_{C2}				01	70	606	
					02	80	606	
					03	60	606	
					04	50	606	
					05	40	606	

See footnotes at end of table.

TABLE I. Electrical performance characteristics - Continued.

Test	Symbol	Conditions $-55°C \le T_C \le +125°C$ 1/ unless otherwise specified	Group A subgroups	Device type	Limits Min	Limits Max	Unit
Delay time, from H1 low to (M)STRB low 6/	t_{D2}	See figure 4 Memory ((M)STRB = 0)	9,10,11	01-04	0	10	ns
				05	0	4	
Delay time, from H1 low to (M) STRB high 6/	t_{D3}			01-03	0	10	
				04	0	6	
				05	0	4	
Delay time, from H1 high to R/W low 6/	t_{D4}		9,10,11	01-03	0	10	
				04	0	9	
				05	0	7	
Delay time, from H1 high to (X)R/W low 6/	t_{D5}			01	0	17	
				02	0	18	
				03	0	15	
				04	0	13	
				05	0	11	
Delay time, from H1 low to A valid 6/	t_{D6}			01	0	16	
				02	0	18	
				03,04	0	14	
				05	0	9	
Delay time, from H1 low to XA valid 6/	t_{D7}			01	0	13	
				02	0	15	
				03	0	10	
				04	0	9	
				05	0	8	
Setup time, D valid before H1 low (read)	t_{SU1}			01,02	19		
				03	16		
				04	14		
				05	10		
Setup time, XD before H1 low (read)	t_{SU2}			01,02	20		
				03	18		
				04	16		
				05	14		
Hold time, (X)D after H1 low (read) 6/	t_{H1}			All	0		
Setup time, RDY before H1 high	t_{SU3}			01,02	10		
				03,04	8		
				05	6		
Setup time, XRDY before H1 high	t_{SU4}			01	10		
				02	12		
				03,04	9		
				05	8		
Hold time, XRDY after H1 high	t_{H2}			All	0		

See footnotes at end of table.

TABLE I. Electrical performance characteristics - Continued.

Test	Symbol	Conditions $-55°C \le T_C \le +125°C$ 1/ unless otherwise specified	Group A subgroups	Device type	Limits		Unit
					Min	Max	
Delay time, from H1 high to (X)R/W high (write)	t_{D8}	See figure 4 Memory ((M)STRB = 0)	9,10,11	01,02 03 04 05		12 10 9 7	ns
(X)D valid after H1 low (write)	t_{V1}			01-03 04 05		20 17 14	
Hold time, X(D) after H1 high (write) 6/	t_{H3}			All	0		
Delay time, from H1 high to A valid on back-to-back write cycles	t_{D9}			01,02 03 04 05		22 18 15 12	
Delay time, from H1 high to XA valid on back-to-back write cycles	t_{D10}			01,02 03 04 05		32 25 21 18	
Delay time, from (X)RDY to A valid 5/	t_{D11}			01-03 04 05		8 7 6	
Delay time, from H1 high to IOSTRB low 6/	t_{D12}	See figure 4 Memory ((IO)STRB = 0)	9,10,11	01,02 03 04 05	0 0 0 0	11 10 9 8	ns
Delay time, from H1 high to IOSTRB high 6/	t_{D13}			01-03 04 05	0 0 0	10 9 8	
Delay time, from H1 low to XR/W high 6/	t_{D14}			01 02 03 04 05	0 0 0 0 0	11 13 10 9 8	
Delay time, from H1 low to XA valid 6/	t_{D15}			01 02 03 04 05	0 0 0 0 0	12 14 10 9 8	

See footnotes at end of table.

TABLE I. Electrical performance characteristics - Continued.

Test	Symbol	Conditions $-55°C \le T_C \le +125°C$ 1/ unless otherwise specified	Group A subgroups	Device type	Limits		Unit
					Min	Max	
Setup time, XD before H1 high	t_{SU5}	See figure 4 Memory ((IO)STRB = 0)	9,10,11	01-03 04 05	15 13 11		ns
Hold time, XD after H1 high 6/	t_{H4}			All	0		
Setup time, XRDY before H1 high	t_{SU6}			01 02 03,04 05	10 12 9 8		
Hold time, XRDY after H1 high	t_{H5}			All	0		
Delay time, from H1 low to (X)R/W low 6/	t_{D16}			01-03 04 05	0 0 0	15 13 11	
XD valid after H1 high	t_{V2}			01-03 04 05		30 25 20	
Hold time, XD after H1 low	t_{H6}			All	0		
Delay time, from H3 high to XF0 low	t_{D17}	See figure 4 Timing for XF0 and XF1 when executing LDFI or LDII		01-03 04 05		15 13 12	
Setup time, XF1 valid before H1 low	t_{SU7}			01,02 03 04,05	15 12 9		
Hold time, XF1 after H1 low	t_{H7}			All	0		

See footnotes at end of table.

TABLE I. Electrical performance characteristics - Continued.

Test	Symbol	Conditions $-55°C \le T_C \le +125°C$ 1/ unless otherwise specified	Group A subgroups	Device type	Limits		Unit
					Min	Max	
Delay time, from H3 high to XF0 high	t_{D18}	See figure 4 Timing for XF0 when executing a STFI or STII	9,10,11	01,02 03 04 05		20 18 13 12	ns
Delay time, from H3 high to XF0 low	t_{D19}	See figure 4 Timing for XF0 and XF1 when executing a SIGI	9,10,11	01-03 04 05		15 13 12	ns
Delay time, from H3 high to XF0 high	t_{D20}			01,02 03 04 05		20 18 13 12	
Setup time, XF1 valid before H1 low	t_{SU8}			01-03 04,05	12 9		
Hold time, XF1 after H1 low	t_{H8}			All	0		
XF valid after H3 high	t_{V3}	See figure 4 Timing for loading XF register when conformed as an output pin		01,02 03 04 05		20 15 13 12	
Hold time, XF after H3 high 5/	t_{H9}	See figure 4 Change of XF from output to input mode		01,02 03 04 05		20 15 13 12	
Setup time, XF before H1 low	t_{SU9}			01-03 04,05	12 9		
Hold time, XF after H1 low	t_{H10}			All	0		
Delay time, from H3 high to XF switching from input to output	t_{D21}	See figure 4 Change of XF from input to output mode		01-03 04,05		20 17	

See footnotes at end of table.

TABLE I. Electrical performance characteristics - Continued.

Test	Symbol	Conditions $-55°C \le T_C \le +125°C$ 1/ unless otherwise specified	Group A subgroups	Device type	Limits		Unit
					Min	Max	
Setup time, for RESET before CLKIN low 5/	t_{SU10}	See figure 4 RESET timing	9,10,11	All	10	t_c (C1)	ns
Delay time, from CLKIN high to H1 high	t_{D22}			01,02	3	18	
				03,04	2	14	
				05	2	10	
Delay time, from CLKIN high to H1 low	t_{D23}			01,02	3	18	
				03,04	2	14	
				05	2	10	
Setup time, $\overline{RESET}$ high before H1 low and after 10 H1 clock cycles 6/	t_{SU11}			01,02	15		
				03	10		
				04	9		
				05	7		
Delay time, from CLKIN high to H3 low	t_{D24}			01,02	3	18	
				03,04	2	14	
				05	2	10	
Delay time, from CLKIN high to H3 high	t_{D25}			01,02	3	18	
				03-04	2	14	
				05	2	10	
Disable time, from H1 high to (X)D three-state 5/	t_{DIS1}			01,02		20	
				03		18	
				04		15	
				05		12	
Disable time, from H3 high to (X)A three-state 5/	t_{DIS2}			01,02		12	
				03		10	
				04		9	
				05		8	

See footnotes at end of table.

TABLE I. Electrical performance characteristics - Continued.

Test	Symbol	Conditions $-55°C \le T_C \le +125°C$ 1/ unless otherwise specified	Group A subgroups	Device type	Limits		Unit
					Min	Max	
Delay time, from H3 high to control signals high 5/	t_{D26}	See figure 4 RESET TIMING	9, 10, 11	01-03		10	ns
				04		9	
				05		8	
Delay time, from H1 high to IACK high 5/	t_{D27}			01,02		12	
				03		10	
				04		9	
				05		8	
Disable time, from RESET low to asynchronously reset signals 5/	t_{DIS3}			01-03		25	
				04		21	
				05		17	
Setup time, INT(3-0) before H1 low	t_{SU12}	See figure 4 INT(3-0) response timing	9,10,11	01-03	15		
				04	13		
				05	10		
Pulse duration, to guarantee one interrupt seen 5/ 6/ 7/	t_{W5}			All	P	< 2P 6/	
Delay time, from H1 high to IACK low	t_{D28}	See figure 4 IACK timing		01,02		12	
				03		10	
				04		9	
				05		7	
Delay time, from H1 high to IACK high during first cyclel of IACK instruct-ion data read	t_{D29}			01,02		12	
				03		10	
				04		9	
				05		7	
Delay time, from H1 high to internal CLKX/R	t_{D30}	See figure 4 Data rate mode		01,02		17	
				03		15	
				04		13	
				05		10	

See footnotes at end of table.

TABLE I. Electrical performance characteristics - Continued.

Test	Symbol	Conditions $-55°C \le T_C \le +125°C$ 1/ unless otherwise specified		Group A subgroups	Device type	Limits		Unit
						Min	Max	
Delay time, from H1 high to internal CLKX/R	t_{D30}	See figure 4 Data rate mode		9,10,11	01,02 03 04 05		17 15 13 10	ns
Cycle time, CLKX/R	t_{C3}		CLKX/R ext	9,10,11	All	t_{c2} x 2.6		
			CLKX/R int 5/			t_{C2} x 2	t_{C2} x 2^{32}	
Pulse width, CLKX/R	t_{W6}		CLKX/R ext 6/		01,02	t_{c2} +15		
			CLKX/R ext 6/		03,04	t_{c2}+12		
					05	t_{c2}+10		
			CLKX/R int		All	$(t_{c3}/2)$ -15	$(t_{c3}/2)$ +5	
Rise time, CLKX/R 5/	t_{R3}				01-03 04 05		8 7 6	

See footnotes at end of table.

TABLE I. Electrical performance characteristics - Continued.

Test	Symbol	Conditions $-55°C \le T_C \le +125°C$ 1/ unless otherwise specified		Group A subgroups	Device type	Limits		Unit
						Min	Max	
Fall time, CLKX/R 5/	t_{F3}	See figure 4 Fixed data rate mode		9,10,11	01-03 04 05		8 7 6	ns
Delay time, from CLKX to DX valid	t_{D31}		CLKX ext		01-03 04 05		35 30 24	
			CLKX int		01-03 04 05		20 17 16	
Setup time, DR before CLKR low	t_{SU13}		CLKR ext		01-03 04,05	10 9		
			CLKR int		01-03 04 05	25 21 17		
Hold time, DR from CLKR low	t_{H11}		CLKR ext		01-03 04 05	10 9 7		
			CLKR int 6/		All	0		
Delay time, from CLKX to internal FSX high/low	t_{D32}		CLKX ext		01-03 04 05		32 27 22	
			CLKX int		01-03 04,05		17 15	
Setup time, FSR before CLKR low	t_{SU14}		CLKR ext		01-03 04 05	10 9 7		
			CLKR int		01-03 04 05	10 9 7		
Hold time, FSX/R from CLKX/R low	t_{H12}		CLKX/R ext		01-03 04 05	10 9 7		
			CLKX/R int 6/		All	0		
Setup time, external FSX before CLKX	t_{SU15}		CLKX ext 5/		All	$-(t_{c2}-8)$	$(t_C3/2)-10$	
			CLKX int 5/			$-(t_{c2}-21)$	$t_C3/2$	

See footnotes at end of table.

TABLE I. Electrical performance characteristics - Continued.

Test	Symbol	Conditions $-55°C \le T_C \le +125°C$ 1/ unless otherwise specified		Group A subgroups	Device type	Limits		Unit
						Min	Max	
Delay time, from CLKX to first DX bit, FSX precedes CLKX high	t_{D33}	See figure 4 Variable rate data mode	CLKX ext	9,10,11	01-03		36	ns
					04		30	
					05		24	
			CLKX int		01-03		21	
					04		18	
					05		14	
Delay time, from FSX to first DX bit, CLKX precedes FSX	t_{D34}				01-03		36	
					04		30	
					05		24	
Delay time, from CLKX high to DX high-Z following last data bit 5/	t_{D35}				01-03		20	
					04		17	
					05		14	
Setup time, HOLD valid before H1 low	t_{SU16}	See figure 4 HOLD/HOLDA timing			01-03	15		
					04	13		
					05	10		
HOLDA valid after H1 low 6/	t_{V4}				01-03	0	10	
					04	0	9	
					05	0	7	
Pulse width, HOLD low	t_{W7}				All	2		H1 cycles
Pulse width, HOLDA low 6/	t_{W8}					$t_C(H) -5$		ns
Delay time, from H1 low to STRB high for a HOLD 5/ 6/	t_{D36}				01-03	0	10	
					04	0	9	
					05		7	
Disable time, from H1 low to STRB high impedance state 5/ 6/	t_{DIS4}				01-03	0	10	
					04	0	9	
					05		8	

See footnotes at end of table.

TABLE I. Electrical performance characteristics - Continued.

Test	Symbol	Conditions $-55°C \le T_C \le +125°C$ 1/ unless otherwise specified	Group A subgroups	Device type	Limits		Unit
					Min	Max	
Enable time, from H1 low to STRB active 5/ 6/	t_{EN1}	See figure 4 HOLD/HOLDA timing	9,10,11	01-03	0	10	ns
				04	0	9	
				05	0	7	
Disable time, from H1 low to R/W high impedance state 5/ 6/	t_{DIS5}			01-03	0	10	
				04	0	9	
				05	0	8	
Enable time, from H1 low to R/W active 5/ 6/	t_{EN2}			01-03	0	10	
				04	0	9	
				05	0	7	
Disable time, from H1 low to address high impedance state 5/ 6/	t_{DIS6}			01,02	0	15	
				03	0	10	
				04	0	9	
				05	0	8	
Enable time, from H1 low to address valid 5/ 6/	t_{EN3}			01-03	0	15	
				04	0	13	
				05	0	12	
Disable time, from H1 high to data high impedance state 5/ 6/	t_{DIS7}			01-03	0	15	
				04	0	12	
				05	0	8	

See footnotes at end of table.

TABLE I. Electrical performance characteristics - Continued.

Test	Symbol	Conditions $-55°C \le T_C \le +125°C$ 1/ unless otherwise specified	Group A subgroups	Device type	Limits		Unit
					Min	Max	
Setup time, general purpose input before H1 low	t_{SU17}	See figure 4 Peripheral pin general General purpose I/O timing	9,10,11	01,02 03 04 05	15 12 10 9		ns
Hold time, general-purpose input after H1 low	t_{H13}			All	0		
Delay time, general purpose output after H1 high	t_{D37}			01-03 04 05		15 13 10	
Setup time, TCLK ext before H1 low 8/	t_{SU18}	See figure 4 Timer pin timing	9,10,11	01,02 03 04 05	15 12 10 8		

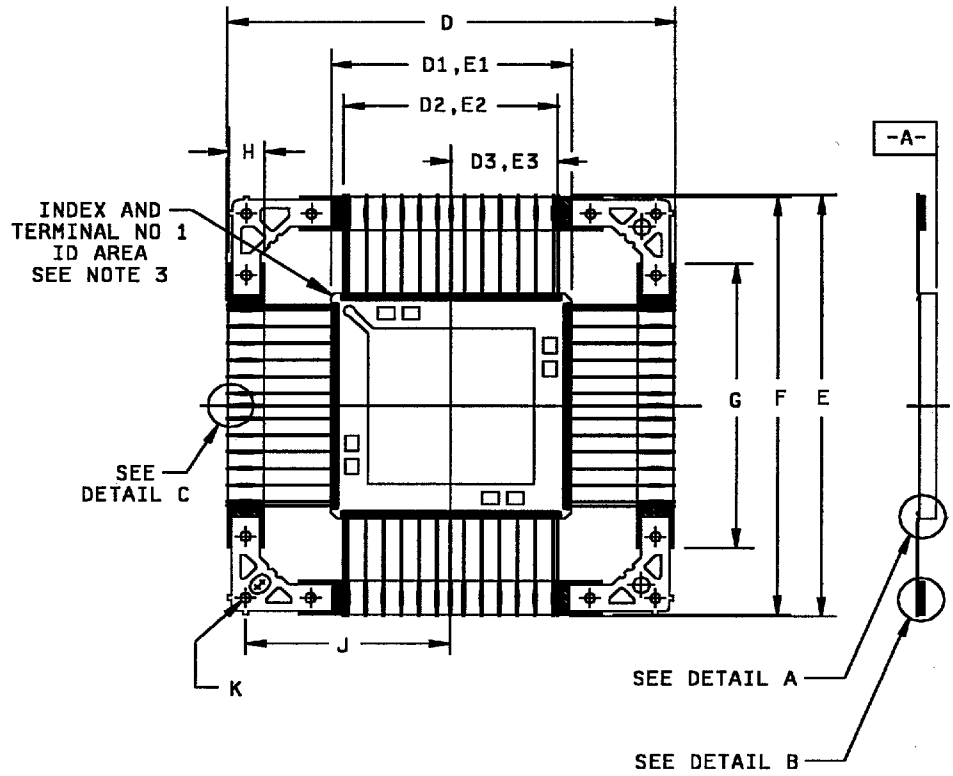
See footnotes at end of table.

TABLE I. Electrical performance characteristics - Continued.

Test	Symbol	Conditions $-55°C \le T_C \le +125°C$ 1/ unless otherwise specified	Group A subgroups	Device type	Limits		Unit
					Min	Max	
Hold time, TCLK ext after H1 low 8/	t_{H14}	See figure 4 Timer pin timing	9,10,11	All	0		ns
Delay time, TCLK int valid after H1 high	t_{D38}			01,02 03 04,05		15 12 9	
Hold time, after H1 high 5/	t_{H15}	See figure 4 Change of peripheral pin from general purpose output to input mode		01-03 04 05		15 13 10	
Setup time, peripheral pin before H1 low	t_{SU19}			01,02 03 04,05	15 12 9		
Hold time, peripheral pin after H1 low	t_{H16}			All	0		
Delay time, from H1 high to peripheral pin switching from input to output	t_{D39}	See figure 4 Change of peripheral pin from general purpose input to output mode		01-03 04 05		15 13 10	

1/ For devices 01, 04 and 05: $4.75 V \le V_{DD} \le 5.25 V$. For devices 02 and 03: $4.5 V \le V_{DD} \le 5.5 V$, unless otherwise specified. All other test conditions shall be worst case conditions unless otherwise specified.
2/ V_{OL} for XA(12-0) is guaranteed from characterization data but not tested.
3/ Pins with internal pull-up devices: INT(0-3), MC/MP, RSV(0-10).
4/ Actual operating current will be less than this maximum value. This value was obtained under specially produced worst-case test conditions, which are not sustained during normal device operation. These conditions consist of continous parallel writes of a checkerboard pattern to both primary and expansion buses at the maximum rate possible.
5/ Maximum limit is derived by design to the limits specified in table I.
6/ Minimum limit is derived from characterization to the limits specified in table I.
7/ Interrupt pulse width must be at least 1 P wide to guarantee it will be seen. It must be less than 2 P wide to guarantee it will be responded to only once. The recommended pulse width is 1.5 P. P = one H1 cycle.
8/ Applicable for a synchronous input clock.

Case U

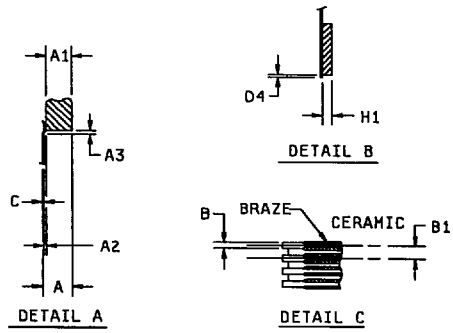


NOTES:

1. Actual pin count not represented for clarity purposes.
2. Metric equivalents for information purposes only.
3. A terminal 1 identification mark shall be located at the index corner in the area shown. Terminal 1 is located immediately adjacent to and counterclockwise from the index corner. Terminal numbers increase in a counterclockwise direction when viewed as shown. The index corner shall be clearly unique.

FIGURE 1. Case outline.

Case U



Letter	Millimeters		Inches		Notes
	Min	Max	Min	Max	
A	---	3.30	---	0.130	
A1	---	2.67	---	0.105	
A2	0.15	0.30	0.006	0.012	At braze pads
A3	---	0.046	---	0.018	
B	0.18	0.33	0.007	0.013	
B1	.064 BSC		.025		
C	0.10	0.23	0.004	0.009	
D	63.50	64.52	2.500	2.540	
D1,E1	33.70	34.70	1.325	1.365	
D2,E2	30.50 BSC		1.200 BSC		
D3,E3	15.25 BSC		0.600 BSC		
D4	---	0.51	---	0.020	
E	63.50	64.52	2.500	2.540	
F	63.12	63.63	2.485	2.505	Tie bar dimension
G	42.93	43.43	1.690	1.710	Tie bar dimension
H	4.45	5.72	0.175	0.225	Tie bar dimension
H1	0.76	1.02	0.030	0.040	Tie bar dimension
J	29.21 BSC		1.150 BSC		
K	1.50	1.55	0.059	0.061	4 places

FIGURE 1. Case outlines - continued.

Case Y

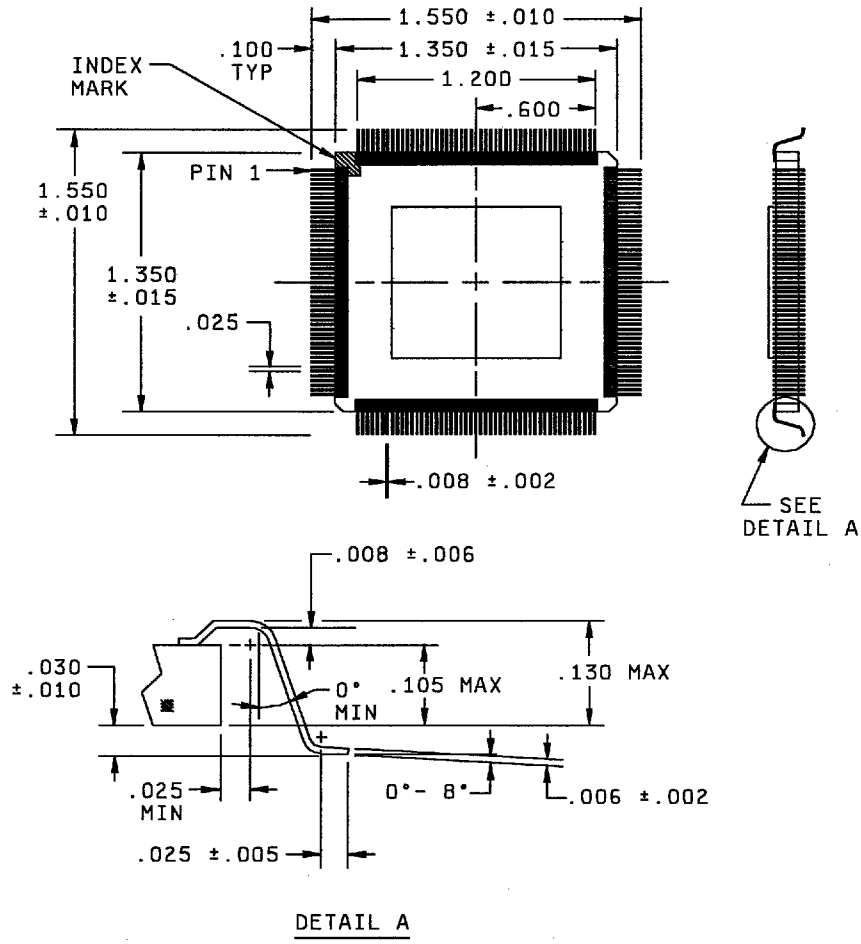
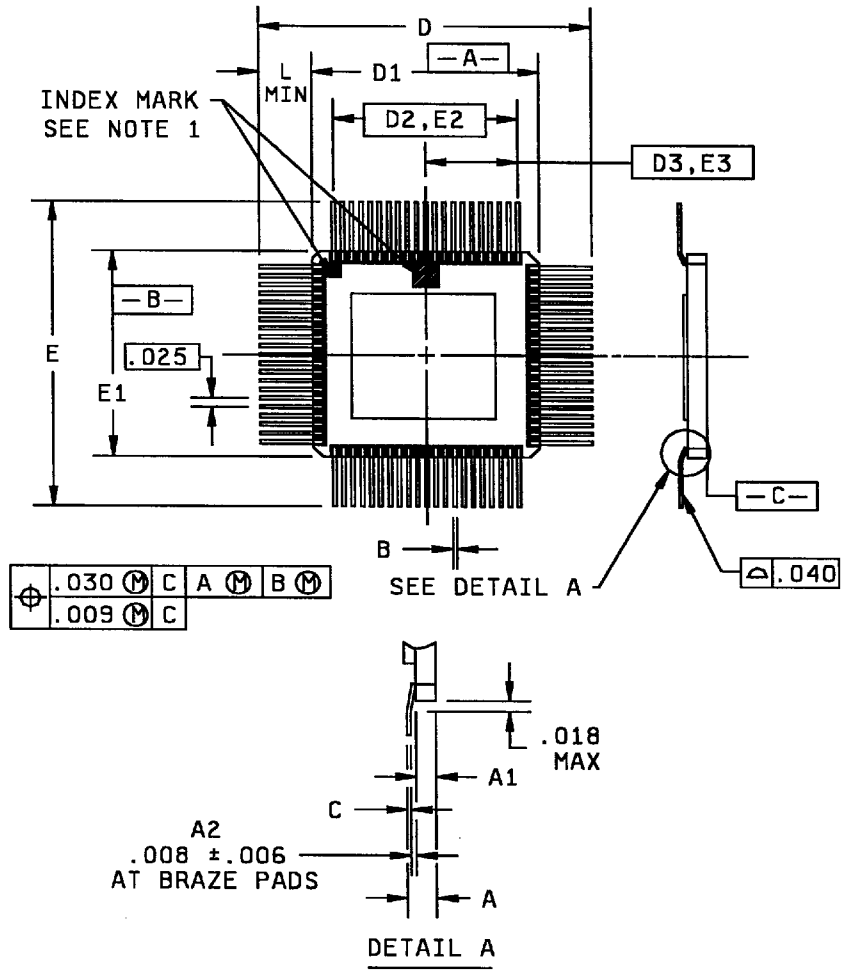


FIGURE 1. Case outlines - continued.

Case Z



NOTES: Actual terminal count not represented for clarity purposes.

FIGURE 1. Case outlines - continued.

Case Z

Symbol	Millimeters		Inches	
	Min	Max	Min	Max
A		3.302		0.130
A1		2.667		0.105
B	0.152	0.254	0.006	0.010
C	0.102	0.203	0.004	0.008
D, E	47.752	48.641	1.880	1.915
D1, E1	33.909	34.671	1.335	1.365
D2, E2	30.48 BSC		1.200 BSC	
D3, E3	15.24 BSC		0.600 BSC	
L	6.35		0.250	
N	196		196	
ND	49		49	

NOTES: N = Total number of leads.
ND = Total number of leads per side.

FIGURE 1. Case outlines - continued.

Case T, M

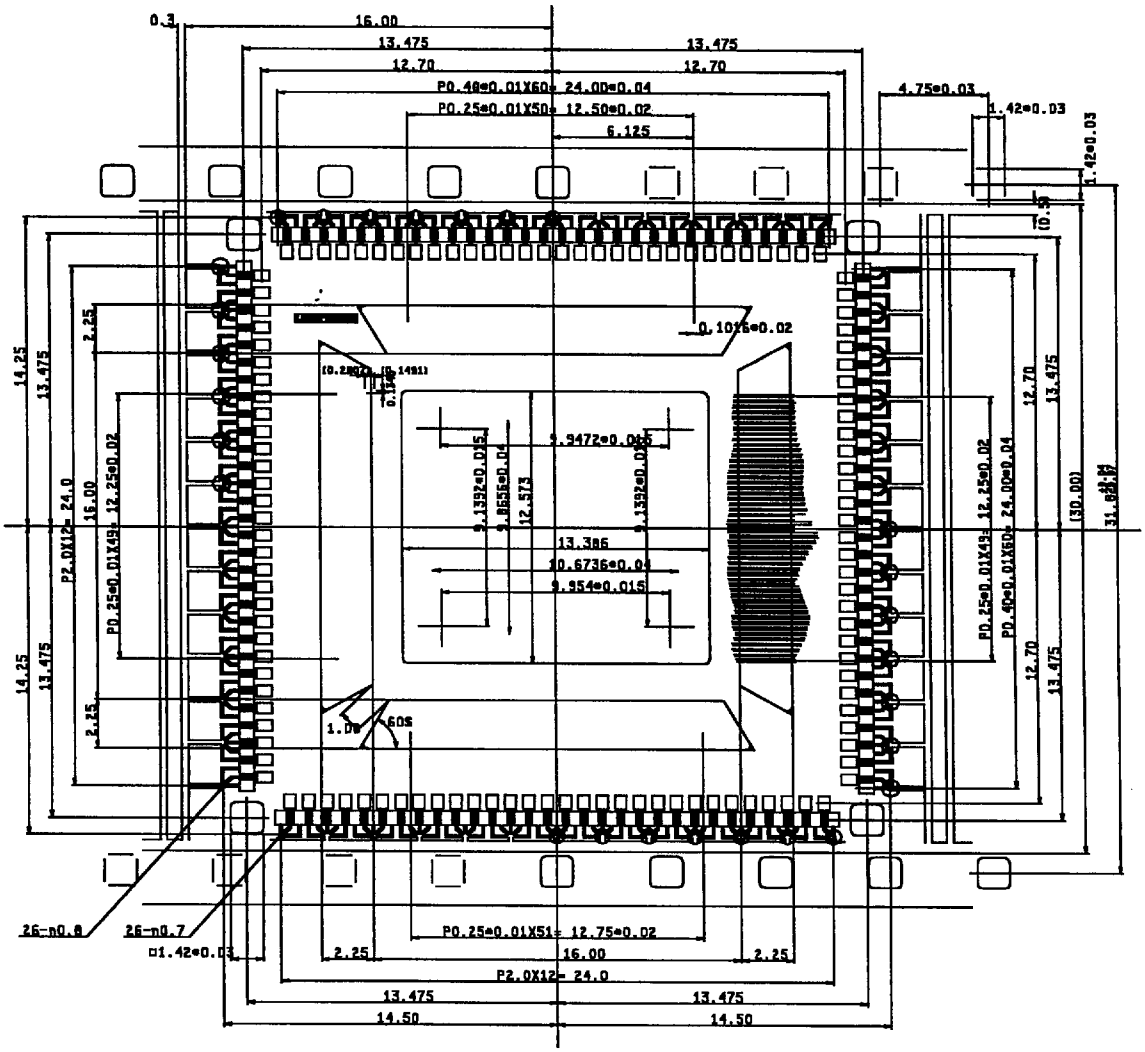


Figure 1. Case Outline - Continued

Device types 01,02,03,04 and 05
1/ 2/ 3/ 4/
Case outline X

Terminal number	Terminal symbol	Terminal number	Terminal symbol	Terminal number	Terminal symbol	Terminal number	Terminal symbol	Terminal number	Terminal symbol
F15	A0	C4	D0	P3	FSR0	A13	XA0	R4	XD0
G12	A1	D5	D1	R2	FSX0	A14	XA1	P5	XD1
G13	A2	A2	D2	N4	CLKR0	D11	XA2	N6	XD2
G14	A3	A3	D3	M5	CLKX0	C12	XA3	R5	XD3
G15	A4	B4	D4	R1	DR0	B13	XA4	P6	XD4
H15	A5	C5	D5	R3	DX0	A15	XA5	M7	XD5
H14	A6	D6	D6	M3	FSR1	B15	XA6	R6	XD6
J15	A7	A4	D7	P1	FSX1	C14	XA7	N7	XD7
J14	A8	B5	D8	L4	CLKR1	E12	XA8	P7	XD8
J13	A9	C6	D9	N2	CLKX1	D13	XA9	R7	XD9
K15	A10	A5	D10	N1	DR1	C15	XA10	P8	XD10
J12	A11	B6	D11	P2	DX1	D14	XA11	R8	XD11
K14	A12	D7	D12			E13	XA12	R9	XD12
L15	A13	A6	D13	F14	EMU0	J3	RSV0	P9	XD13
K13	A14	C7	D14	E15	EMU1	J4	RSV1	N9	XD14
L14	A15	B7	D15	F13	EMU2	K1	RSV2	R10	XD15
M15	A16	A7	D16	E14	EMU3	K2	RSV3	M9	XD16
K12	A17	A8	D17	F12	EMU4	L1	RSV4	P10	XD17
L13	A18	B8	D18	C1	EMU5	K3	RSV5	R11	XD18
M14	A19	A9	D19	M6	EMU6	L2	RSV6	N10	XD19
N15	A20	B9	D20	B3	H1	K4	RSV7	P11	XD20
M13	A21	C9	D21	A1	H3	M1	RSV8	R12	XD21
L12	A22	A10	D22			L3	RSV9	M10	XD22
N14	A23	D9	D23	C2	X1	M2	RSV10	N11	XD23
E5	LOC	B10	D24	B1	X2/CLKIN	D12	ADV_{DD}	P12	XD24
G1	$\overline{ACK}$	A11	D25	P4	TCLK0	H11	ADV_{DD}	R13	XD25
H2	$\overline{INT0}$	C10	D26	N5	TCLK1	D4	DDV_{DD}	R14	XD26
H1	$\overline{INT1}$	B11	D27			E8	DDV_{DD}	M11	XD27
J1	$\overline{INT2}$	A12	D28	G2	XF0	L8	$IODV_{DD}$	N12	XD28
J2	$\overline{INT3}$	D10	D29	G3	XF1	M12	$IODV_{DD}$	P13	XD29
D15	$\overline{MC/MP}$	C11	D30	D3	V_{BBP}	H5	MDV_{DD}	R15	XD30
E3	$\overline{MSTRB}$	B12	D31	E4	V_{SUBS}	M4	PDV_{DD}	P15	XD31
E1	$\overline{RDY}$		$\overline{\quad\quad}$	H4	V_{DD}	B2	CV_{SS}	C3	DV_{SS}
F1	$\overline{RESET}$	F3	$\overline{HOLD}$	D8	V_{DD}	P14	CV_{SS}	C13	DV_{SS}
G4	$\overline{R/W}$	E2	$\overline{HOLDA}$	M8	V_{DD}	C8	V_{SS}	N3	DV_{SS}
F2	$\overline{STRB}$	D2	$\overline{XRDY}$	H12	V_{DD}	H3	V_{SS}	N13	DV_{SS}
F4	$\overline{IOSTRB}$	D1	$\overline{XR/W}$	N8	V_{SS}	H13	V_{SS}	B14	IV_{SS}

FIGURE 2. Terminal connections.

Device types 01, 02, 03, 04 and 05
1/ 2/ 3/ 4/
Case outlines: U, Y and Z

Terminal number	Terminal symbol	Terminal number	Terminal symbol	Terminal number	Terminal symbol	Terminal number	Terminal symbol	Terminal number	Terminal symbol
1	PDV_{DD}	40	XD22	79	A3	118	D22	157	MSTRB
2	PDV_{DD}	41	XD23	80	A2	119	D21	158	IOSTRB
3	DR0	42	XD24	81	A1	120	D20	159	XR/W
4	FSR0	43	XD25	82	A0	121	D19	160	HOLDA
5	CLKR0	44	XD26	83	EMU0	122	D18	161	HOLD
6	CLKX0	45	XD27	84	EMU1	123	V_{DD}	162	MDV_{DD}
7	FSX0	46	XD28	85	EMU2	124	V_{DD}	163	MDV_{DD}
8	DX0	47	XD29	86	EMU3	125	V_{SS}	164	RDY
9	TCLK0	48	XD30	87	EMU4	126	V_{SS}	165	STRB
10	TCLK1	49	$IODV_{DD}$	88	MC/MP	127	D17	166	R/W
11	EMU6	50	DV_{SS}	89	XA12	128	D16	167	RESET
12	XD0	51	CV_{SS}	90	XA11	129	D15	168	XF1
13	XD1	52	CV_{SS}	91	XA10	130	D14	169	XF0
14	XD2	53	XD31	92	XA9	131	D13	170	IACK
15	$IODV_{DD}$	54	A23	93	XA8	132	D12	171	INT0
16	$IODV_{DD}$	55	A22	94	XA7	133	D11	172	V_{DD}
17	XD3	56	A21	95	XA6	134	D10	173	V_{DD}
18	XD4	57	A20	96	IV_{SS}	135	D9	174	V_{SS}
19	XD5	58	A19	97	IV_{SS}	136	D8	175	V_{SS}
20	XD6	59	A18	98	DV_{SS}	137	D7	176	INT1
21	XD7	60	A17	99	V_{SUBS}	138	D6	177	INT2
22	XD8	61	A16	100	ADV_{DD}	139	D5	178	INT3
23	XD9	62	A15	101	ADV_{DD}	140	D4	179	RSV0
24	XD10	63	A14	102	XA5	141	D3	180	RSV1
25	V_{DD}	64	ADV_{DD}	103	XA4	142	D2	181	RSV2
26	V_{DD}	65	A13	104	XA3	143	D1	182	RSV3
27	V_{SS}	66	A12	105	XA2	144	D0	183	RSV4
28	V_{SS}	67	A11	106	XA1	145	H1	184	RSV5
29	XD11	68	A10	107	XA0	146	H3	185	RSV6
30	XD12	69	A9	108	D31	147	DDV_{DD}	186	RSV7
31	XD13	70	A8	109	D30	148	DV_{SS}	187	RSV8
32	XD14	71	A7	110	D29	149	CV_{SS}	188	RSV9
33	XD15	72	A6	111	D28	150	CV_{SS}	189	RSV10
34	XD16	73	V_{DD}	112	D27	151	X2/CLKIN	190	DR1
35	XD17	74	V_{DD}	113	D26	152	X1	191	FSR1
36	XD18	75	V_{SS}	114	DDV_{DD}	153	V_{SUBS}	192	CLKR1
37	XD19	76	V_{SS}	115	D25	154	V_{BBP}	193	CLKX1
38	XD20	77	A5	116	D24	155	EMU5	194	FSX1
39	XD21	78	A4	117	D23	156	XRDY	195	DX1
								196	DV_{SS}

1/ ADV_{DD}, DDV_{DD}, $IODV_{DD}$, MDV_{DD}, and PDV_{DD} pins are on a common plane internal to the device.
2/ V_{DD} pins are on a common plane internal to the device.
3/ V_{SS}, CV_{SS}, and IV_{SS} pins are on a common plane internal to the device.
4/ DV_{SS} pins are on a common plane internal to the device.

FIGURE 2. Terminal connections - continued

Case T, M

DIE BOND PAD LOCATIONS	DIE/TAB BOND PAD IDENTITY	TAB TEST PAD LOCATIONS	X COORDINATE OF THE DIE BOND PAD	Y COORDINATE OF THE DIE BOND PAD	PITCH OF LEAD (#,#) REFERENCE WHICH DIE BOND PADS
Die Side #1					
1	PDV_{DD}	1,2	-423.80	9563.00	195.20 (1,2)
2	PDV_{DD}	3,4		9367.80	168.60 (2,3)
3	DR0	5		9199.20	192.00 (3,4)
4	FSR0	6		9007.20	184.00 (4,5)
5	CLKR0	7		8823.20	192.00 (5,6)
6	CLKX0	8		8631.20	184.00 (6,7)
7	FSX0	9		8447.20	192.00 (7,8)
8	DX0	10		8255.20	184.00 (8,9)
9	TCLK0	11		8071.20	192.00 (9,10)
10	TCLK1	12		7879.20	184.00 (10,11)
11	EMU6	13		7695.20	192.00 (11,12)
12	XD0	14		7503.20	184.00 (12,13)
13	XD1	15		7319.20	192.00 (13,14)
14	XD2	16		7127.20	180.20 (14,15)
15	$IODV_{DD}$	17,18		6947.00	195.20 (15,16)
16	$IODV_{DD}$	19,20		6751.80	168.60 (16,17)
17	XD3	21		6853.20	184.00 (17,18)
18	XD4	22		6399.20	192.00 (18,19)
19	XD5	23		6207.20	184.00 (19,20)
20	XD6	24		6023.20	192.00 (20,21)
21	XD7	25		5831.20	184.00 (21,22)
22	XD8	26		5647.20	192.00 (22,23)
23	XD9	27		5455.20	184.00 (23,24)
24	XD10	28		5271.20	188.20 (24,25)
25	V_{DD}	29,30		5083.00	195.20 (25,26)
26	V_{DD}	31,32		4887.80	156.80 (26,27)
27	V_{SS}	33,34,35		4731.00	195.20 (27,28)
28	V_{SS}	36,37		4535.80	168.60 (28,29)
29	XD11	38		4367.20	184.00 (29,30)
30	XD12	39		4183.20	192.00 (30,31)
31	XD13	40		3991.20	184.00 (31,32)
32	XD14	41		3807.20	192.00 (32,33)
33	XD15	42		3615.20	184.00 (33,34)
34	XD16	43		3431.20	192.00 (34,35)
35	XD17	44		3239.20	184.00 (35,36)
36	XD18	45		3055.20	192.00 (36,37)
37	XD19	46		2863.20	184.00 (37,38)
38	XD20	47		2679.20	192.00 (38,39)
39	XD21	48		2487.20	184.00 (39,40)
40	XD22	49		2303.20	192.00 (40,41)
41	XD23	50		2111.20	184.00 (41,42)
42	XD24	51		1927.20	192.00 (42,43)
43	XD25	52		1735.20	184.00 (43,44)
44	XD26	53		1551.20	192.00 (44,45)
45	XD27	54		1359.20	184.00 (45,46)
46	XD28	55		1175.20	192.00 (46,47)
47	XD29	56		983.20	184.00 (47,48)
48	XD30	57		799.20	180.20 (48,49)
49	$IODV_{DD}$	58,59		619.00	195.20 (49,50)
50	$IODV_{DD}$	60,61		423.80	

FIGURE 2. Terminal connections - continued

Case T, M

DIE BOND PAD LOCATIONS	DIE/TAB BOND PAD IDENTITY	TAB TEST PAD LOCATIONS	X COORDINATE OF THE DIE BOND PAD	Y COORDINATE OF THE DIE BOND PAD	PITCH OF LEAD (#,#) REFERENCE WHICH DIE BOND PADS
Die Side #2					
51	DV_{SS}	62,63	0.00	0.00	195.20 (51,52)
52	DV_{SS}	64	195.20		179.60 (52,53)
53	CV_{SS}	65,66	374.80		195.20 (53,54)
54	CV_{SS}	67	570.00		176.60 (54,55)
55	XD31	68	746.60		192.00 (55,56)
56	A23	69	938.60		200.00 (56,57)
57	A22	70	1138.60		200.00 (57,58)
58	A21	71	1338.60		192.00 (58,59)
59	A20	72	1530.60		200.00 (59,60)
60	A19	73	1730.60		192.00 (60,61)
61	A18	74	1922.60		200.00 (61,62)
62	A17	75	2122.60		200.00 (62,63)
63	A16	76	2322.60		192.00 (63,64)
64	A15	77	2514.36		200.00 (64,65)
65	A14	78	2902.80		188.20 (65,66)
66	ADV_{DD}	79,80	2714.60		195.20 (66,67)
67	ADV_{DD}	81	2902.80		176.60 (67,68)
68	A13	82	3098.00		200.00 (68,69)
69	A12	83	3274.60		192.00 (69,70)
70	A11	84	3474.60		200.00 (70,71)
71	A10	85	3666.60		200.00 (71,72)
72	A9	86	3866.60		192.00 (72,73)
73	A8	87	4258.60		200.00 (73,74)
74	A7	88	4458.60		192.00 (74,75)
75	A6	89	4650.60		196.20 (75,76)
76	V_{DD}	90,91	4846.80		195.20 (76,77)
77	V_{DD}	92,93	5042.00		172.80 (77,78)
78	V_{SS}	94,95	5214.80		195.20 (78,79)
79	V_{SS}	96,97	2410.00		168.60 (79,80)
80	A5	98	5578.60		200.00 (80,81)
81	A4	99	5778.60		192.00 (81,82)
82	A3	100	5970.60		200.00 (82,83)
83	A2	101	6170.60		200.00 (83,84)
84	A1	102	6370.60		192.00 (84,85)
85	A0	103	6562.60		212.20 (85,86)
86	EMU0	104	6774.80		216.00 (86,87)
87	EMU1	105	6990.80		208.00 (87,88)
88	EMU2	106	7198.80		203.80 (88,89)
89	EMU3	107	7402.60		204.20 (89,90)
90	EMU4	108	7606.80		216.00 (90,91)
91	MC/MP	109	7822.80		203.80 (91,92)
92	XA12	110	8026.60		192.00 (92,93)
93	XA11	111	8218.60		200.00 (93,94)
94	XA10	112	8418.60		192.00 (94,95)
95	XA9	113	8610.60		200.00 (95,96)
96	XA8	114	8810.60		200.00 (96,97)
97	XA7	115	9010.60		192.00 (97,98)
98	XA6	116	9202.60		196.20 (98,99)
99	IV_{SS}	117,118	9398.80		195.20 (99,100)
100	IV_{SS}	119	9594.00		164.80 (100,101)
101	DV_{SS}	120,121	9758.80		195.20 (101,102)
102	DV_{SS}	122	9954.00		

FIGURE 2. Terminal connections - continued

Case T, M

DIE BOND PAD LOCATIONS	DIE/TAB BOND PAD IDENTITY	TAB TEST PAD LOCATIONS	X COORDINATE OF THE DIE BOND PAD	Y COORDINATE OF THE DIE BOND PAD	PITCH OF LEAD (#,#) REFERENCE WHICH DIE BOND PADS
Die Side #3					
103	ADV_{DD}	123,124	10377.80	430.60	195.20 (103,104)
104	ADV_{DD}	125,126		625.80	168.60 (104,105)
105	XA5	127		764.40	192.00 (105,106)
106	XA4	128		986.40	184.00 (106,107)
107	XA3	129		1170.40	192.00 (107,108)
108	XA2	130		1362.40	184.00 (108,109)
109	XA1	131		1546.40	192.00 (109,110)
110	XA0	132		1738.40	184.00 (110,111)
111	D31	133		1922.40	192.00 (111,112)
112	D30	134		2114.40	184.00 (112,113)
113	D29	135		2298.40	192.00 (113,114)
114	D28	136		2490.40	184.00 (114,115)
115	D27	137		2674.40	192.00 (115,116)
116	D26	138		2866.40	180.20 (116,117)
117	DDV_{DD}	139,140		3046.60	195.20 (117,118)
118	DDV_{DD}	141,142		3241.80	168.60 (118,119)
119	D25	143		3410.40	184.00 (119,120)
120	D24	144		3594.40	192.00 (120,121)
121	D23	145		3786.40	184.00 (121,122)
122	D22	146		3970.40	192.00 (122,123)
123	D21	147		4162.40	184.00 (123,124)
124	D20	148		4346.40	192.00 (124,125)
125	D19	149		4538.40	184.00 (125,126)
126	D18	150		4722.40	188.20 (126,127)
127	V_{DD}	151,152		4910.60	195.20 (127,128)
128	V_{DD}	153,154,155		5105.80	156.80 (128,129)
129	V_{SS}	156,157		5262.60	195.20 (129,130)
130	V_{SS}	158,159		5457.80	168.60 (130,131)
131	D17	160		5626.40	184.00 (131,132)
132	D16	161		5810.40	192.00 (132,133)
133	D15	162		6002.40	184.00 (133,134)
134	D14	163		6186.40	192.00 (134,135)
135	D13	164		6378.40	184.00 (135,136)
136	D12	165		6562.40	192.00 (136,137)
137	D11	166		6754.40	184.00 (137,138)
138	D10	167		6938.40	192.00 (138,139)
139	D9	168		7130.40	184.00 (139,140)
140	D8	169		7314.40	192.00 (140,141)
141	D7	170		7506.40	184.00 (141,142)
142	D6	171		7690.40	192.00 (142,143)
143	D5	172		7882.40	184.00 (143,144)
144	D4	173		8066.40	192.00 (144,145)
145	D3	174		8258.40	184.00 (145,146)
146	D2	175		8442.40	192.00 (146,147)
147	D1	176		8634.40	184.00 (147,148)
148	D0	177		8818.40	192.00 (148,149)
149	H1	178		9010.40	184.00 (149,150)
150	H3	179		9194.40	180.20 (150,151)
151	DDV_{DD}	180,181		9374.60	195.20 (151,152)
152	DDV_{DD}	182,183		9569.80	

FIGURE 2. Terminal connections - continued

Case T, M

DIE BOND PAD LOCATIONS	DIE/TAB BOND PAD IDENTITY	TAB TEST PAD LOCATIONS	X COORDINATE OF THE DIE BOND PAD	Y COORDINATE OF THE DIE BOND PAD	PITCH OF LEAD (#,#) REFERENCE WHICH DIE BOND PADS
Die Side #4					
153	DV_{SS}	184	9947.20	9993.60	195.20 (153,154)
154	DV_{SS}	185,186	9752.00	9993.60	164.80 (154,155)
155	CV_{SS}	187	9587.20	9993.60	195.20 (155,156)
156	CV_{SS}	188,189	9392.00	9993.60	175.00 (156,157)
157	X2/CLKIN	190	9217.00	9986.80	173.20 (157,158)
158	X1	191	9043.80	9986.80	347.80 (158,159)
159	V_{SUBS}	192,193	8696.00	9993.60	160.60 (159,160)
160	V_{BBP}	194	8535.40	9993.60	600.00 (160,161)
161	EMU5	195	7935.40	9993.60	196.00 (161,162)
162	XRDY	196	7739.40	9993.60	188.00 (162,163)
163	MSTRB	197	7551.40	9993.60	192.00 (163,164)
164	IOSTRB	198	7359.40	9993.60	184.00 (164,165)
165	XRW	199	7175.40	9993.60	184.00 (165,166)
166	HOLDA	200	6991.40	9993.60	196.20 (166,167)
167	HOLD	201	6795.20	9993.60	184.00 (167,168)
168	MDV_{DD}	202	6611.20	9993.60	195.20 (168,169)
169	MDV_{DD}	203,204	6416.00	9993.60	172.80 (169,170)
170	RDY	205	6243.20	9993.60	187.80 (170,171)
171	STRB	206	6055.40	9993.60	192.00 (171,172)
172	R/W	207	5863.40	9993.60	196.20 (172,173)
173	RESET	208	5667.20	9993.60	187.80 (173,174)
174	XF1	209	5479.40	9993.60	184.00 (174,175)
175	XF0	210	5295.40	9993.60	184.00 (175,176)
176	IACK	211	5111.40	9993.60	196.20 (176,177)
177	INT0	212	4915.20	9993.60	184.00 (177,178)
178	V_{DD}	213,214	4731.20	9993.60	195.20 (178,179)
179	V_{DD}	215,216	4536.00	9993.60	164.80 (179,180)
180	V_{SS}	217,218	4371.20	9993.60	195.20 (180,181)
181	V_{SS}	219,220	4176.00	9993.60	172.80 (181,182)
182	INT1	221	4003.20	9993.60	200.00 (182,183)
183	INT2	222	3803.20	9993.60	200.00 (183,184)
184	INT3	223	3603.20	9993.60	200.00 (184,185)
185	RSV0	224	3403.20	9993.60	200.00 (185,186)
186	RSV1	225	3203.20	9993.60	200.00 (186,187)
187	RSV2	226	3003.20	9993.60	208.00 (187,188)
188	RSV3	227	2795.20	9993.60	200.00 (188,189)
189	RSV4	228	2595.20	9993.60	187.80 (189,190)
190	RSV5	229	2407.40	9993.60	184.00 (190,191)
191	RSV6	230	2223.40	9993.60	184.00 (191,192)
192	RSV7	231	2039.40	9993.60	184.00 (192,193)
193	RSV8	232	1855.40	9993.60	184.00 (193,194)
194	RSV9	233	1671.40	9993.60	192.00 (194,195)
195	RSV10	234	1479.40	9993.60	184.00 (195,196)
196	DR1	235	1295.40	9993.60	184.00 (196,197)
197	FSR1	236	1111.40	9993.60	184.00 (197,198)
198	CLKR1	237	927.40	9993.60	184.00 (198,199)
199	CLKX1	238	743.40	9993.60	184.00 (199,200)
200	FSX1	239	559.40	9993.60	184.00 (200,201)
201	DX1	240	375.40	9993.60	180.20 (201,202)
202	DV_{SS}	241,242	195.20	9993.60	195.20 (202,203)
203	DV_{SS}	243,244	0.00	9993.60	

FIGURE 2. Terminal connections - continued

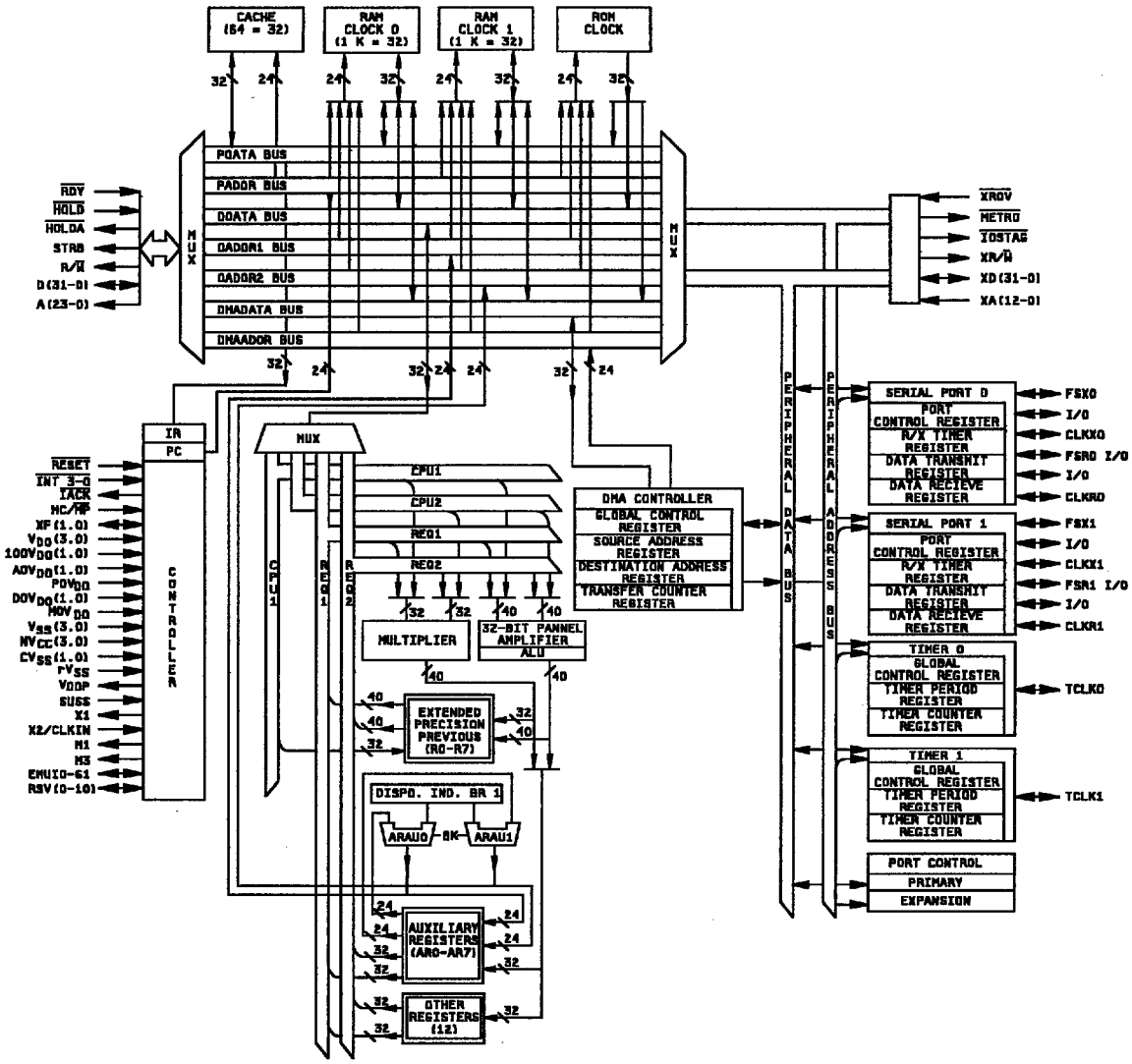
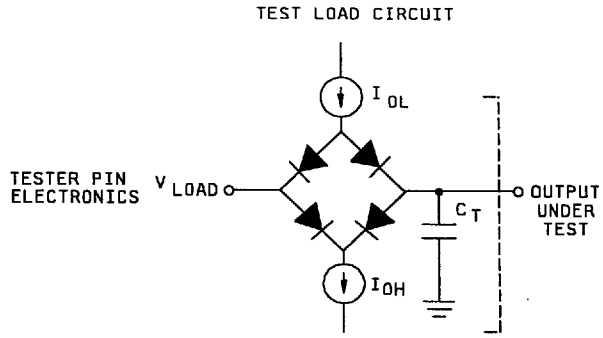


FIGURE 3. Functional block diagram.

STANDARD MICROCIRCUIT DRAWING DEFENSE SUPPLY CENTER COLUMBUS COLUMBUS, OHIO 43216-5000	SIZE A		5962-90526
		REVISION LEVEL G	SHEET 32



Where: I_{OL} = 2.0 mA (all outputs)
I_{OH} = 300 µA (all outputs)
V_{Load} = 1.54 V to emulate 50Ω
C_T = 80 pF typical load circuit capacitance.

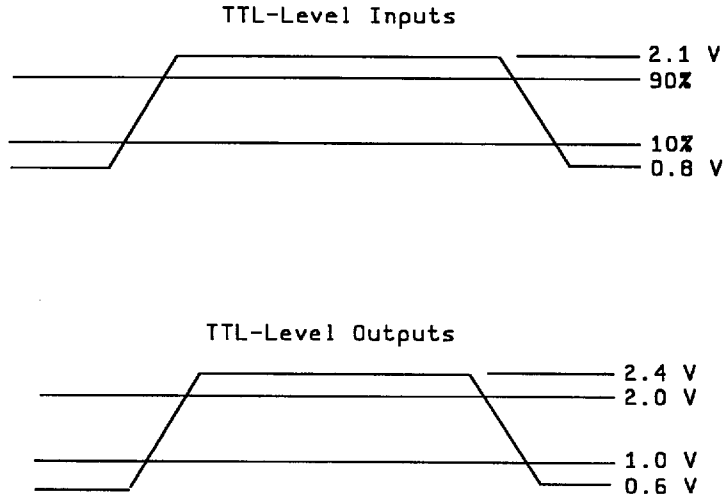
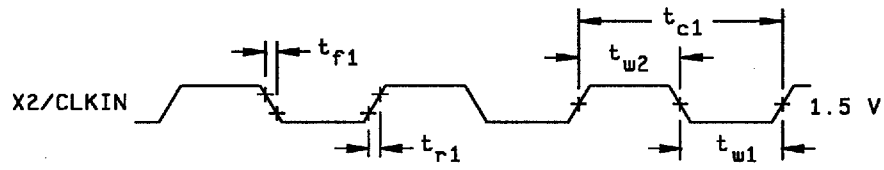


FIGURE 4. Switching waveforms and test circuit.

X2/CLKIN timing



H1/H3 timing

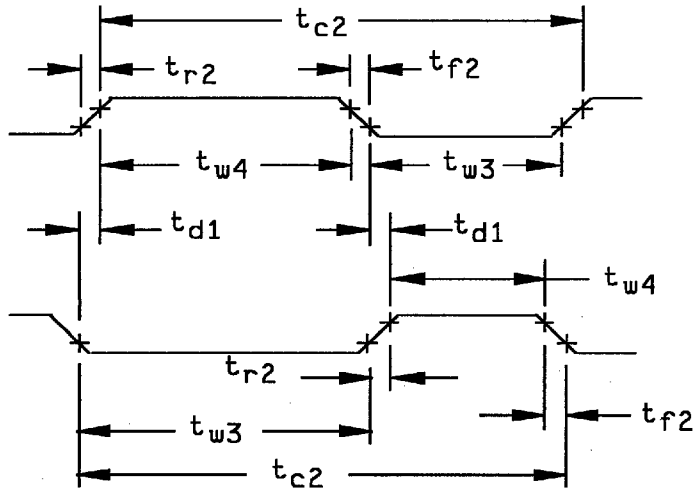


FIGURE 4. Switching waveforms and test circuit - continued.

Memory ($\overline{(M)STRB}$ = 0) Read

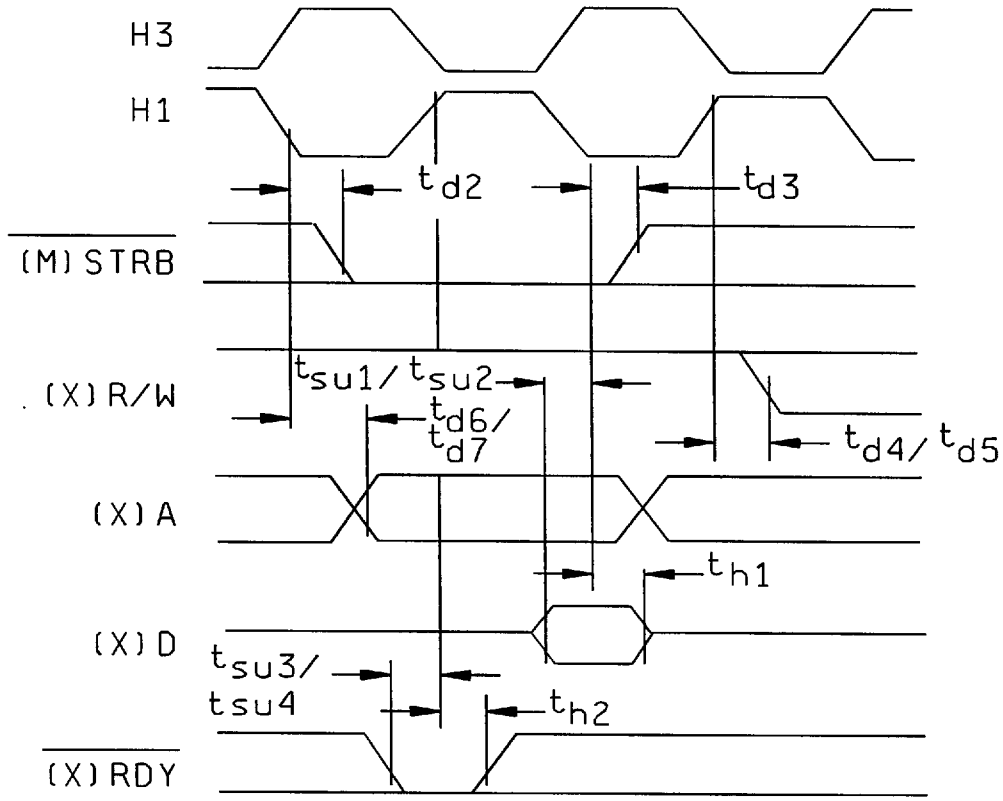
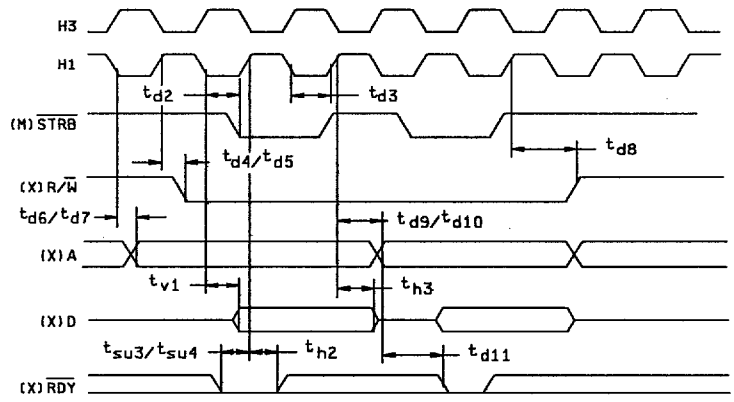


FIGURE 4. Switching waveforms and test circuit - continued.

Memory ($\overline{\text{(M)STRB}}$ = 0) Write



Memory ($\overline{(IO)STRB}$ = 0) Read

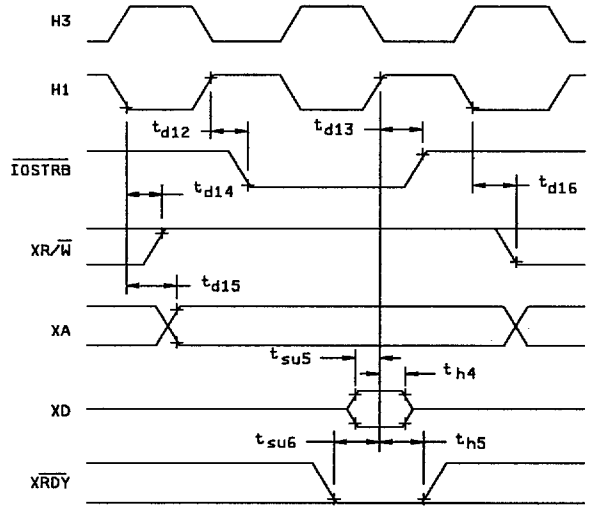


FIGURE 4. Switching waveforms and test circuit - continued.

Memory ((IO)$\overline{STRB}$ = 0) Write

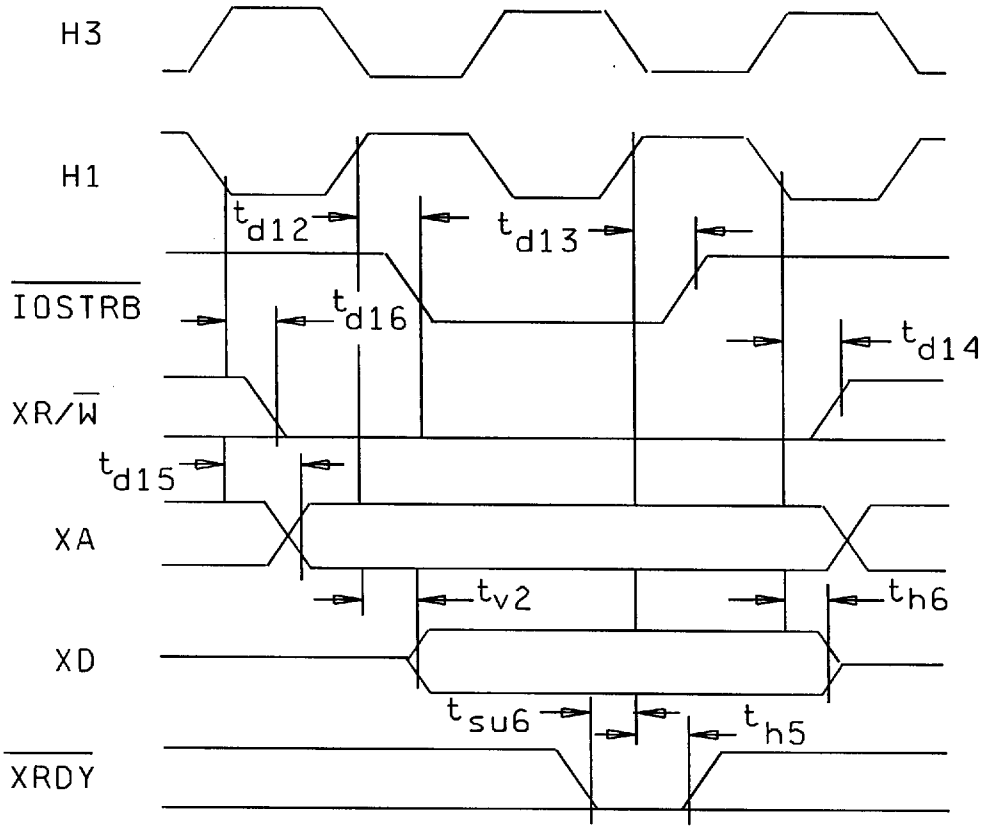
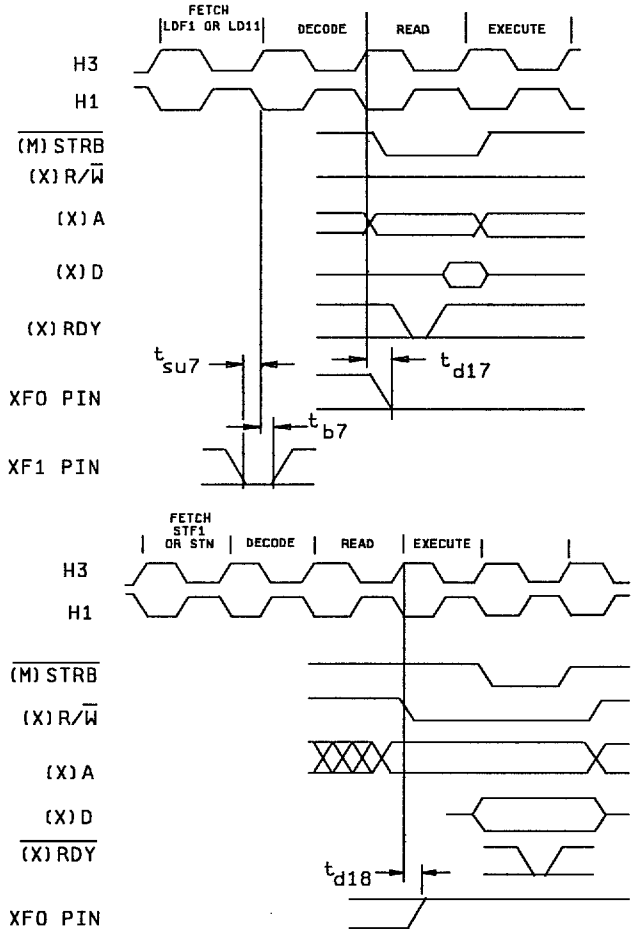


FIGURE 4. Switching waveforms and test circuit - continued.

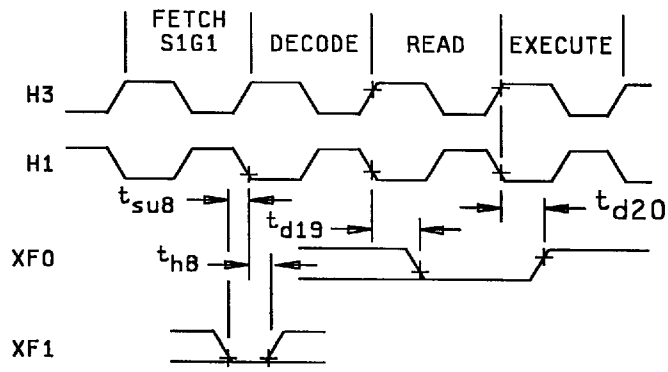
Timing XF0 and XF1 when executing LDF1 or LDII



Timing for XF0 when executing a STF1 or STII

FIGURE 4. Switching waveforms and test circuit - continued.

Timing for XF0 and XF1 when executing SIGI



Timing for loading XF register when configured as an output pin

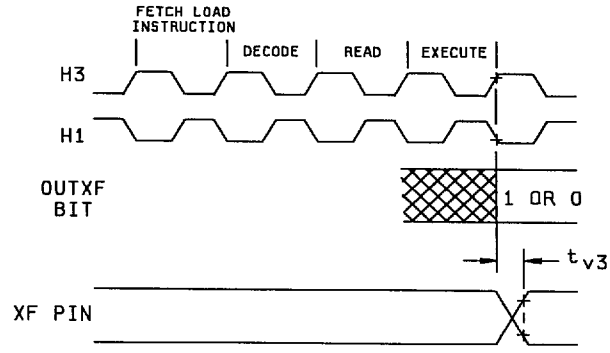
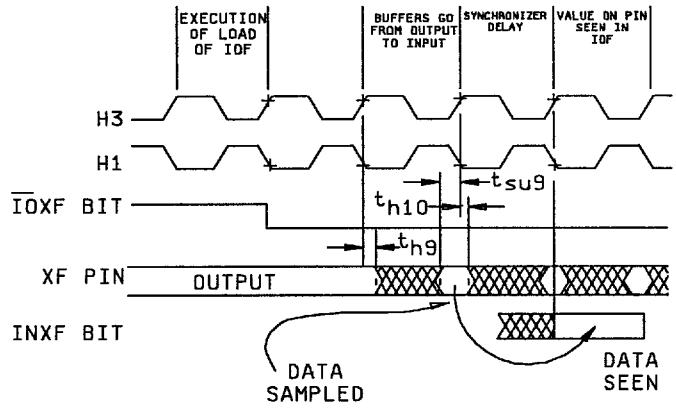


FIGURE 4. Switching waveforms and test circuit - continued.

Change of XF from output to input mode



Change of XF from input to output mode

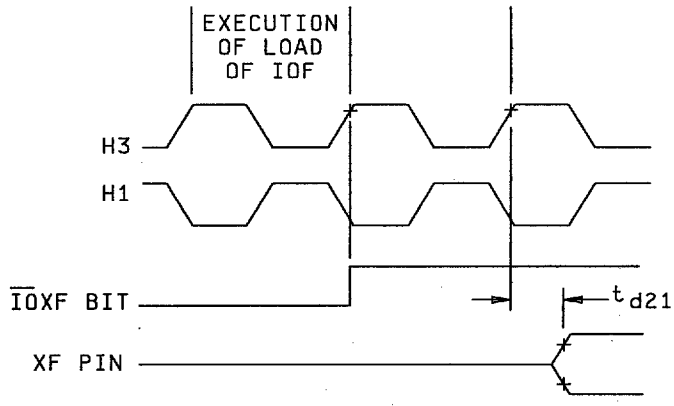
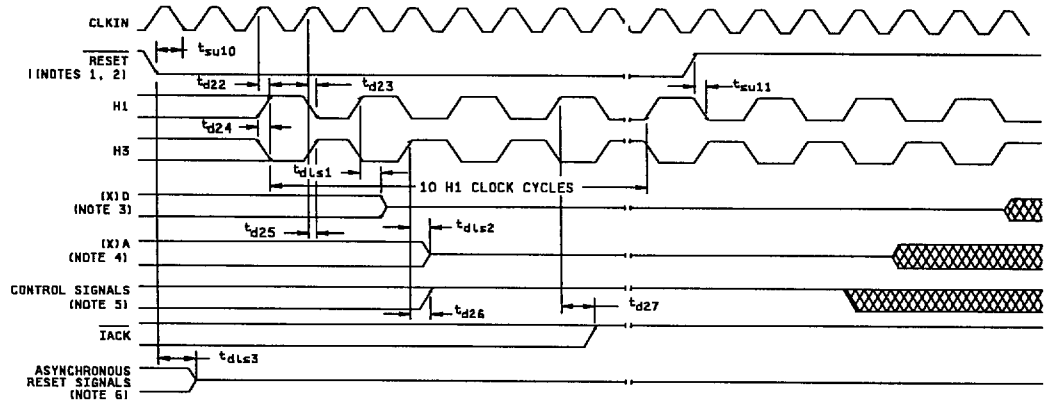


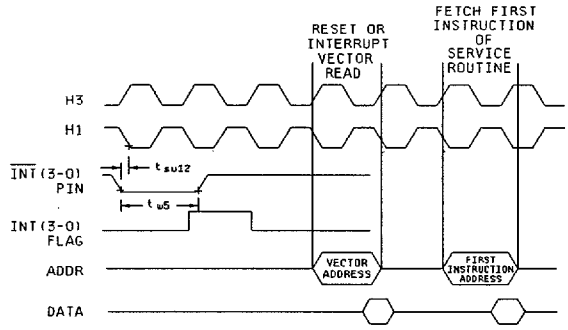
FIGURE 4. Switching waveforms and test circuit - continued.



NOTES:
1. RESET is asynchronous input and can be asserted at any point during a clock cycle. If the specified timings are met, the exact sequence shown will occur; otherwise, an additional delay of one clock cycle may occur.
2. Note that the R/$\overline{W}$ outputs are placed in a high impedance state during reset and can be provided with a resitive pull-up, nominally 20 KΩ, if desirable spurious writes could be caused when these outputs go low.
3. (X)D includes D(31-0) and XD(31-0).
4. (X)A includes A(23-0), XA(12-0).
5. Control signals include $\overline{STRB}$, $\overline{MSTRB}$, and $\overline{TOSTRB}$.
6. Asynchronously reset signals include XF1, XF0, CLKX0, DX0, FSX0, CLKR0, DR0, FSR0, CLKX1, DX1, FSX1, CLKR1, DR1, FSR1, TCLK0, and TCLK1.

FIGURE 4. Switching waveforms and test circuit - continued.

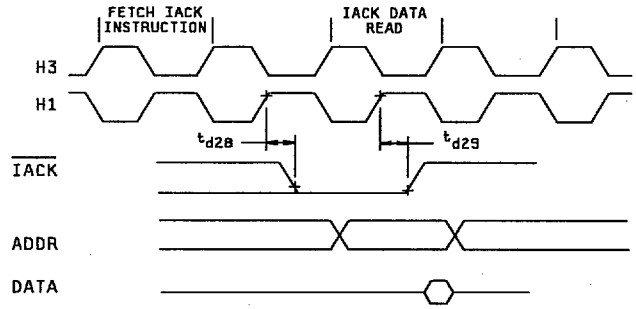
$\overline{\text{INT}}$(3-0) response timing



NOTES:

7. Interrupt pulse width must be at least 1 P wide to guarantee it will be seen. It must be less than 2 P wide to guarantee it will be responded to only once. The recommended pulse width is 1.5 P.
8. INT is an asynchronous input and can be asserted at any point during a clock cycle. If the specified timings are met, the exact sequence shown will occur; otherwise, an additional delay of one clock cycle may occur.

$\overline{\text{IACK}}$ timing

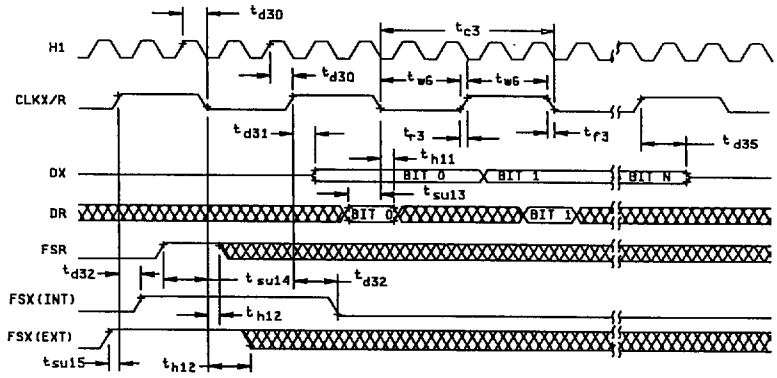


NOTE:

9. The IACK output is active for the entire duration of the bus cycle and is therefore extended if the bus cycle utilizes wait states.

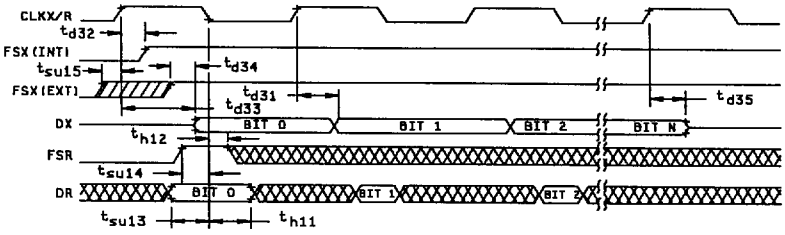
FIGURE 4. Switching waveforms and test circuit - Continued.

Fixed data rate mode



NOTES:
10. Timing diagrams show operations with CLKXP = CLKRP = FSXP = FSRP = 0.
11. These timings are valid for all serial port modes, including handshake, except where otherwise indicated.

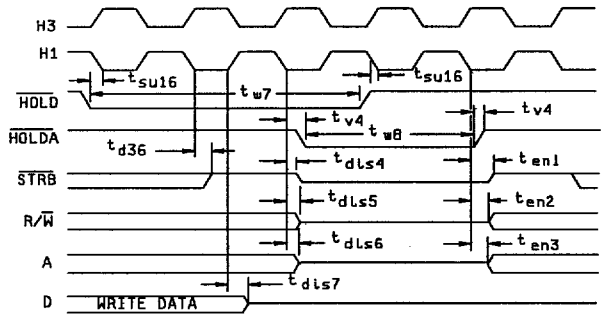
Variable data rate mode



NOTES:
12. Timing diagrams show operation with CLKXP = CLKRP = FSXP = FSRP = 0.
13. Timings not expressly specified for variable data rate mode are the same as those for fixed data rate mode.
14. Timings are valid for all serial port modes, including handshake mode, except where otherwise indicated.

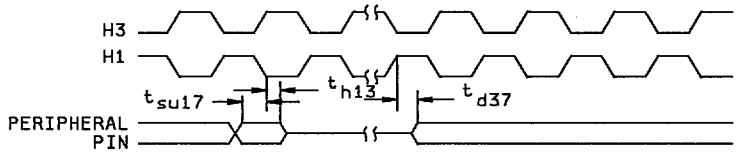
FIGURE 4. Switching waveforms and test circuit - Continued.

$\overline{\text{HOLD}}/\overline{\text{HOLDA}}$ timing



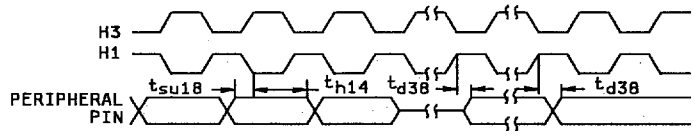
NOTE 15: $\overline{\text{HOLD}}$ is an asynchronous input and can be asserted at any point during a clock cycle. If the specified timings are met, the exact sequence shown will occur; otherwise, an additional delay of one clock cycle may occur.

Peripheral pin general-purpose I/O timing



NOTE 16: Peripheral pins include CLKX0/1, CLKR0/1, DX0/1, DR0/1, FSX0/1, FSR0/1, and TCLK0/1. The modes of these pins are defined by the contents of internal control registers associated with each peripheral.

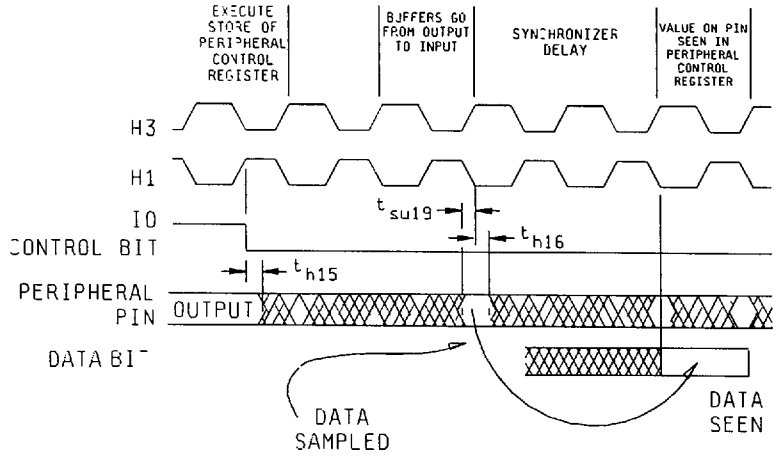
Timer pin timings



NOTE 17: Period and polarity of valid logic level are specified by contents of internal control registers.

FIGURE 4. Switching waveforms and test circuit - continued.

Change of peripheral pin from general purpose output to input mode



Change of peripheral pin from general-purpose input to output mode

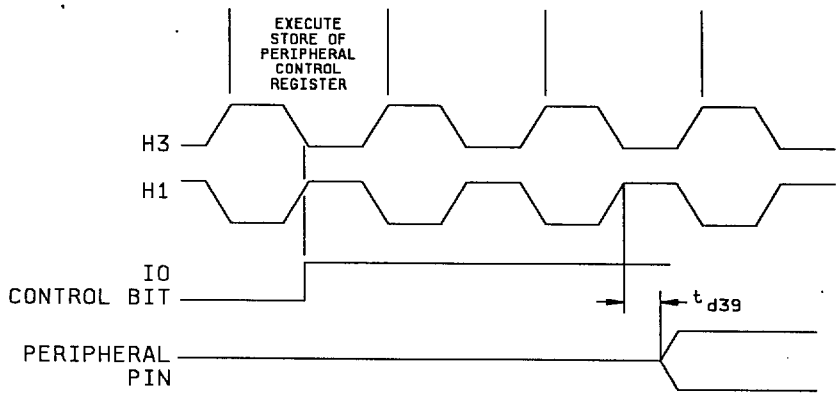


FIGURE 4. Switching waveforms and test circuit - Continued.

4. QUALITY ASSURANCE PROVISIONS

4.1 Sampling and inspection. For device classes Q and V, sampling and inspection procedures shall be in accordance with MIL-PRF-38535 and Appendix F of MIL-PRF-38535, or as modified in the device manufacturer's Quality Management (QM) plan. The modification in the QM plan shall not affect the form, fit, or function as described herein. For device class M, sampling and inspection procedures shall be in accordance with MIL-PRF-38535, appendix A and Appendix F of MIL-PRF-38535.

4.2 Screening. For device classes Q and V, screening shall be in accordance with MIL-PRF-38535, and Appendix F of MIL-PRF-38535 and shall be conducted on all devices prior to qualification and technology conformance inspection. For device class M, screening shall be in accordance with method 5004 of MIL-STD-883, and Appendix F of MIL-PRF-38535, and shall be conducted on all devices prior to quality conformance inspection.

4.2.1 Additional criteria for device class M.

a. Burn-in test, method 1015 of MIL-STD-883.

(1) Test condition A or D. The test circuit shall be maintained by the manufacturer under document revision level control and shall be made available to the preparing or acquiring activity upon request. The test circuit shall specify the inputs, outputs, biases, and power dissipation, as applicable, in accordance with the intent specified in test method 1015.

(2) T_A = +125°C, minimum.

b. Interim and final electrical test parameters shall be as specified in table II herein.

4.2.2 Additional criteria for device classes Q and V.

a. The burn-in test duration, test condition and test temperature, or approved alternatives shall be as specified in the device manufacturer's QM plan in accordance with MIL-PRF-38535. The burn-in test circuit shall be maintained under document revision level control of the device manufacturer's Technology Review Board (TRB) in accordance with MIL-PRF-38535 and shall be made available to the acquiring or preparing activity upon request. The test circuit shall specify the inputs, outputs, biases, and power dissipation, as applicable, in accordance with the intent specified in test method 1015 of MIL-STD-883.

b. Interim and final electrical test parameters shall be as specified in table II herein.

c. Additional screening for device class V beyond the requirements of device class Q shall be as specified in MIL-PRF-38535, appendix B.

4.3 Qualification inspection for device classes Q and V. Qualification inspection for device classes Q and V shall be in accordance with MIL-PRF-38535. Inspections to be performed shall be those specified in MIL-PRF-38535 and herein for groups A, B, C, D, and E inspections (see 4.4.1 through 4.4.4).

4.4 Conformance inspection. Technology conformance inspection for classes Q and V shall be in accordance with MIL-PRF-38535 and Appendix F of MIL-PRF-38535 including groups A, B, C, D, and E inspections and as specified herein except where option 2 of MIL-PRF-38535 permits alternate in-line control testing. Quality conformance inspection for device class M shall be in accordance with MIL-PRF-38535, appendix A, Appendix F of MIL-PRF-38535. and as specified herein. Inspections to be performed for device class M shall be those specified in method 5005 of MIL-STD-883 and herein for groups A, B, C, D, and E inspections (see 4.4.1 through 4.4.4).

4.4.1 Group A inspection.

a. Tests shall be as specified in table II herein.

b. Subgroup 4 (C_{IN}, C_{OUT} and C_X measurements) shall be measured only for the initial test and after process or design changes which may affect capacitance. A minimum sample size of five devices with zero rejects shall be required.

c. Subgroups 5 and 6 in table I, method 5005 of MIL-STD-883 shall be omitted.

d. For device class M, subgroups 7 and 8 tests shall be sufficient to verify the functionality of the device. For device classes Q and V, subgroups 7 and 8 shall include verifying the functionality of the device; these tests shall have been fault graded in accordance with MIL-STD-883, test method 5012 (see 1.5 herein).

4.4.2 Group B inspection.

a. Attachability is not a requirement of Case outlines T and M.

b. For Case outlines T and M bond strength (method 2011) shall not be less than 30 g.

c. For Case outlines T and M constant acceleration in accordance with Method 2001 test condition E, Y1 direction, is required. 4 devices are to be tested with zero failures.

TABLE II. Electrical test requirements.

Test requirements	Subgroups (in accordance with MIL-STD-883, method 5005, table I)	Subgroups (in accordance with MIL-PRF-38535, table III)	
	Device class M	Device class Q	Device class V
Interim electrical parameters (see 4.2)	- - - -	- - -	- - -
Final electrical parameters (see 4.2)	1, 2, 3, 7, 8 1/ 9, 10, 11	1, 2, 3, 7, 8 1/ 9, 10, 11	1, 2, 3, 7, 8, 9, 10, 11 2/
Group A test requirements (see 4.4)	1, 2, 3, 4, 7, 8, 9, 10, 11	1, 2, 3, 4, 7, 8, 9, 10, 11	1, 2, 3, 4, 7, 8, 9, 10, 11
Group C end-point electrical parameters (see 4.4)	2, 8a, 10	2, 8a, 10	2, 8a, 10
Group D end-point electrical parameters (see 4.4)	2, 8a, 10	2, 8a, 10	2, 8a, 10
Group E end-point electrical parameters (see 4.4)	2, 8a, 10	2, 8a, 10	2, 8a, 10

1/ PDA applies to subgroup 1.
2/ PDA applies to subgroups 1 and 7.

4.4.3 Group C inspection. The group C inspection end-point electrical parameters shall be as specified in table II herein.

4.4.3.1 Additional criteria for device class M. Steady-state life test conditions, method 1005 of MIL-STD-883:

a. Test condition A or D. The test circuit shall be maintained by the manufacturer under document revision level control and shall be made available to the preparing or acquiring activity upon request. The test circuit shall specify the inputs, outputs, biases, and power dissipation, as applicable, in accordance with the intent specified in test method 1005 of MIL-STD-883.

b. T_A = +125° C, minimum.

c. Test duration: 1,000 hours, except as permitted by method 1005 of MIL-STD-883.

4.4.3.2 Additional criteria for device classes Q and V. The steady-state life test duration, test condition and test temperature, or approved alternatives shall be as specified in the device manufacturer's QM plan in accordance with MIL-PRF-38535. The test circuit shall be maintained under document revision level control by the device manufacturer's TRB in accordance with MIL-PRF-38535 and shall be made available to the acquiring or preparing activity upon request. The test circuit shall specify the inputs, outputs, biases, and power dissipation, as applicable, in accordance with the intent specified in test method 1005 of MIL-STD-883.

4.4.4 Group D inspection. The group D inspection end-point electrical parameters shall be as specified in table II herein.

4.4.5 Group E inspection. Group E inspection is required only for parts intended to be marked as radiation hardness assured (see 3.5 herein).

a. End-point electrical parameters shall be as specified in table II herein.

b. For device classes Q and V, the devices or test vehicle shall be subjected to radiation hardness assured tests as specified in MIL-PRF-38535 for the RHA level being tested. For device class M, the devices shall be subjected to radiation hardness assured tests as specified in MIL-PRF-38535, appendix A for the RHA level being tested. All device classes must meet the postirradiation end-point electrical parameter limits as defined in table I at T_A = +25° C ±5° C, after exposure, to the subgroups specified in table II herein.

c. When specified in the purchase order or contract, a copy of the RHA delta limits shall be supplied.

5. PACKAGING

5.1 Packaging requirements. The requirements for packaging shall be in accordance with MIL-PRF-38535 for device classes Q and V or MIL-PRF-38535, appendix A for device class M.

6. NOTES

6.1 Intended use. Microcircuits conforming to this drawing are intended for use for Government microcircuit applications (original equipment), design applications, and logistics purposes.

6.1.1 Replaceability. Microcircuits covered by this drawing will replace the same generic device covered by a contractor-prepared specification or drawing.

6.1.2 Substitutability. Device class Q devices will replace device class M devices.

6.2 Configuration control of SMD's. All proposed changes to existing SMD's will be coordinated with the users of record for the individual documents. This coordination will be accomplished in accordance with MIL-STD-973 using DD Form 1692, Engineering Change Proposal.

6.3 Record of users. Military and industrial users should inform Defense Supply Center Columbus when a system application requires configuration control and which SMD's are applicable to that system. DSCC will maintain a record of users and this list will be used for coordination and distribution of changes to the drawings. Users of drawings covering microelectronic devices (FSC 5962) should contact DSCC-VA, telephone (614) 692-0525.

6.4 Comments. Comments on this drawing should be directed to DSCC-VA , Columbus, Ohio 43216-5000, or telephone (614) 692-0674.

6.5 Abbreviations, symbols, and definitions. The abbreviations, symbols, and definitions used herein are defined in MIL-PRF-38535 and MIL-HDBK-1331 and as follows:

PIN		I/O/Z	Description
Name	Numbers	1/	Primary bus interface
D31-D0	32	I/O/Z	32-bit data port of the primary bus interface.
A23-A0	24	O/Z	24-bit address port of the primary bus interface.
R/$\overline{W}$	1	O/Z	Read/write signal for primary bus interface. This pin is high when a read is performed and low when a write is performed over the parallel interface.
$\overline{STRB}$	1	O/Z	External access strobe for the primary bus interface.
$\overline{RDY}$	1	I	Ready signal. This pin indicates that the external device is prepared for a primary bus interface transaction to complete. As long as RDY is a logic high, the data and address buses of the primary bus interface remain valid.
$\overline{HOLD}$	1	I	Hold signal for primary bus interface. When HOLD is a logic low, any ongoing transaction is completed. The A23-A0, D31-D0, STRB, and R/W signals are placed in a high-impedance state, and all transactions over the primary bus interface are held until HOLD becomes a logic high.
$\overline{HOLDA}$	1	O	Hold acknowledge signal for primary bus interface. This signal is generated in response to a logic low on HOLD. It signals that A23-A0, D31-D0, STRB, and R/W are placed in a high-impedance state and that all transactions over the bus will be held. HOLDA will be high in response to a logic high of HOLD.

6.5 Symbols, definitions, and functional descriptions - Continued.

PIN Name	PIN Numbers	I/O/Z 1/	Description Expansion bus interface
		Expansion bus interface	
XD31-XD0	32	I/O/Z	32-bit data port of the expansion bus interface.
XA12-XA0	13	O/Z	13-bit address port of the expansion bus interface.
XR/W	1	O/Z	Read/write signal for expansion bus interface. When a read is performed, this pin is held high; when a write is performed, this pin is low.
$\overline{\text{MSTRB}}$	1	O	External memory access strobe for the expansion bus interface.
$\overline{\text{IOSTRB}}$	1	O	External I/O access strobe for the expansion bus interface.
$\overline{\text{XRDY}}$	1	I	Ready signal. This pin indicates that the external device is prepared for an expansion bus interface transaction to complete. As long as XRDY is high, the data and address buses of the expansion bus interface remain valid.
		Control signals	
$\overline{\text{RESET}}$	1	I	Reset. When this pin is a logic low, the device is placed in the reset condition. When RESET becomes a logic high, execution begins from the location specified by the reset vector.
$\overline{\text{INT3}}$-$\overline{\text{INT0}}$	4	I	External interrupts.
$\overline{\text{IACK}}$	1	O	Interrupt acknowledge signal. IACK is set to 1 by the IACK instruction. This can be used to indicate the beginning or end of an interrupt service routine.
$\overline{\text{MC}}$/MP	1	I	Microcomputer/microprocessor mode pin.
XF1, XF0	2	I/O	External flag pins. They are used as general-purpose I/O pins or to support interlocked processor instructions.
		Serial port 0 signals	
CLKX0	1	I/O	Serial port 0 transmit clock. This pin serves as the serial shift clock for the serial port 0 transmitter.
DX0	1	O/Z	Data transmit output. Serial port 0 transmits serial data on this pin.
FSX0	1	I/O	Frame synchronization pulse for transmit. The FSX0 pulse initiates the transmit data process over pin DX0.
CLKR0	1	I/O	Serial port 0 receive clock. This pin serves as the serial shift clock for the serial port 0 transmitter.
DR0	1	I	Data receive. Serial port 0 receives serial data via the DR0 pin.
FSR0	1	I	Frame synchronization pulse for receive. The FSR0 pulse initiates the receive data process over DR0.

PIN Name	PIN Numbers	I/O/Z 1/	Description
			Serial port 1 signals
CLKX1	1	I/O	Serial port 1 transmit clock. This pin serves as the serial shift clock for the serial port 1 transmitter.
DX1	1	O/Z	Data transmit output. Serial port 1 transmits serial data on this pin.
FSX1	1	I/O	Frame synchronization pulse for transmit. The FSX1 pulse initiates the transmit data process over pin DX1.
CLKR1	1	I/O	Serial port 1 receive clock. This pin serves as the serial shift clock for the serial port 1 receiver.
DR1	1	I	Data receive. Serial port 1 receives serial data via the DR1 pin.
FSR1	1	I	Frame synchronization pulse for receive. The FSR1 pulse initiates the receive data process over DR1.
			Timer 0 signals
TCLKO	1	I/O	Timer clock. As an input, TCLK0 is used by timer 0 to count external pulses. As an output pin, TCLK0 outputs pulses generated by timer 0.
			Timer 1 signals
TCLK1	1	I/O	Timer clock. As an input, TCLK1 is used by timer 1 to count external pulses. As an output pin, TCLK1 outputs pulses generated by timer 1.
			Supply and oscillator signals 2/
V_{DD}	4/8	I	+5 V supply pin.
$IODV_{DD}$	2/3	I	+5 V supply pin.
ADV_{DD}	2/3	I	+5 V supply pin.
PDV_{DD}	1/2	I	+5 V supply pin.
DDV_{DD}	2/2	I	+5 V supply pin.
MDV_{DD}	1/2	I	+5 V supply pin.
V_{SS}	4/8	I	Ground pin.
DV_{SS}	4/4	I	Ground pin.
CV_{SS}	2/4	I	Ground pin.
IV_{SS}	1/2	I	Ground pin.
V_{BBP}	1/1	NC	V_{BB} pump oscillator output.

See footnotes at end of table.

6.5 Symbols, definitions, and functional descriptions - Continued.

PIN Name	PIN Numbers	I/O/Z 1/	Description Supply and oscillator signals 2/
V_{SUBS}	1/2	I	Substrate pin. Tie to ground.
X1	1	O	Output pin from the internal oscillator for the crystal. If a crystal is not used, this pin should be left unconnected.
X2/CLKIN	1	I	Input pin to the internal oscillator from the crystal or a clock.
H1	1	O	External H1 clock. This clock has a period equal to twice CLKIN.
H3	1	O	External H3 clock. This clock has a period equal to twice CLKIN.
Reserved			
EMU0-EMU2	3	I	Reserved. Use pullups to +5 volts.
EMU3	1	O	Reserved.
EMU4	1	I	Reserved. Use pullups to +5 volts.
EMU5,EMU6	2	NC	Reserved.
RSV0-RSV10	11	I	Reserved. Use pullups to +5 volts.

1/ I = input, O = output, Z = high impedance state.

2/ Case X and Y power pins.

6.6 Sources of supply.

6.6.1 Sources of supply for device classes Q and V. Sources of supply for device classes Q and V are listed in QML-38535. The vendors listed in QML-38535 have submitted a certificate of compliance (see 3.6 herein) to DSCC-VA and have agreed to this drawing.

6.6.2 Approved sources of supply for device class M. Approved sources of supply for class M are listed in MIL-HDBK-103. The vendors listed in MIL-HDBK-103 have agreed to this drawing and a certificate of compliance (see 3.6 herein) has been submitted to and accepted by DSCC-VA.

STANDARD MICROCIRCUIT DRAWING BULLETIN

DATE: 97-12-01

Approved sources of supply for SMD 5962-90526 are listed below for immediate acquisition information only and shall be added to MIL-HDBK-103 and QML-38535 during the next revision. MIL-HDBK-103 and QML-38535 will be revised to include the addition or deletion of sources. The vendors listed below have agreed to this drawing and a certificate of compliance has been submitted to and accepted by DSCC-VA. This bulletin is superseded by the next dated revision of MIL-HDBK-103 and QML-38535.

Standard microcircuit drawing PIN 1/	Vendor CAGE number	Vendor similar PIN 2/
5962-9052601MUX	3/	SMJ320C30HFGM28
5962-9052601MXX	3/	SMJ320C30GBM28
5962-9052601MYX	3/	SMJ320C30HUM28
5962-9052601MZX	3/	SMJ320C30HTM28
5962-9052602MUX	3/	SMJ320C30HFGM25
5962-9052602MXX	3/	SMJ320C30GBM25
5962-9052602MYX	3/	SMJ320C30HUM25
5962-9052602MZX	3/	SMJ320C30HTM25
5962-9052603MXA	3/	SMJ320C30GBM33
5962-9052603MUA	3/	SMJ320C30HFGM33
5962-9052603QTC	3/	SMJ320C30TAM33
5962-9052603QMC	3/	SMJ320C30TBM33
5962-9052604MXA	01295	SMJ320C30GBM40
5962-9052604MUA	01295	SMJ320C30HFGM40
5962-9052605MXA	01295	SMJ320C30GBM50

1/ The lead finish shown for each PIN representing a hermetic package is the most readily available from the manufacturer listed for that part. If the desired lead finish is not listed contact the Vendor to determine its availability.

2/ Caution. Do not use this number for item acquisition. Items acquired to this number may not satisfy the performance requirements of this drawing.

3/ Not available fron an approved source of supply.

Vendor CAGE number	Vendor name and address
01295	Texas Instruments, Incorporated 13500 North Central Expressway P.O. Box 655303 Dallas, TX 75265

The information contained herein is disseminated for convenience only and the Government assumes no liability whatsoever for any inaccuracies in the information bulletin.