REVISIONS			
LTR	DESCRIPTION	DATE (YR-MO-DA)	APPROVED

REV																			
SHEET																			
REV																			
SHEET	15	16	17	18	19	20	21	22	23	24	25	26	27	28	29				
REV STATUS OF SHEETS				REV															
				SHEET			1	2	3	4	5	6	7	8	9	10	11	12	13	14

PMIC N/A

STANDARDIZED MILITARY DRAWING

THIS DRAWING IS AVAILABLE FOR USE BY ALL DEPARTMENTS AND AGENCIES OF THE DEPARTMENT OF DEFENSE

AMSC N/A

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DRAWING APPROVAL DATE
92-09-29

REVISION LEVEL

DEFENSE ELECTRONICS SUPPLY CENTER
DAYTON, OHIO 45444

MICROCIRCUIT, CMOS, PROGRAMMABLE DMA CONTROLLER, MONOLITHIC SILICON

SIZE	CAGE CODE	5962-90543
A	67268	

SHEET 1 OF 29

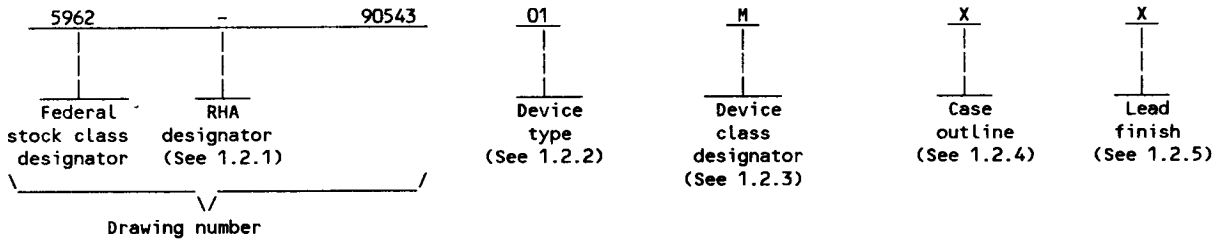
DESC FORM 193
JUL 91

5962-E534-92

1. SCOPE

1.1 Scope. This drawing forms a part of a one part - one part number documentation system (see 6.6 herein). Two product assurance classes consisting of military high reliability (device classes B, Q, and M) and space application (device classes S and V), and a choice of case outlines and lead finishes are available and are reflected in the Part or Identifying Number (PIN). Device class M microcircuits represent non-JAN class B microcircuits in accordance with 1.2.1 of MIL-STD-883, "Provisions for the use of MIL-STD-883 in conjunction with compliant non-JAN devices". When available, a choice of radiation hardness assurance (RHA) levels are reflected in the PIN.

1.2 PIN. The PIN shall be as shown in the following example:



1.2.1 Radiation hardness assurance (RHA) designator. Device classes M, B, and S RHA marked devices shall meet the MIL-M-38510 specified RHA levels and shall be marked with the appropriate RHA designator. Device classes Q and V RHA marked devices shall meet the MIL-I-38535 specified RHA levels and shall be marked with the appropriate RHA designator. A dash (-) indicates a non-RHA device.

1.2.2 Device type(s). The device type(s) shall identify the circuit function as follows:

Device type	Generic number	Circuit function
01	82C37A-5	5 MHz programmable DMA controller
02	82C37A	8 MHz programmable DMA controller
03	82C37A-12	12.5 MHz programmable DMA controller
04	82C237	8 MHz programmable DMA controller
05	82C237-12	12.5 MHz programmable DMA controller

1.2.3 Device class designator. The device class designator shall be a single letter identifying the product assurance level as follows:

Device class	Device requirements documentation
M	Vendor self-certification to the requirements for non-JAN class B microcircuits in accordance with 1.2.1 of MIL-STD-883
B or S	Certification and qualification to MIL-M-38510
Q or V	Certification and qualification to MIL-I-38535

1.2.4 Case outline. The case outlines shall be designated in MIL-STD-1835 and as follows:

Outline letter	Descriptive designator	Terminals	Package style
Q	GDIP1-T40	40	Dual-in-line
X	CQCC1-N44	44	Square leadless chip carrier

1.2.5 Lead finish. The lead finish shall be as specified in MIL-M-38510 for classes M, B, and S or MIL-I-38535 for classes Q and V. Finish letter "X" shall not be marked on the microcircuit or its packaging. The "X" designation is for use in specifications when lead finishes A, B, and C are considered acceptable and interchangeable without preference.

1.3 Absolute maximum ratings.

Supply voltage (referenced to ground)	+8.0 V dc maximum
Input, output, or I/O voltage applied range	GND -0.5 V dc to V_{CC} +0.5 V dc
Storage temperature range	-65°C to +150°C
Power dissipation (P_D) 1/	1.0 W maximum
Lead temperature (soldering, 10 seconds)	275°C
Junction temperature (T_J)	+150°C maximum
Thermal resistance, junction-to-case (Θ_{JC})	See MIL-STD-1835

1.4 Recommended operating conditions.

Case operating temperature range	-55°C to +125°C
Supply voltage range (V_{CC})	+4.5 V dc to +5.5 V dc

1.5 Digital testing for device classes Q and V.

Fault coverage measurement of manufacturing logic tests (MIL-STD-883, test method 5012)	XX percent 2/

2. APPLICABLE DOCUMENTS

2.1 Government specifications, standards, bulletin, and handbook. Unless otherwise specified, the following specifications, standards, bulletin, and handbook of the issue listed in that issue of the Department of Defense Index of Specifications and Standards specified in the solicitation, form a part of this drawing to the extent specified herein.

SPECIFICATIONS

MILITARY

MIL-M-38510 - Microcircuits, General Specification for.
MIL-I-38535 - Integrated Circuits, Manufacturing, General Specification for.

STANDARDS

MILITARY

MIL-STD-480 - Configuration Control-Engineering Changes, Deviations and Waivers.
MIL-STD-883 - Test Methods and Procedures for Microelectronics.
MIL-STD-1835 - Microcircuit Case Outlines.

BULLETIN

MILITARY

MIL-BUL-103 - List of Standardized Military Drawings (SMD's).

HANDBOOK

MILITARY

MIL-HDBK-780 - Standardized Military Drawings.

(Copies of the specifications, standards, bulletin, and handbook required by manufacturers in connection with specific acquisition functions should be obtained from the contracting activity or as directed by the contracting activity.)

2.2 Order of precedence. In the event of a conflict between the text of this drawing and the references cited herein, the text of this drawing shall take precedence.

1/ Power dissipation based on package heat transfer limitations, not device power consumption.
2/ Values will be added when they become available.

3. REQUIREMENTS

3.1 Item requirements. The individual item requirements for device class M shall be in accordance with 1.2.1 of MIL-STD-883, "Provisions for the use of MIL-STD-883 in conjunction with compliant non-JAN devices" and as specified herein. The individual item requirements for device classes B and S shall be in accordance with MIL-M-38510 and as specified herein. For device classes B and S, a full electrical characterization table for each device type shall be included in this SMD when a qualified source exists. The individual item requirements for device classes Q and V shall be in accordance with MIL-I-38535 and as specified herein.

3.2 Design, construction, and physical dimensions. The design, construction, and physical dimensions shall be as specified in MIL-M-38510 for device classes M, B, and S and MIL-I-38535 for device classes Q and V and herein.

3.2.1 Case outlines. The case outlines shall be in accordance with 1.2.4 herein.

3.2.2 Terminal connections. The terminal connections shall be as specified on figure 1.

3.2.3 Functional block diagram. The functional block diagram shall be as specified on figure 2.

3.3 Electrical performance characteristics and postirradiation parameter limits. Unless otherwise specified herein, the electrical performance characteristics and postirradiation parameter limits are as specified in table I and shall apply over the full case operating temperature range.

3.4 Electrical test requirements. The electrical test requirements shall be the subgroups specified in table IIA. The electrical tests for each subgroup are defined in table I.

3.5 Marking. The part shall be marked with the PIN listed in 1.2 herein. Marking for device class M shall be in accordance with MIL-STD-883 (see 3.1 herein). In addition, the manufacturer's PIN may also be marked as listed in MIL-BUL-103. Marking for device classes B and S shall be in accordance with MIL-M-38510. Marking for device classes Q and V shall be in accordance with MIL-I-38535.

3.5.1 Certification/compliance mark. The compliance mark for device class M shall be a "C" as required in MIL-STD-883 (see 3.1 herein). The certification mark for device classes B and S shall be a "J" or "JAN" as required in MIL-M-38510. The certification mark for device classes Q and V shall be a "QML" as required in MIL-I-38535.

3.6 Certificate of compliance. For device class M, a certificate of compliance shall be required from a manufacturer in order to be listed as an approved source of supply in MIL-BUL-103 (see 6.7.3 herein). For device classes Q and V, a certificate of compliance shall be required from a QML-38535 listed manufacturer in order to supply to the requirements of this drawing (see 6.7.2 herein). The certificate of compliance submitted to DESC-ECC prior to listing as an approved source of supply for this drawing shall affirm that the manufacturer's product meets, for device class M, the requirements of MIL-STD-883 (see 3.1 herein), or for device classes Q and V, the requirements of MIL-I-38535 and the requirements herein.

3.7 Certificate of conformance. A certificate of conformance as required for device class M in MIL-STD-883 (see 3.1 herein) or device classes B and S in MIL-M-38510 or for device classes Q and V in MIL-I-38535 shall be provided with each lot of microcircuits delivered to this drawing.

3.8 Notification of change for device class M. For device class M, notification to DESC-ECC of change of product (see 6.2 herein) involving devices acquired to this drawing is required for any change as defined in MIL-STD-480.

3.9 Verification and review for device class M. For device class M, DESC, DESC's agent and the acquiring activity retain the option to review the manufacturer's facility and applicable required documentation. Offshore documentation shall be made available onshore at the option of the reviewer.

3.10 Microcircuit group assignment for device classes M, B, and S. Device classes M, B, and S devices covered by this drawing shall be in microcircuit group number 105 (see MIL-M-38510, appendix E).

3.11 Serialization for device class S. All device class S devices shall be serialized in accordance with MIL-M-38510.

TABLE I. Electrical performance characteristics.

Test	Symbol	Conditions $-55°C \le T_C \le +125°C$ 1/ unless otherwise specified	Group A subgroups	Device type	Limits Min	Limits Max	Unit
Input high voltage	V_{IH}	V_{CC} = 5.5 V	1,2,3	All	2.2		V
Input low voltage	V_{IL}	V_{CC} = 4.5 V				0.8	
High level output voltage	V_{OH}	V_{CC} = 4.5 V, 2/ I_{OH} = -2.5 mA			3.0		
		V_{CC} = 4.5 V, 2/ I_{OH} = -100 µA			V_{CC} -0.4		
Low level output voltage	V_{OL}	V_{CC} = 4.5 V, 2/ I_{OL} = 3.2 mA for EOP I_{OL} = 2.5 mA for all other output pins				0.40	
Input leakage current	I_I	V_{CC} = 5.5 V V_{IN} = V_{CC} or GND			-1.0	+1.0	µA
I/O and output leakage current	I_O	V_{CC} = 5.5 V V_{OUT} = V_{CC} or GND			-10	+10	
Standby supply current	I_{CCSB}	V_{CC} = 5.5 V V_{IN} = V_{CC} or GND, outputs open				10	
Operating supply current	I_{CCOP}	V_{CC} = 5.5 V, f = maximum V_{IN} = V_{CC} or GND, outputs open				2	mA/MHz
Input capacitance	C_I	f = 1 MHz, T_C = 25°C, All measurements are referenced to device ground. See 4.4.1c.	4			25	pF
Output capacitance	C_O					40	
I/O capacitance	$C_{I/O}$					25	
Functional test		V_{CC} = 4.5 V and 5.5 V, 3/ See 4.4.1d.	7,8				

See footnotes at end of table.

TABLE I. Electrical performance characteristics - Continued.

Test	Symbol	Conditions $-55°C \le T_C \le +125°C$ 1/ unless otherwise specified	Group A subgroups	Device type	Limits		Unit
					Min	Max	
AEN high from CLK low (S1) delay time	1	DMA master mode See figure 3	9,10,11	01 02,04 03,05		175 105 50	ns
AEN low from CLK high (S1) delay time	2			01 02,04 03,05		130 80 50	
ADR active to float 4/ delay from CLK high	3			01 02,04 03,05		90 55 55	
READ or WRITE float 4/ delay from CLK high	4			01 02,04 03,05		120 75 50	
DB active to float 4/ delay from CLK high	5			01 02,04 03,05		170 135 90	
ADR from READ high hold time	6			01 02,04 03,05	TCY-100 TCY-75 TCY-65		
DB from ADSTB low hold time	7			All	TCL-18		
ADR from WRITE high hold time	8			01 02,04 03,05	TCY-65 TCY-65 TCY-50		
DACK valid from CLK low delay time	9			01 02,04 03,05		170 105 69	
EOP high from CLK high delay time	9			01 02,04 03,05		170 105 90	
EOP low from CLK high delay time	9			01 02,04 03,05		100 60 35	
ADR stable from CLK high	10			01 02,04 03,05		110 60 50	
DB to ADSTB low setup time	11			ALL	TCH-20		
Clock high time (transitions 10 ns)	12			01 02,04 03,05	70 55 30		

See footnotes at end of table.

TABLE I. Electrical performance characteristics - Continued.

Test	Symbol	Conditions $-55°C \le T_C \le +125°C$ 1/ unless otherwise specified	Group A subgroups	Device type	Limits		Unit
					Min	Max	
Clock low time (transitions 10 ns)	13	DMA master mode See figure 3	9,10,11	01 02,04 03,05	50 43 30		ns
CLK cycle time	14			01 02,04 03,05	200 125 80		
CLK high to READ or WRITE low delay	15			01 02,04 03,05		190 130 120	
READ high from CLK high (S4) delay time	16			01 02,04 03,05		190 115 80	
WRITE high from CLK high (S4) delay time	17			01 02,04 03,05		130 80 70	
HRQ valid from CLK high delay time	18			01 02,04 03,05		120 75 30	
EOP hold time from CLK low (S2)	19			01 02,04 03,05	90 90 50		
EOP low to CLK low setup time	20			01 02,04 03,05	40 25 0		
EOP pulse width high delay time	21			01 02,04 03,05	220 135 50		
ADR valid delay from CLK high	22			01 02,04 03,05		110 60 50	
READ or WRITE active from CLK high	23			01 02,04 03,05		150 90 50	
DB valid delay from CLK high	24			01 02,04 03,05		110 60 45	
HLDA valid to CLK high setup time	25			01 02,04 03,05	75 45 10		
Input data from MEMR high hold time	26			All	0		

See footnotes at end of table.

TABLE I. Electrical performance characteristics - Continued.

Test	Symbol	Conditions $-55°C \le T_C \le +125°C$ 1/ unless otherwise specified	Group A subgroups	Device type	Limits		Unit
					Min	Max	
Input data to MEMR high setup time	27	DMA master mode See figure 3	9,10,11	01 02,04 03,05	155 90 45		ns
Output data from MEMW high hold time	28			01 02,04 03,05	15 15 TCY-50		
Output data valid to MEMW high	29			01 02,04 03,05	TCY-35 TCY-35 TCY-10		
DREQ to CLK low (S1,S4) setup time	30			All	0		
CLK to READY low hold time	31			01 02,04 03,05	20 20 10		
READY to CLK low setup time	32			01 02,04 03,05	60 35 15		
ADSTB high from CLK low delay time	33			01 02,04 03,05		80 70 70	
ADSTB low from CLK low delay time	34			01 02,04 03,05		120 120 60	
READ high delay from WRITE high	35			01 02,04 03,05	0 0 5		
READ pulse width, normal timing	36			01 02,04 03,05	2TCY-60 2TCY-60 2TCY-55		
ADSTB pulse width	37			01 02,04 03,05	TCY-80 TCY-50 TCY-35		
Extended WRITE pulse width	38			01 02,04 03,05	2TCY-100 2TCY-85 2TCY-80		
WRITE pulse width	39			01 02,04 03,05	TCY-100 TCY-85 TCY-80		

See footnotes at end of table.

TABLE I. Electrical performance characteristics - Continued.

Test	Symbol	Conditions $-55°C \le T_C \le +125°C$ 1/ unless otherwise specified	Group A subgroups	Device type	Limits		Unit
					Min	Max	
READ pulse width, compressed	40	DMA master mode See figure 3	9,10,11	01 02,04 03,05	TCY-60 TCY-60 TCY-55		ns
DB float delay from 4/ READ high	47			01 02,04 03,05	5 5 5	85 85 55	
ADR valid to READ low	56			All	17		
ADR valid to WRITE low	57			All	7		
READ high to AEN low	58			All	15		
READ high to ADSTB high	59			All	13		
WRITE high to ADSTB high	60			All	15		
DACK valid to READ low	61			All	25		
DACK valid to WRITE low	62			All	25		
READ high to DACK inactive	63			All	12		
ADR float to READ low 4/	64			All	- 2.5		
Output enable valid before WRITE high	65			01 02,03 04,05	5/ 5/ TCY+20		
Output enable hold time from WRITE high	66			01 02,03 04,05	5/ 5/ TCY-50		
ADR valid or CS low to READ low	41	Peripheral slave mode See figure 3	9,10,11	01 02,04 03,05	10 10 0		
ADR valid to WRITE low setup time	42			All	0		

See footnotes at end of table.

TABLE I. Electrical performance characteristics - Continued.

Test	Symbol	Conditions $-55°C \le T_C \le +125°C$ 1/ unless otherwise specified	Group A subgroups	Device type	Limits		Unit
					Min	Max	
CS low to WRITE low setup time	43	Peripheral slave mode See figure 3	9,10,11	All	0		ns
Data valid to WRITE high setup time	44			01 02,04 03,05	150 100 60		
ADR or CS hold from READ high	45	Peripheral slave mode See figure 3	9,10,11	All	0		
Data access from READ	46			01 02,04 03,05		140 120 80	
RESET to first IOR or IOW	49			All	2TCY		
RESET pulse width	50			All	300		
READ pulse width high setup time	51			01 02,04 03,05	200 155 85		
ADR from WRITE high hold time	52			All	0		
CS high from WRITE high hold time	53			All	0		
Data from WRITE high hold time	54			All	10		
WRITE pulse width	55			01 02,04 03,05	150 100 45		

1/ The following pins are active low: $\overline{IOR}$, $\overline{IOW}$, $\overline{MEMR}$($\overline{READ}$), $\overline{MEMW}$($\overline{WRITE}$), $\overline{CS}$ and $\overline{EOP}$. Unless otherwise specified, all test conditions shall be worst case condition. Unless otherwise specified, ac parameters are tested as follows: V_{CC} of 4.5 V and 5.5 V, inputs are driven at 1 ns/V, and must switch between V_{IH} + 0.4 V and V_{IL} - 0.4 V. Input and output timing reference levels are 1.5 V.
2/ Interchanging of force and sense conditions is permitted.
3/ Tested as follows: V_{CC} of 4.5 V and 5.5 V, frequency = 2.5 MHz, inputs are driven at 1 ns/V, and must switch between V_{IH} + 0.4 V and V_{IL} - 0.4 V.
4/ Guaranteed if not tested to the limits specified in table I.
5/ These test conditions only specified for device types 04 and 05. These limits are not specified for device types 01, 02 or 03.

Device types 01, 02 and 03

Case Q

Top view

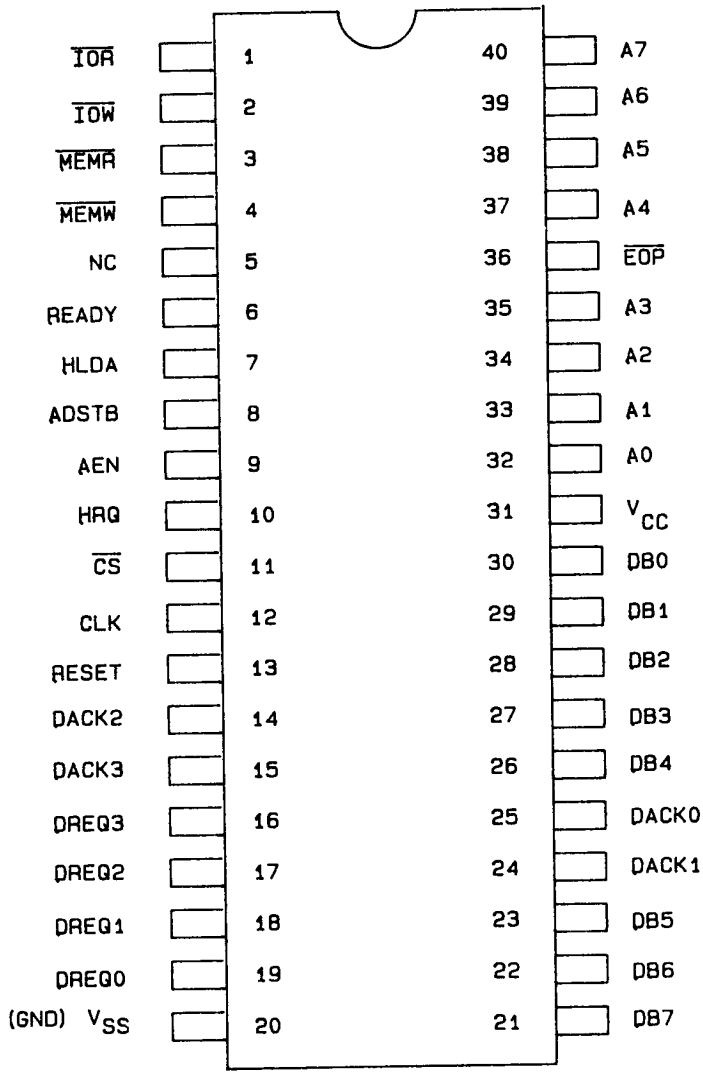


FIGURE 1. Terminal connections.

Device types 04 and 05

Case Q

Top view

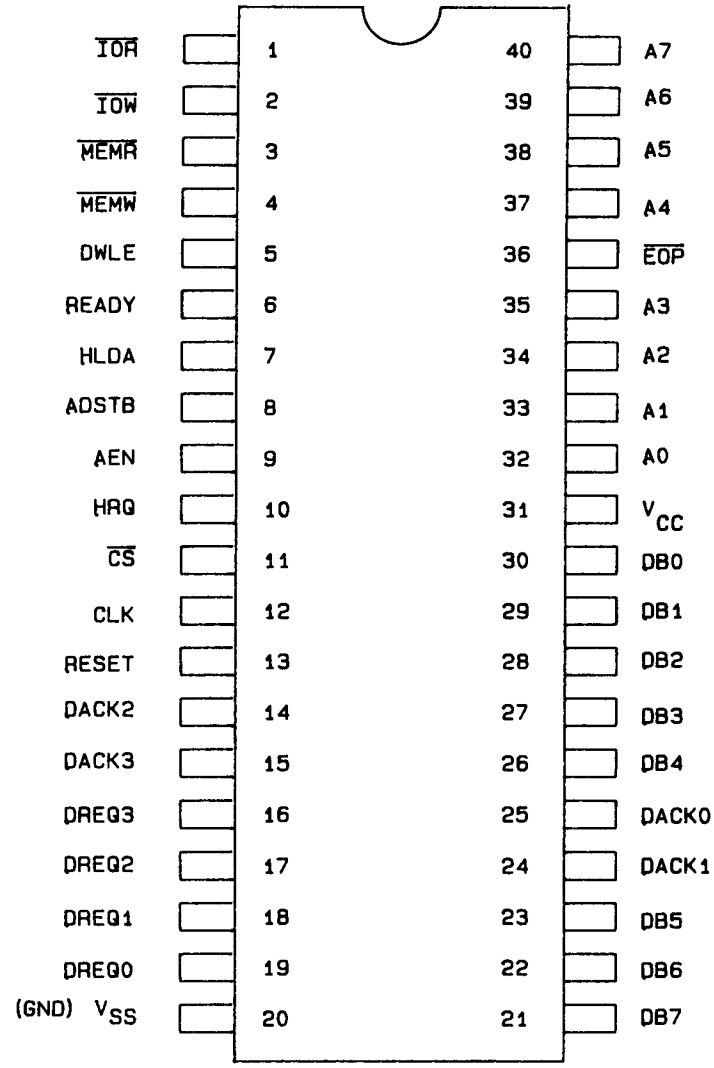


FIGURE 1. Terminal connections - Continued.

Device types 01, 02 and 03

Case X

Top view

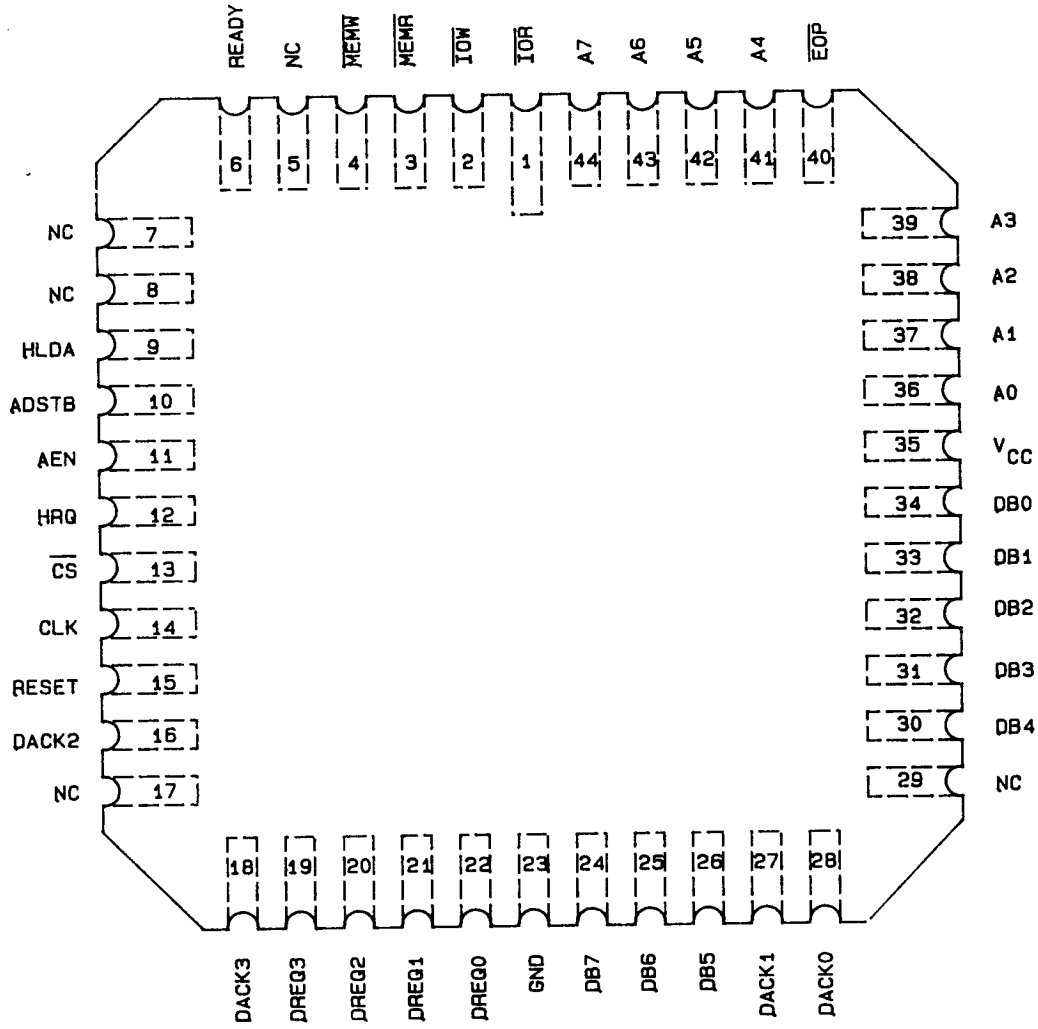


FIGURE 1. Terminal connections - Continued.

Device types 04 and 05

Case X

Top view

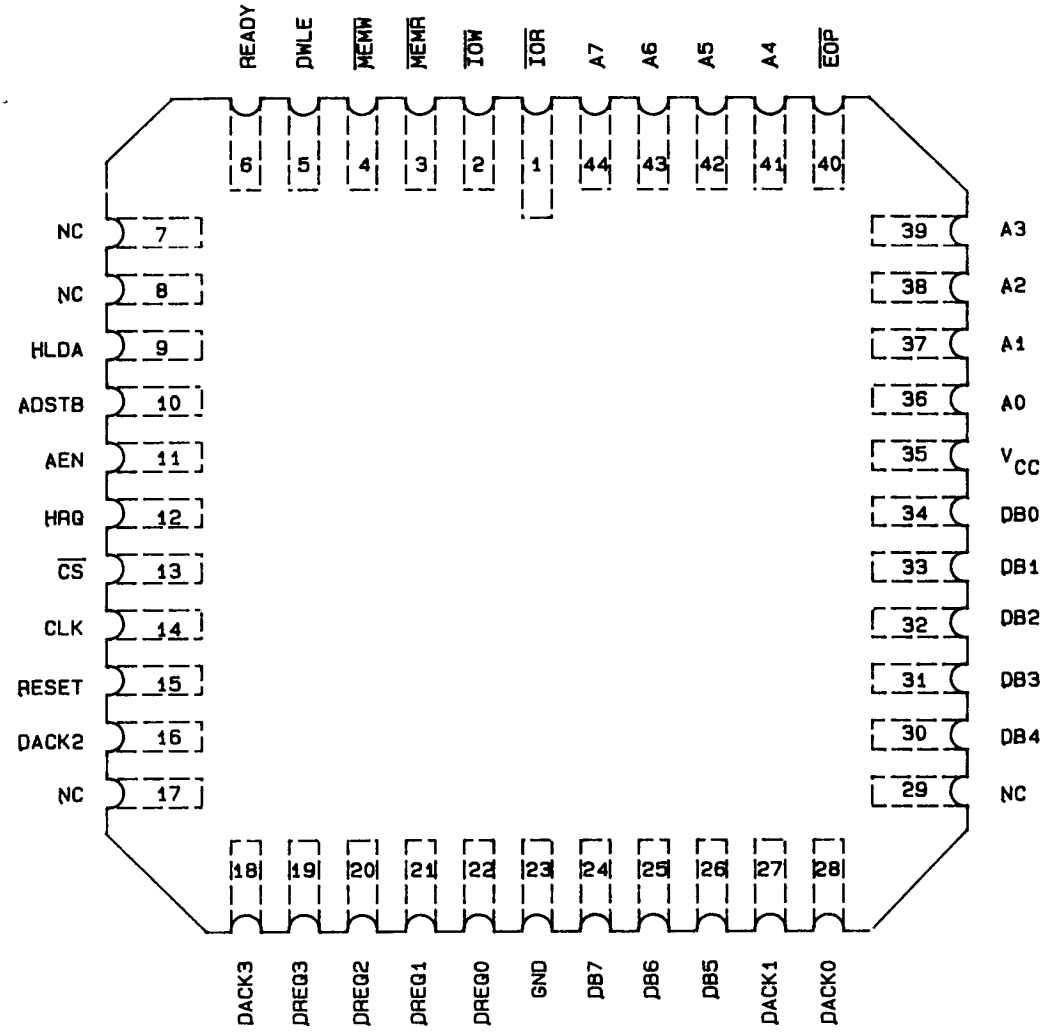


FIGURE 1. Terminal connections - Continued.

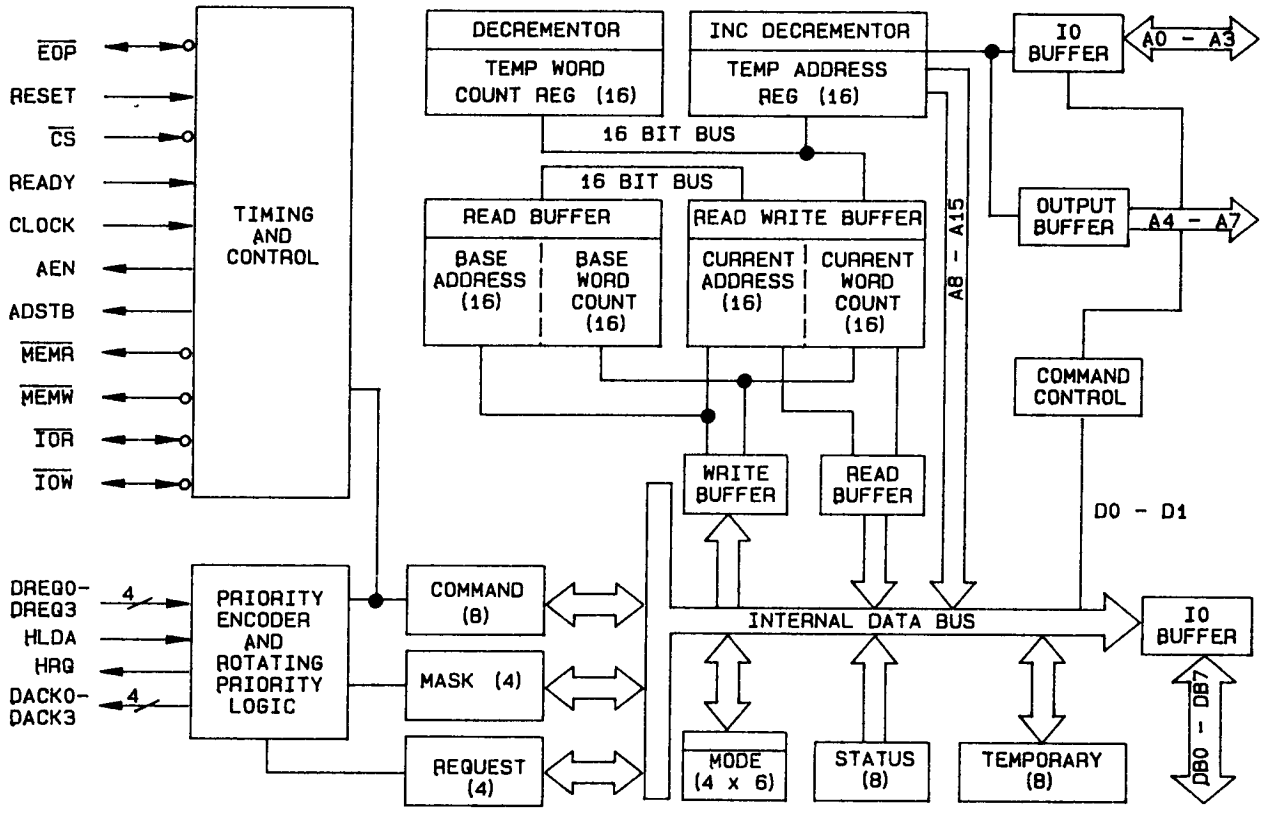


FIGURE 2. Functional block diagram.

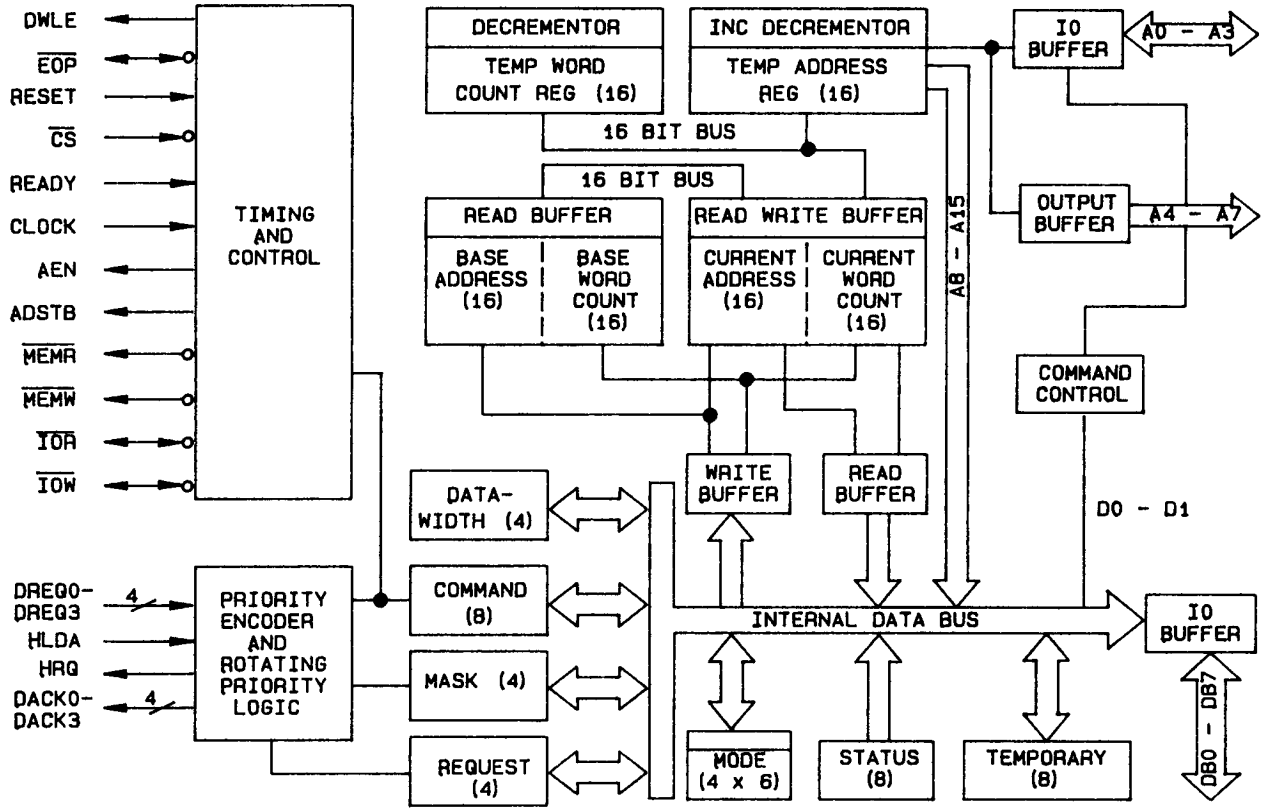
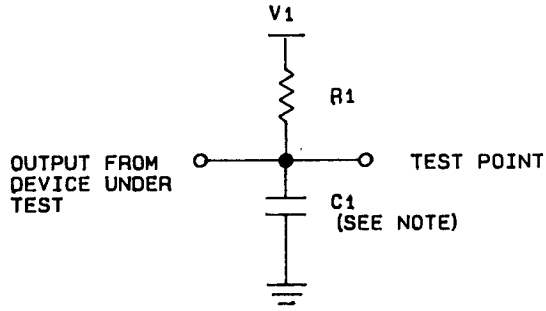


FIGURE 2. Functional block diagram - Continued.

AC test circuit

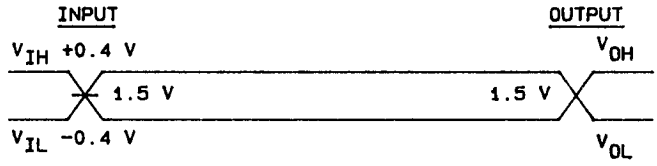


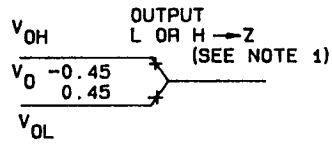
NOTE: Includes STRAY and FIXTURE capacitance.

Test condition definition table

PINS	V1	R1	C1
All outputs except $\overline{EOP}$	1.7 V	520Ω	100 pF
$\overline{EOP}$	V_{CC}	1.6 kΩ	50 pF

AC testing input, output waveforms

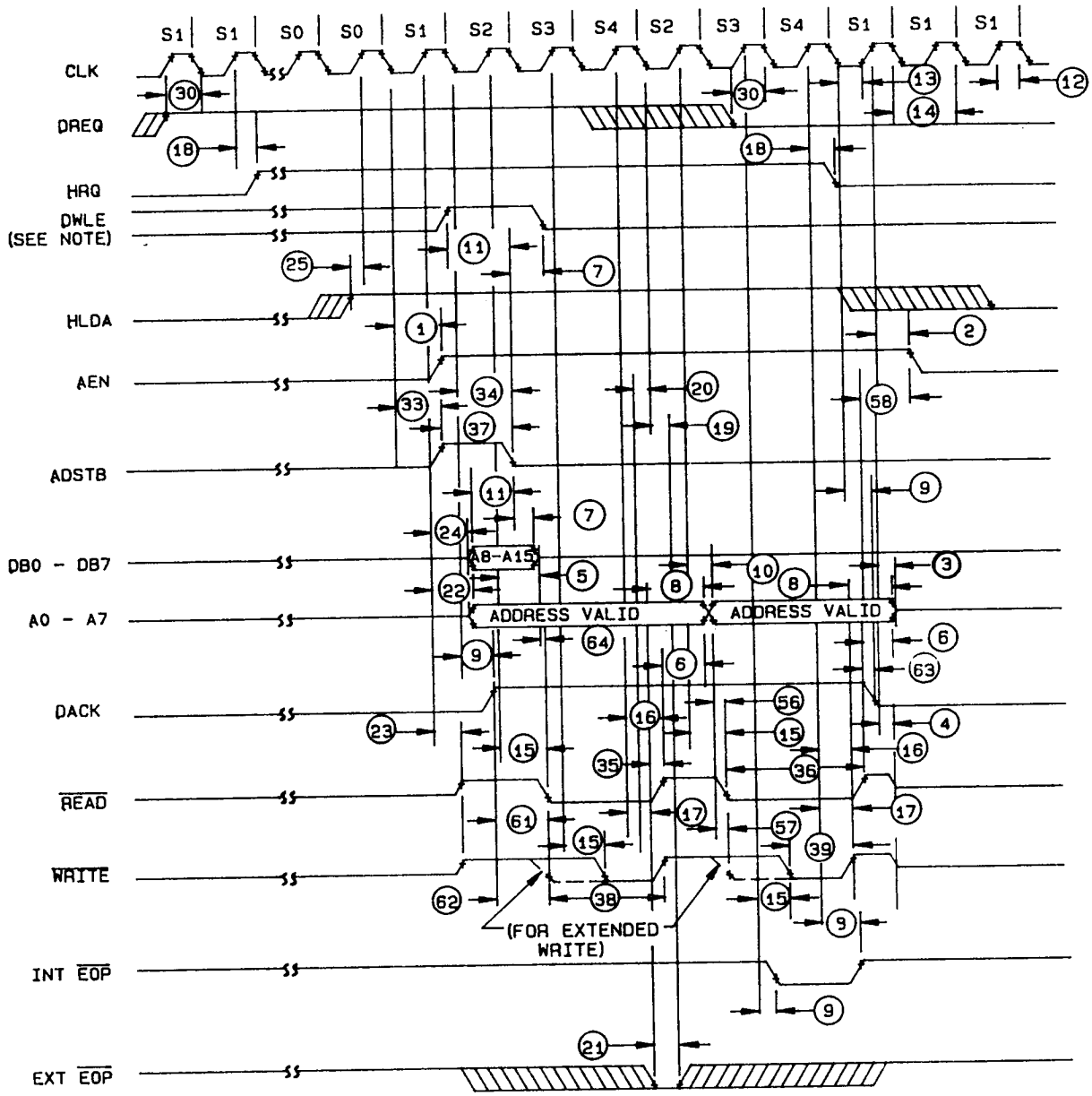




NOTES:
1. This specification applies only to valid-to-3-state outputs of recommended operation conditions: TAFAB(3), TAFC(4), TAFDB(5), TRDF(47), and TAZRL(64). Number in parentheses refers to ac parameter in figure 3.
2. AC testing: All ac parameters tested in accordance with test circuits, input RISE and FALL times are driven at 1 ns/V.

FIGURE 3. Test circuit and switching waveforms.

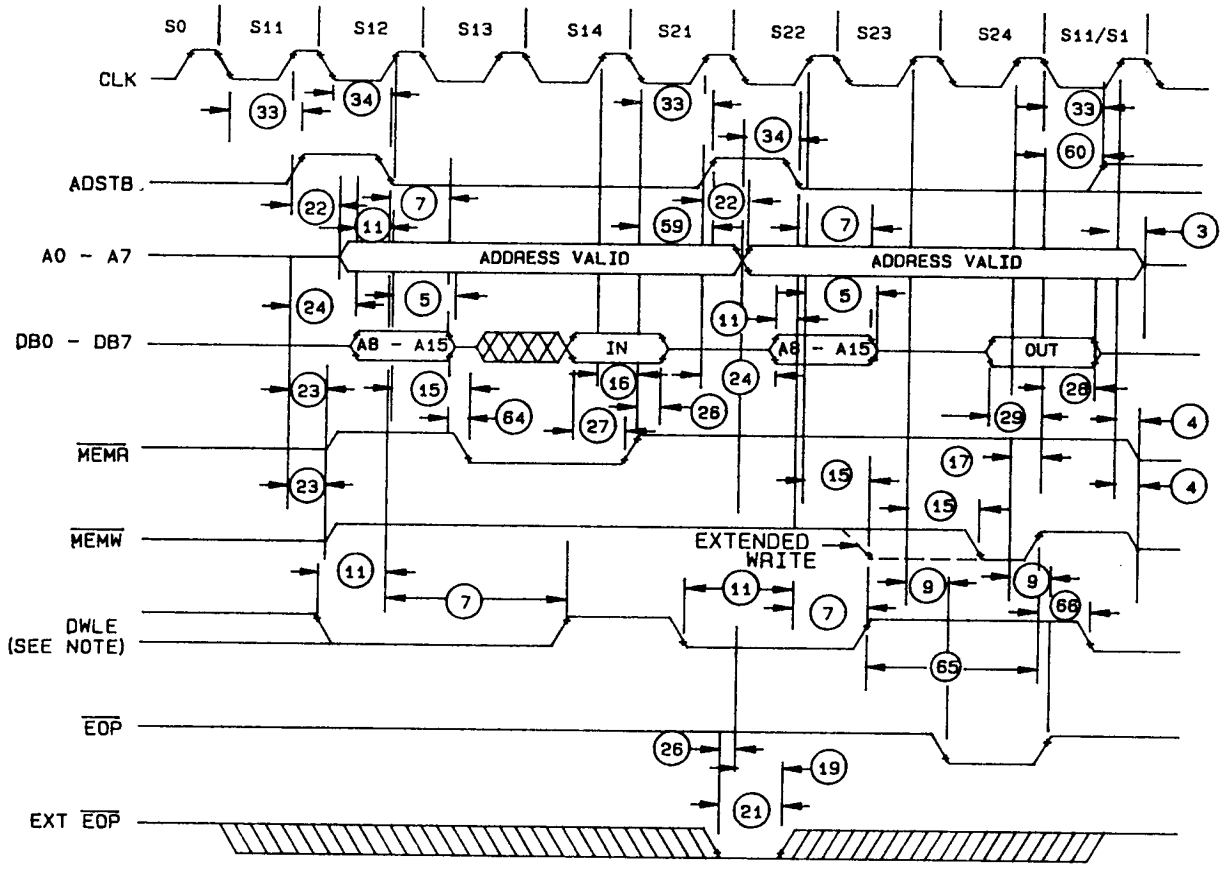
DMA transfer timing



NOTE: For devices 04 and 05 only: In 8-bit mode, this signal is always high impedance 3-stated. Waveform shown is for an 8-bit transfer with the devices programmed in 16-bit mode. For a 16-bit transfer, DWLE will go low at least (CLK high time - 20 ns) before the falling edge of ADSTB in S2, and remain low for the entire transfer.

FIGURE 3. Test circuit and switching waveforms - Continued.

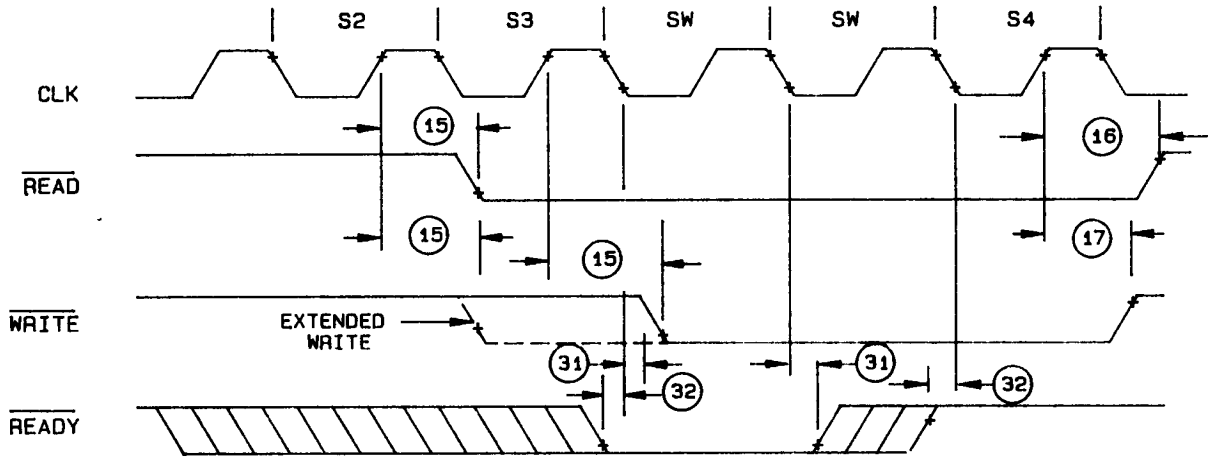
Memory-to-memory timing



NOTE: For 16-bit mode, devices 04 and 05 only. In 8-bit mode, this signal is always high impedance 3-stated. Waveform shown is for a 16-bit memory-to-memory transfer. For an 8-bit transfer in 16-bit mode, DWLE will go high at least (CLK high time - 20 ns) before the falling edge of ADSTB in S2, then low (CLK low time - 18 ns) after the falling edge of ADSTB, and will remain low until the next ADSTB where the cycle is repeated.

FIGURE 5. Test circuit and switching waveforms - Continued.

Ready timing



NOTE: READY must not transition during the specified setup and hold times.

Compressed transfer timing

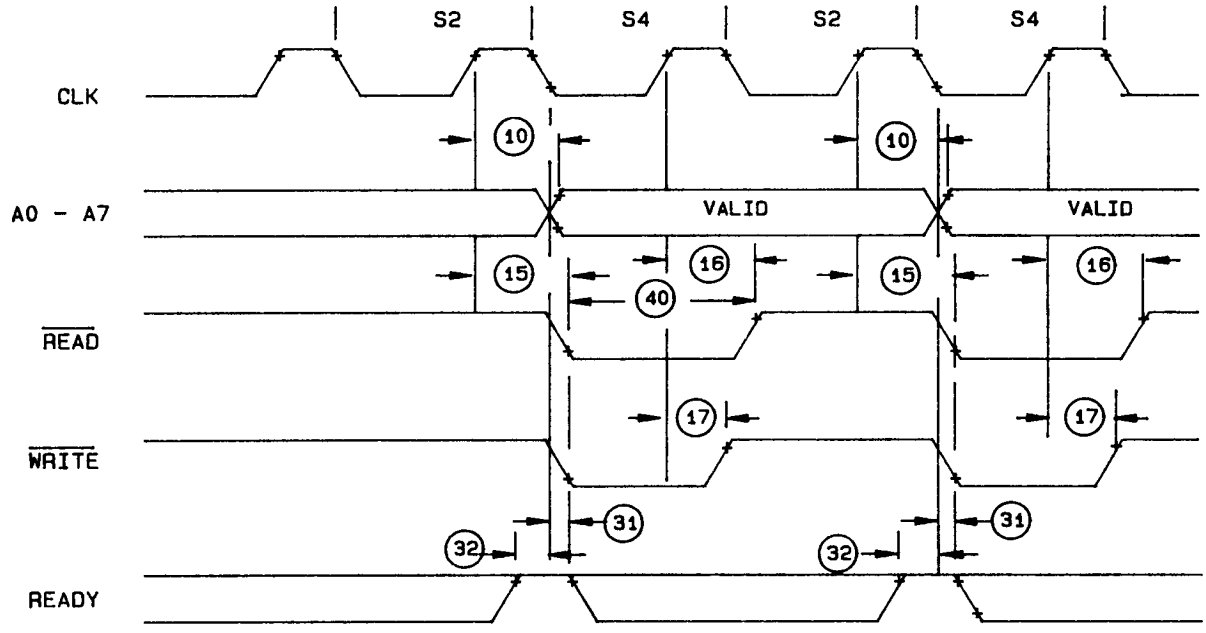
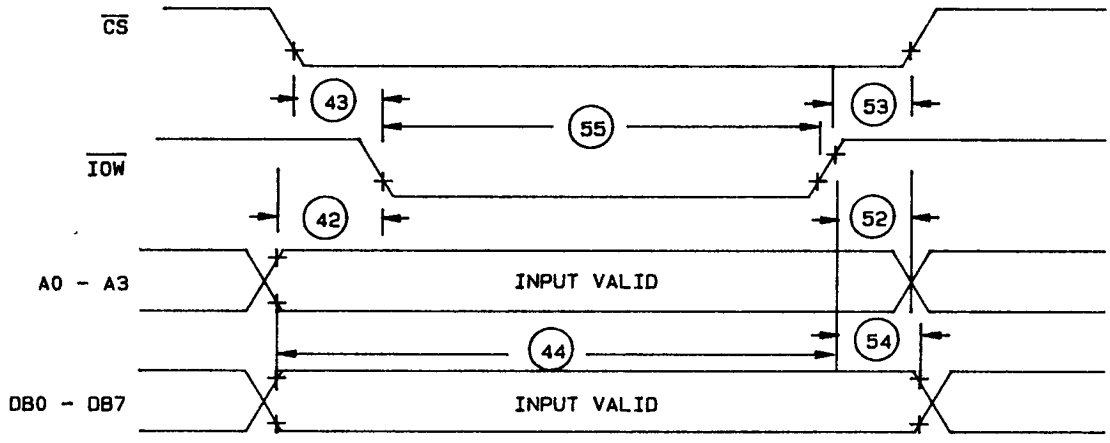


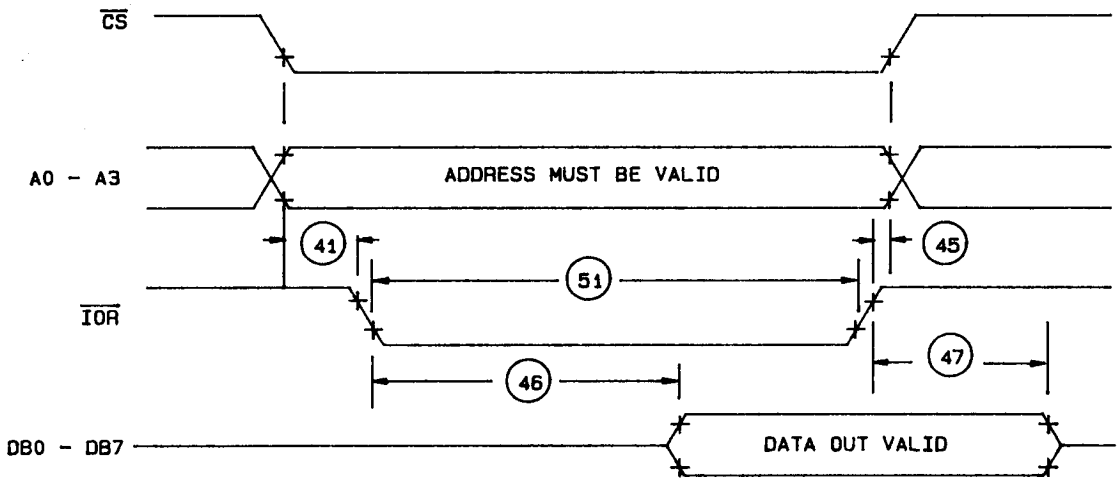
FIGURE 3. Test circuit and switching waveforms - Continued.

Slave mode write timing



NOTE: Successive WRITE accesses to the devices must allow at least a CLK cycle time as recovery time between accesses. A CLK cycle time recovery time must be allowed before executing a WRITE access after a READ access.

Slave mode read timing



NOTE: Successive READ accesses to the devices must allow at least a CLK cycle time as recovery time between accesses. A CLK cycle time recovery time must be allowed before executing a WRITE access after a READ access.

FIGURE 3. Test circuit and switching waveforms - Continued.

RESET timing

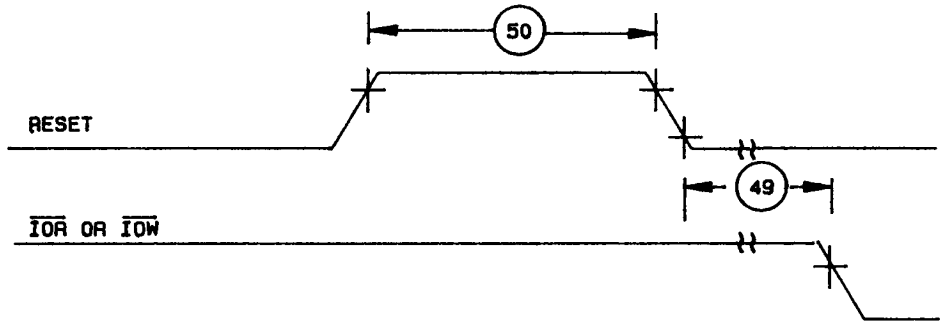


FIGURE 3. Test circuit and switching waveforms - Continued.

4. QUALITY ASSURANCE PROVISIONS

4.1 Sampling and inspection. For device class M, sampling and inspection procedures shall be in accordance with section 4 of MIL-M-38510 to the extent specified in MIL-STD-883 (see 3.1 herein). For device classes B and S, sampling and inspection procedures shall be in accordance with MIL-M-38510 and method 5005 of MIL-STD-883, except as modified herein. For device classes Q and V, sampling and inspection procedures shall be in accordance with MIL-I-38535.

4.2 Screening. For device class M, screening shall be in accordance with method 5004 of MIL-STD-883, and shall be conducted on all devices prior to quality conformance inspection. For device classes B and S, screening shall be in accordance with method 5004 of MIL-STD-883, and shall be conducted on all devices prior to qualification and quality conformance inspection. For device classes Q and V, screening shall be in accordance with MIL-I-38535, and shall be conducted on all devices prior to qualification and technology conformance inspection. The following additional criteria shall apply.

4.2.1 Additional criteria for device classes M, B, and S.

a. Burn-in test, method 1015 of MIL-STD-883.

(1) Test condition A, B, C, or D. For device class M, the test circuit shall be submitted to DESC-ECC for review with the certificate of compliance. For device classes B and S, the test circuit shall be submitted to the qualifying activity. For device classes Q and V, the test circuit shall be submitted to DESC-ECC with the certificate of compliance and under the control of the device manufacturer's technical review board (TRB) in accordance with MIL-I-38535.

(2) T_A = +125°C, minimum.

b. Interim and final electrical test parameters shall be as specified in table IIA herein, except interim electrical parameter tests prior to burn-in are optional at the discretion of the manufacturer.

4.2.2 Additional criteria for device classes Q and V.

a. The burn-in test duration, test condition and test temperature or approved alternatives shall be as specified in the device manufacturer's QM plan in accordance with MIL-I-38535. The burn-in test circuit shall be submitted to DESC-ECC with the certificate of compliance and shall be under the control of the device manufacturer's Technology Review Board (TRB) in accordance with MIL-I-38535.

b. Interim and final electrical test parameters shall be as specified in table IIA herein.

c. Additional screening for device class V beyond the requirements of device class Q shall be as specified in appendix B of MIL-I-38535 and as detailed in table IIB herein.

4.3 Qualification inspection.

4.3.1 Qualification inspection for device classes B and S. Qualification inspection for device classes B and S shall be in accordance with MIL-M-38510. Inspections to be performed shall be those specified in method 5005 of MIL-STD-883 and herein for groups A, B, C, D, and E inspections (see 4.4.1 through 4.4.5).

4.3.2 Qualification inspection for device classes Q and V. Qualification inspection for device classes Q and V shall be in accordance with MIL-I-38535. Inspections to be performed shall be those specified in MIL-I-38535 and herein for groups A, B, C, D, and E inspections (see 4.4.1 through 4.4.5).

4.4 Conformance inspection. Quality conformance inspection for device class M shall be in accordance with MIL-STD-883 (see 3.1 herein) and as specified herein. Quality conformance inspection for device classes B and S shall be in accordance with MIL-M-38510 and as specified herein. Inspections to be performed for device classes M, B, and S shall be those specified in method 5005 of MIL-STD-883 and herein for groups A, B, C, D, and E inspections (see 4.4.1 through 4.4.5). Technology conformance inspection for classes Q and V shall be in accordance with MIL-I-38535 including groups A, B, C, D, and E inspections and as specified herein.

4.4.1 Group A inspection.

a. Tests shall be as specified in table IIA herein.

b. Subgroups 5 and 6 in table I, method 5005 of MIL-STD-883 shall be omitted.

c. Subgroup 4 (C_I, C_O and $C_{I/O}$ measurement) shall be measured only for the initial test and after process or design changes which may affect capacitance. Sample size is 15 devices with no failures, and all input and output terminals tested.

d. Subgroups 7 and 8 functional test shall include verification of programming set.

4.4.2 Group B inspection. The group B inspection end-point electrical parameters shall be as specified in table IIA herein.

TABLE IIA. Electrical test requirements.

Test requirements	Subgroups (per method 5005, table I)			Subgroups (per MIL-I-38535, table III)	
	Device class M	Device class B	Device class S	Device class Q	Device class V
Interim electrical parameters (see 4.2)	----		1,7		1,7
Final electrical parameters (see 4.2)	1,2,3, 1/ 5,6,7,8, 9,10,11	1,2,3, 1/ 5,6,7,8, 9,10,11	1,2,3, 2/ 5,6,7,8, 9,10,11	1,2,3, 1/ 5,6,7,8, 9,10,11	1,2,3, 2/ 5,6,7,8, 9,10,11
Group A test requirements (see 4.4)	1,2,3,4, 7,8,9, 10,11	1,2,3,4, 7,8,9, 10,11	1,2,3,4, 7,8,9, 10,11	1,2,3,4, 7,8,9, 10,11	1,2,3,4, 7,8,9, 10,11
Group B end-point electrical parameters (see 4.4)	----		---		---
Group C end-point electrical parameters (see 4.4)	2,5,8,10	2,5,8,10		2,5,8,10	2,5,7,8,10
Group D end-point electrical parameters (see 4.4)	2,5,8,10	2,5,8,10	2,5,7,8,10	2,5,8,10	2,5,7,8,10
Group E end-point electrical parameters (see 4.4)	2,5,8,10	2,5,8,10	2,5,8,10	2,5,8,10	2,5,8,10

1/ PDA applies to subgroup 1.
2/ PDA applies to subgroups 1 and 7.

4.4.3 Group C inspection. The group C inspection end-point electrical parameters shall be as specified in table IIA herein.

4.4.3.1 Additional criteria for device classes M, B, and S. Steady-state life test conditions, method 1005 of MIL-STD-883:

a. Steady-state life test conditions, method 1005 of MIL-STD-883:

(1) Test condition A, B, C or D. For device class M, the test circuit shall be submitted to DESC-ECC for review with the certificate of compliance. For device classes B and S, the test circuit shall be submitted to the qualifying activity. For device classes Q and V, the test circuit shall be submitted to DESC-ECC with the certificate of compliance and under the control of the device manufacturer's technical review board (TRB) in accordance with MIL-I-38535.

b. T_A = +125°C, minimum.

c. Test duration: 1,000 hours, except as permitted by method 1005 of MIL-STD-883.

4.4.3.2 Additional criteria for device classes Q and V. The steady-state life test duration, test condition and test temperature or approved alternatives shall be as specified in the device manufacturer's QM plan in accordance with MIL-I-38535. The steady-state life test circuit shall be submitted to DESC-ECS with the certificate of compliance and shall be under the control of the device manufacturer's TRB in accordance with MIL-I-38535.

4.4.4 Group D inspection. For group D inspection end-point electrical parameters shall be as specified in table IIA herein.

4.4.5 Group E inspection. Group E inspection is required only for parts intended to be marked as radiation hardness assured (see 3.5 herein). RHA levels for device classes B and S shall be M, D, R, and H and for device class M shall be M and D. RHA quality conformance inspection sample tests shall be performed at the level specified in the acquisition document. RHA tests for device classes Q and V shall be performed in accordance with MIL-I-38535 and 1.2.1 herein.

TABLE IIB. Additional screening for device class V.

Test	MIL-STD-883, test method	Lot requirement
Particle impact noise detection	2020	100 percent
Internal visual	2010, condition A or approved alternate	100 percent
Nondestructive bond pull	2023 or approved alternate	100 percent
Reverse bias burn-in	1015	100 percent
Burn-in parameters	1015, total of 240 hrs. at +125°C	100 percent
Radiographic	2012	100 percent

a. RHA tests for device classes B and S for levels M, D, R, and H or for device class M for levels M and D shall be performed through each level to determine at what levels the devices meet the RHA requirements. These RHA tests shall be performed for initial qualification and after design or process changes which may affect the RHA performance of the device.

b. End-point electrical parameters shall be as specified in table IIA herein.

c. Prior to total dose irradiation, each selected sample shall be assembled in its qualified package. It shall pass the specified group A electrical parameters in table I for subgroups specified in table IIA herein.

d. For device classes M, B, and S, the devices shall be subjected to radiation hardness assured tests as specified in MIL-M-38510 for RHA level being tested, and meet the postirradiation end-point electrical parameter limits as defined in table I at T_A = 25°C ±5 percent, after exposure.

e. Prior to and during total dose irradiation testing, the devices shall be biased to establish a worst case condition as specified in the radiation exposure circuit.

(1) Inputs tested high, V_{CC} = volts dc, R_{CC} = Ω +5 percent, V_{IN} = volts dc, R_{IN} = Ω +20 percent, and all outputs are open.

(2) Inputs tested low V_{CC} = volts dc, R_{CC} = Ω +5 percent, V_{IN} = 0.0 V dc, and all outputs are open.

f. For device classes M, B, and S, subgroups 1 and 2 in table V, method 5005 of MIL-STD-883 shall be tested as appropriate for device construction.

g. When specified in the purchase order or contract, a copy of the RHA delta limits shall be supplied.

5. PACKAGING

5.1 Packaging requirements. The requirements for packaging shall be in accordance with MIL-M-38510 for device classes M, B, and S, and MIL-I-38535 for device classes Q and V.

6. NOTES

6.1 Intended use. Microcircuits conforming to this drawing are intended for use for Government microcircuit applications (original equipment), design applications, and logistics purposes.

6.1.1 Replaceability. Microcircuits covered by this drawing will replace the same generic device covered by a contractor-prepared specification or drawing.

6.1.2 Substitutability. Device classes B and Q devices will replace device class M devices.

6.2 Configuration control of SMD's. All proposed changes to existing SMD's will be coordinated with the users of record for the individual documents. This coordination will be accomplished in accordance with MIL-STD-481 using DD Form 1693, Engineering Change Proposal (Short Form).

6.3 Record of users. Military and industrial users shall inform Defense Electronics Supply Center when a system application requires configuration control and which SMD's are applicable to that system. DESC will maintain a record of users and this list will be used for coordination and distribution of changes to the drawings. Users of drawings covering microelectronic devices (FSC 5962) should contact DESC-ECS, telephone (513) 296-6022.

6.4 Comments. Comments on this drawing should be directed to DESC-ECC, Dayton, OH 45444, or telephone (513) 296-8525.

6.5 Symbols, definitions and functional descriptions.

Symbol	Type	Functional description
V_{CC}		+5 V power supply pin. A 0.1 μF capacitor between pins 31 and 20 is recommended for decoupling.
GND		Ground.
CLK	I	Clock input: The clock input is used to generate the timing signals which control the devices operations. This input may be driven from dc to 12.5 MHz for devices 03 and 05. The clock may be stopped in either state for standby operation.
$\overline{CS}$	I	Chip select: Chip select is an active low input used to enable the controller onto the data bus for CPU communications.
RESET	I	Reset: This is an active high input which clears the command, status, request, and temporary registers, the first/last flip-flop, and the mode register counter. The mask register is set to ignore requests. The data-width register is set to perform 8-bit transfers on all channels (devices 04 and 05 only). Following a reset, the controller is in an idle cycle.
READY	I	Ready: This signal can be used to extend the memory read and write pulses from devices 01 through 05 to accommodate slow memories or I/O devices. Ready must not make transitions during its specified set-up and hold times. Ready is ignored in verify transfer mode.

6.5 Symbols, definitions and functional descriptions - Continued.

Symbol	Type	Functional description
HLDA	I	Hold acknowledge: The active high hold acknowledge from the CPU indicates that it has relinquished control of the system buses. HLDA is a synchronous input and must not transition during its specified set-up time. There is an implied hold time (HLDA inactive) of a CLK high time from rising edge of clock, during which time HLDA must not transition.
DREQ0- DREQ3	I	DMA request: The DMA request (DREQ) lines are individual asynchronous channel request inputs used by peripheral circuits to obtain DMA service. In fixed priority, DREQ0 has the highest priority and DREQ3 has the lowest priority. A request is generated by activating the DREQ line of a channel. DACK will acknowledge the recognition of a DREQ signal. Polarity of DREQ is programmable. Reset initializes these lines to active high. DREQ must be maintained until the corresponding DACK goes active. DREQ will not be recognized while the clock is stopped. Unused DREQ inputs should be pulled high or low (inactive) and the corresponding mask bit set. In 16-bit transfer mode (devices 04 and 05 only), each DREQ channel may be programmed to perform either 8-bit or 16-bit DMA transfers.
DB0- DB7	I/O	Data bus: The data bus lines are bidirectional three-state signals connected to the system data bus. The outputs are enabled in program condition during the I/O read to output the contents of a register to the CPU. The outputs are disabled and the inputs are read during an I/O write cycle when the CPU is programming the control registers of devices 01 through 05. During DMA cycles, the most significant 8 bits of the address are output onto the data bus to be strobed into an external latch by ADSTB. In memory-to-memory operations, data from the memory enters devices 01 through 05 on the data bus during the read-from-memory transfer, then during the write-to-memory transfer, the data bus outputs write the data into the new memory location.
$\overline{IOR}$	I/O	I/O read: I/O read is a bidirectional active low three-state line. In the idle cycle, it is an input control signal used by the CPU to read the control registers. In the active cycle, it is an output control signal used by devices 01 through 05 to access data from a peripheral during a DMA write transfer.
$\overline{IOW}$	I/O	I/O write: I/O write is a bidirectional active low three-state line. In the idle cycle, it is an input control signal used by the CPU to load information into devices 01 through 05. In the active cycle, it is an output control signal used by devices 01 through 05 to load data to the peripheral during a DMA read transfer.
$\overline{EOP}$	I/O	End of process: End of process is an active low bidirectional signal. Information concerning the completion of DMA services is available at the bidirectional $\overline{EOP}$ pin. Devices 01 through 05 allow an external signal to terminate an active DMA service by pulling the $\overline{EOP}$ pin low. A pulse is generated by devices 01 through 05 when terminal count (TC) for any channel is reached, except for channel 0 in memory-to-memory mode. During memory-to-memory transfers, $\overline{EOP}$ will be output when the TC for channel 1 occurs. The $\overline{EOP}$ pin is driven by open drain transistor on-chip, and requires an external pull-up resistor to V_{CC}. When an $\overline{EOP}$ pulse occurs, whether internally or externally generated, devices 01 through 05 will terminate the service, and if autoinitialize is enabled, the base registers will be written to the current registers of that channel. The mask bit and TC bit in the status word will be set for the currently active channel $\overline{EOP}$ unless the channel is programmed for autoinitialize. In that case, the mask bit remains clear.

6.5 Symbols, definitions and functional descriptions - Continued.

Symbol	Type	Functional description
A0-A3	I/O	Address: The four least significant address lines are bidirectional three-state signals. In the idle cycle, they are inputs and are used by devices 01 through 05 to address the control register to be loaded or read. In the active cycle, they are outputs and provide the lower 4 bits of the output address. When in 16-bit mode (devices 04 and 05 only), and the active channel is a 16-bit channel (as defined by the data width register), then A0 will remain low during the entire transfer (i.e. an even word address will always be generated).
A4-A7	O	Address: The four most significant address lines are three-state outputs and provide 4 bits of address. These lines are enabled only during the DMA service.
HRQ	O	Hole request: The hold request output is used to request control of the system bus. When a DREQ occurs and the corresponding mask bit is clear, or a software DMA request is made, devices 01 through 05 issue HRQ. The HLDA signal then informs the controller when access to the system buses is permitted. For stand-alone operation where devices 01 through 05 always controls the buses, HRQ may be tied to HLDA. This will result in one S0 state before the transfer.
DACK0- DACK3	O	DMA acknowledge: DMA acknowledge is used to notify the individual peripherals when one has been granted a DMA cycle. The sense of these lines is programmable. Reset initializes them to active low.
AEN	O	Address enable: Address enable enables the 8-bit latch containing the upper 8 address bits onto the system address bus. AEN can also be used to disable other system bus drivers during DMA transfers. AEN is active high.
ADSTB	O	Address strobe: This is an active high signal used to control latching of the upper address byte. It will drive directly the strobe input of external transparent octal latches. During block operations, ADSTB will only be issued when the upper address byte must be updated, thus speeding operation through elimination of S1 states. ADSTB timing is referenced to the falling edge of devices 01 through 05.
$\overline{\text{MEMR}}$	O	Memory read: The memory read signal is an active low three-state output used to access data from the selected memory location during a DMA read or a memory-to-memory transfer.
$\overline{\text{MEMW}}$	O	Memory write: The memory write is an active low three-state output used to write data to the selected memory location during a DMA write or a memory-to-memory transfer.
DWLE	O	Data-width, latch enable: In normal 8-bit transfer mode (16-bit transfer mode not enabled, or devices 01 through 05), this output is always high impedance three-stated. In 16-bit transfer mode (devices 04 and 05), this output serves a dual purpose. During S1 cycles, the DWLE output indicates the data width (0 = 16-bit, 1 = 8-bit) of the active channel. During memory-to-memory transfers, the DWLE output is used to enable an external latch which temporarily stores the 8 most significant bits of data during the read-from-memory transfer. DWLE enables this byte of data on the data bus during the write-to-memory transfer of a memory-to-memory operation.

6.6 One part - one part number system. The one part - one part number system described below has been developed to allow for transitions between identical generic devices covered by the four major microcircuit requirements documents (MIL-M-38510, MIL-H-38534, MIL-I-38535, and 1.2.1 of MIL-STD-883) without the necessity for the generation of unique PIN's. The four military requirements documents represent different class levels, and previously when a device manufacturer upgraded military product from one class level to another, the benefits of the upgraded product were unavailable to the Original Equipment Manufacturer (OEM), who was contractually locked into the original unique PIN. By establishing a one part number system covering all four documents, the OEM can acquire to the highest class level available for a given generic device to meet system needs without modifying the original contract parts selection criteria.

Military documentation format	Example PIN under new system	Manufacturing source listing	Document listing
New MIL-M-38510 Military Detail Specifications (in the SMD format)	5962-XXXXXZZ(B or S)YY	QPL-38510 (Part 1 or 2)	MIL-BUL-103
New MIL-H-38534 Standardized Military Drawings	5962-XXXXXZZ(H or K)YY	QML-38534	MIL-BUL-103
New MIL-I-38535 Standardized Military Drawings	5962-XXXXXZZ(Q or V)YY	QML-38535	MIL-BUL-103
New 1.2.1 of MIL-STD-883 Standardized Military Drawings	5962-XXXXXZZ(M)YY	MIL-BUL-103	MIL-BUL-103

6.7 Sources of supply.

6.7.1 Sources of supply for device classes B and S. Sources of supply for device classes B and S are listed in QPL-38510.

6.7.2 Sources of supply for device classes Q and V. Sources of supply for device classes Q and V are listed in QML-38535. The vendors listed in QML-38535 have submitted a certificate of compliance (see 3.6 herein) to DESC-ECC and have agreed to this drawing.

6.7.3 Approved sources of supply for device class M. Approved sources of supply for class M are listed in MIL-BUL-103. The vendors listed in MIL-BUL-103 have agreed to this drawing and a certificate of compliance (see 3.6 herein) has been submitted to and accepted by DESC-ECC.