

REVISIONS																			
LTR	DESCRIPTION	DATE (YR-MO-DA)	APPROVED																
A	Add case outline Y. Rewrite entire document.	93-10-14	K. A. Cottongim																
B	Changes in accordance with NOR 5962-R115-96	96-04-22	K. A. Cottongim																
C	Make changes/corrections to table I.	97-07-14	K. A. Cottongim																

REV																				
SHEET																				
REV	C																			
SHEET	15																			

REV STATUS OF SHEETS	REV	C	C	C	C	C	C	C	C	C	C	C	C	C	C	C	C
	SHEET	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16

PMIC N/A STANDARD MICROCIRCUIT DRAWING THIS DRAWING IS AVAILABLE FOR USE BY ALL DEPARTMENTS AND AGENCIES OF THE DEPARTMENT OF DEFENSE AMSC N/A	PREPARED BY Donald R. Osborne CHECKED BY Robert M. Heber APPROVED BY William K. Heckman DRAWING APPROVAL DATE 91-03-25 REVISION LEVEL C	DEFENSE SUPPLY CENTER COLUMBUS P. O. BOX 3990 COLUMBUS, OHIO 43216-5000 MICROCIRCUIT, HYBRID, LINEAR, 1.0 VOLT, DIRECT RESOLVER TO DIGITAL CONVERTER <table style="width: 100%; border: none;"> <tr> <td style="width: 15%; border: none;">SIZE</td> <td style="width: 35%; border: none;">A</td> <td style="width: 20%; border: none;">CAGE CODE</td> <td style="width: 30%; border: none;">67268</td> <td style="width: 20%; border: none;">5962-90551</td> </tr> </table> SHEET 1 OF 15	SIZE	A	CAGE CODE	67268	5962-90551
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DISTRIBUTION STATEMENT A Approved for public release; distribution is unlimited.

5962-E233-97

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1. SCOPE

1.1 Scope. This drawing describes device requirements for class H hybrid microcircuits to be processed in accordance with MIL-PRF-38534 and a choice of case outlines and lead finishes are available and are reflected in the Part or Identifying Number (PIN).

1.2 PIN. The PIN shall be as shown in the following example:

<u>5962-90551</u>	<u>01</u>	<u>X</u>	<u>A</u>
Drawing number	Device type (see 1.2.1)	Case outline (see 1.2.2)	Lead finish (see 1.2.3)

1.2.1 Device type(s). The device type(s) shall identify the circuit function as follows:

<u>Device type</u>	<u>Generic number</u>	<u>Circuit function</u>	<u>Accuracy (± 1.0 LSB)</u>
01	SDC14567-111	1.0 V, 400 Hz, DR/D converter	6.0 minutes
02	SDC14567-112	1.0 V, 400 Hz, DR/D converter	4.0 minutes
03	SDC14567-114	1.0 V, 400 Hz, DR/D converter	2.0 minutes
04	SDC14567-115	1.0 V, 400 Hz, DR/D converter	1.0 minute
05	SDC14569-111	1.0 V, 400 Hz, trimmed velocity, DR/D converter	6.0 minutes
06	SDC14569-112	1.0 V, 400 Hz, trimmed velocity, DR/D converter	4.0 minutes
07	SDC14569-114	1.0 V, 400 Hz, trimmed velocity, DR/D converter	2.0 minutes
08	SDC14569-115	1.0 V, 400 Hz, trimmed velocity, DR/D converter	1.0 minutes

1.2.2 Case outline(s). The case outline(s) shall be as designated in MIL-STD-1835 and as follows:

<u>Outline letter</u>	<u>Descriptive designator</u>	<u>Terminals</u>	<u>Package style</u>
X	See figure 1	36	Dual-in-line
Y	See figure 1	36	Dual-in-line

1.2.3 Lead finish. The lead finish shall be as specified in MIL-H-38534.

1.3 Absolute maximum ratings. 1/

Positive supply voltage (V_{CC})	+18 V dc
Negative supply voltage (V_{EE})	-18 V dc
Logic supply voltage (V_{DD})	+8.0 V dc
Reference input voltage	130 V rms
Digital input voltage	-0.3 V dc to +8.0 V dc
Power dissipation, $T_C = +125^\circ\text{C}$ (P_D)	720 mW
Storage temperature range	-65°C to +150°C
Lead temperature (soldering, 10 seconds)	+300°C
Thermal resistance, junction-to-case (θ_{JC})	8.0°C/W
Thermal resistance, junction-to-ambient (θ_{JA})	20°C/W

1/ Stresses above the absolute maximum rating may cause permanent damage to the device. Extended operation at the maximum levels may degrade performance and affect reliability.

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1.4 Recommended operating conditions.

Positive supply voltage range (V_{CC})	+14.25 V dc to +15.75 V dc
Negative supply voltage range (V_{EE})	-14.25 V dc to -15.75 V dc
Logic supply voltage range (V_{DD})	+4.5 V dc to +5.5 V dc
Case operating temperature range (T_C)	-55°C to +125°C

2. APPLICABLE DOCUMENTS

2.1 Government specification, standards, and handbook. The following specification, standards, and handbook form a part of this drawing to the extent specified herein. Unless otherwise specified, the issues of these documents are those listed in the issue of the Department of Defense Index of Specifications and Standards (DoDISS) and supplement thereto, cited in the solicitation.

SPECIFICATION

DEPARTMENT OF DEFENSE

MIL-PRF-38534 - Hybrid Microcircuits, General Specification for.

STANDARDS

DEPARTMENT OF DEFENSE

MIL-STD-883 - Test Methods and Procedures for Microelectronics.
MIL-STD-973 - Configuration Management.
MIL-STD-1835 - Microcircuit Case Outlines.

HANDBOOK

DEPARTMENT OF DEFENSE

MIL-HDBK-780 - Standard Microcircuit Drawings.

(Unless otherwise indicated, copies of the specification, standards, and handbook are available from the Standardization Document Order Desk, 700 Robbins Avenue, Building 4D, Philadelphia, PA 19111-5094.)

2.2 Order of precedence. In the event of a conflict between the text of this drawing and the references cited herein, the text of this drawing takes precedence. Nothing in this document, however, supersedes applicable laws and regulations unless a specific exemption has been obtained.

3. REQUIREMENTS

3.1 Item requirements. The individual item performance requirements for device class H shall be in accordance with MIL-PRF-38534. Compliance with MIL-PRF-38534 may include the performance of all tests herein or as designated in the device manufacturer's Quality Management (QM) plan or as designated for the applicable device class. Therefore, the tests and inspections herein may not be performed for the applicable device class (see MIL-PRF-38534). Furthermore, the manufacturers may take exceptions or use alternate methods to the tests and inspections herein and not perform them. However, the performance requirements as defined in MIL-PRF-38534 shall be met for the applicable device class.

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3.2 Design, construction, and physical dimensions. The design, construction, and physical dimensions shall be as specified in MIL-PRF-38534 and herein.

3.2.1 Case outline(s). The case outline(s) shall be in accordance with 1.2.4 herein and figure 1.

3.2.2 Terminal connections. The terminal connections shall be as specified on figure 2.

3.2.3 Timing diagram(s). The timing diagram(s) shall be as specified on figure 3.

3.3 Electrical performance characteristics. Unless otherwise specified herein, the electrical performance characteristics are as specified in table I and shall apply over the full specified operating temperature range.

3.4 Electrical test requirements. The electrical test requirements shall be the subgroups specified in table II. The electrical tests for each subgroup are defined in table I.

3.5 Marking of device(s). Marking of device(s) shall be in accordance with MIL-PRF-38534. The device shall be marked with the PIN listed in 1.2 herein. In addition, the manufacturer's vendor similar PIN may also be marked as listed in QML-38534.

3.6 Data. In addition to the general performance requirements of MIL-PRF-38534, the manufacturer of the device described herein shall maintain the electrical test data (variables format) from the initial quality conformance inspection group A lot sample, for each device type listed herein. Also, the data should include a summary of all parameters manually tested, and for those which, if any, are guaranteed. This data shall be maintained under document revision level control by the manufacturer and be made available to the preparing activity (DSCC-VA) upon request.

3.7 Certificate of compliance. A certificate of compliance shall be required from a manufacturer in order to supply to this drawing. The certificate of compliance (original copy) submitted to DSCC-VA shall affirm that the manufacturer's product meets the performance requirements of MIL-PRF-38534 and herein.

3.8 Certificate of conformance. A certificate of conformance as required in MIL-PRF-38534 shall be provided with each lot of microcircuits delivered to this drawing.

4. QUALITY ASSURANCE PROVISIONS

4.1 Sampling and inspection. Sampling and inspection procedures shall be in accordance with MIL-PRF-38534 or as modified in the device manufacturer's Quality Management (QM) plan. The modification in the QM plan shall not affect the form, fit, or function as described herein.

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TABLE I. Electrical performance characteristics.

Test	Symbol	Conditions 1/ $-55^{\circ}\text{C} \leq T_c \leq +125^{\circ}\text{C}$ unless otherwise specified	Group A subgroups	Device type	Limits		Unit
					Min	Max	
Resolution control	RC	2/ $A = B = 0.8\text{ V}$ $A = 2.0\text{ V}, B = 0.8\text{ V}$ $A = 0.8\text{ V}, B = 2.0\text{ V}$ $A = B = 2.0\text{ V}$	7,8A,8B	All	10	10	Bits
					12	12	
					14	14	
					16	16	
Accuracy differential	AD	3/	7,8A,8B	All	-1.0	+1.0	LSB
Differential linearity	DL				-1.0	+1.0	
Accuracy repeatability	AR				-1.0	+1.0	
Output Accuracy	AOUT	4/	4,5,6	01,05	-19.0	+19.0	LSB
				02,06	-13.0	+13.0	
				03,07	-7.0	+7.0	
				04,08	-4.0	+4.0	
Reference synthesizer	RS	Reference phase shift 3/ between the converter signal and reference inputs	4,5,6	All	-45	+45	Degree
Reference input impedence	Z_{IN1}	Single ended 3/	4,5,6	All	100		k Ω
		Differential 3/	4,5,6	All	250		
Reference input common mode range	CMR ₁	3/	4,5,6	All	-210	+210	V _{pk}
Signal input impedance	Z_{IN2}	Voltage follower 3/	4,5,6	All	20		M Ω
Signal input transient	T _{vp}	3/	4,5,6	All	100		V _{pk}

See footnotes at end of table.

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TABLE I. Electrical performance characteristics - Continued.

Test	Symbol	Conditions 1/ -55°C ≤ T _c ≤ +125°C unless otherwise specified	Group A subgroups	Device type	Limits		Unit
					Min	Max	
Digital output low voltage	V _{OL}	I _{OL} = -1.6 mA, output bits 1 through 16, CB, and BIT	1,2,3	All		0.4	V
Digital output high voltage	V _{OH}	I _{OH} = -0.4 mA, output bits 1 through 16, CB, and BIT	1,2,3	All	2.8		V
Output leakage current (high impedance)	I _z	Output bits 1 through 16	1,2,3	All	-10	+10	μA
Digital output delay, converter busy	t _{CB}	Positive pulse, see figure 3.	7,8A,8B	All	0.4	1.0	μs
Digital output error detection (built-in-test)	BIT	Logic 0 indicates fault, minimum error for bit condition	7,8A,8B	All	20	100	LSB
Analog output error	e _{OUT}	All analog outputs loaded with a resistor of ≤ 3 KΩ to ground.	7,8A,8B	All	42.5	57.5	mVrms/LSB
		12-bit mode		All	21.25	28.75	
		14-bit mode		All	10.63	14.39	
		16-bit mode		All	5.31	7.19	
Analog output offset voltage	V _{OS}	V _{OUT} at zero speed 5/	4,5,6	All		40	mV
Analog output positive linearity error	EUP	5/ 6/	4,5,6	01,02, 03,04		2.0	%
				05,06, 07,08		0.7	

See footnotes at end of table.

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TABLE I. Electrical performance characteristics - Continued.

Test	Symbol	Conditions 1/ -55°C ≤ T _c ≤ +125°C unless otherwise specified	Group A subgroups	Device type	Limits		Unit
					Min	Max	
Analog output negative linearity error	EUN	5/ 6/	4,5,6	01,02, 03,04		±2.0	%
				05,06, 07,08		±0.7	
Analog output reversal error	EB	Difference between positive and negative linearity 5/	4,5,6	01,02, 03,04		±2.0	%
				05,06, 07,08		±0.7	
Analog output scale factor	SF	5/	4,5,6	All	52	70	mV/LSB/s
Digital input high voltage	V _{IH}	INH, EL, EM, S, A, B, and digital bits 1 through 16 while in CT mode	7,8A,8B	All	2.0		V
Digital input low voltage	V _{IL}		7,8A,8B	All		0.8	V
Inhibit (INH) voltage	V _{INH}	No digital angles change 2/ while INH is logic 0 and analog input is rotating	7,8A,8B	All		0.8	V
Enable voltage	V _E	EM controls output bit 1 through 8 and EL controls output bits 9 through 16 2/	7,8A,8B	All		0.8	V
Disable voltage (high impedance)	V _O		7,8A,8B	All	2.0		V
Set (S) voltage	V _S	For use in CT mode 2/	7,8A,8B	All		0.8	V

See footnotes at end of table.

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TABLE I. Electrical performance characteristics - Continued.

Test	Symbol	Conditions 1/ -55°C ≤ T _c ≤ +125°C unless otherwise specified	Group A subgroups	Device type	Limits		Unit
					Min	Max	
Positive supply current	I _{cc}	V _{cc} = +15.75 V	1,2,3	All		25	mA
Negative supply current	I _{ee}	V _{ee} = -15.75 V	1,2,3	All		-15	mA
Logic supply current	I _{od}	V _{od} = +5.5 V	1,2,3	All		10	mA
Bandwidth	BW	16-bit and 14-bit mode	7,8A,8B	All	38	70	Hz
		12-bit and 10-bit mode			154	286	

1/ V_{cc} = +15.0 V dc, V_{ee} = -15.0 V dc, and V_{od} = +5.0 V dc, unless otherwise specified.

2/ These parameters are tested on a go-no-go basis only or in conjunction with other measured parameters and are not directly testable.

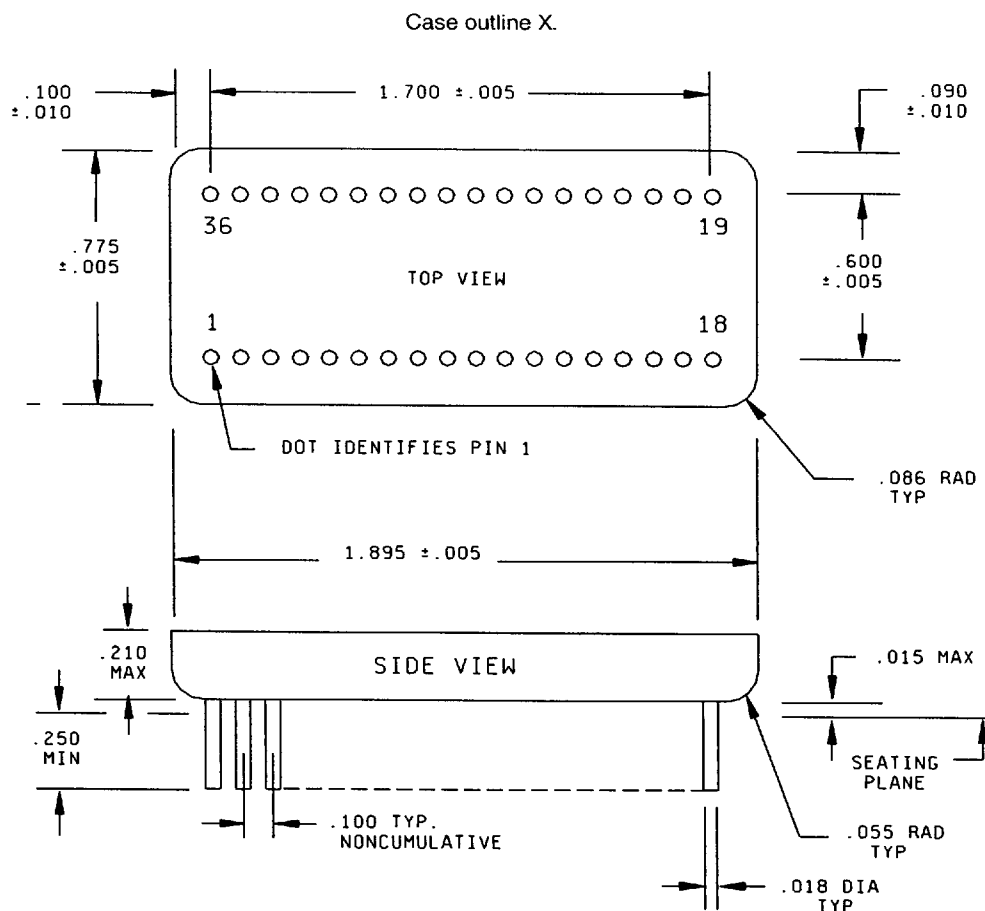
3/ Parameter shall be tested as part of device initial characterization and after design and process changes. Parameter shall be guaranteed to limits specified in table I for all lots not specifically tested.

4/ Output accuracy is measured at angles from 0° to 180°, in 15° increments, and at 225°, 270°, and 315°. Output accuracy measurements at 10, 12, and 14-bit resolutions are performed on a go-no-go basis only at 0° and 45°.

5/ Tests are performed in 12-bit resolution with a full speed of 400 Hz. Velocity data is measured at multiples of full scale, 3/4, 1/2, 1/4, and ±0 of the rated full speed.

6/ Analog output linearity error is defined as the best straight line from zero speed, to either positive or negative direction as applicable, that yields the lowest peak error readings.

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Inches	mm	Inches	mm
.002	0.05	.100	2.54
.005	0.13	.210	5.33
.010	0.25	.250	6.35
.015	0.38	.600	15.24
.018	0.46	.775	19.69
.055	1.40	1.700	43.18
.086	2.18	1.895	48.13
.090	2.29		

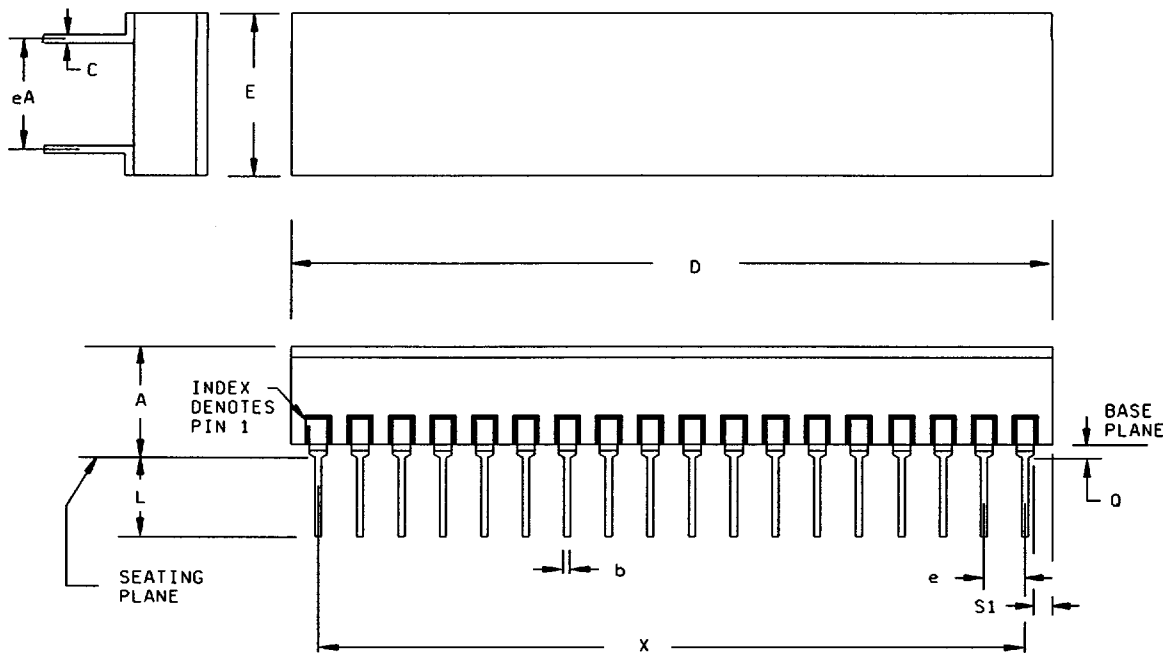
NOTES:

1. Dot on lid of package indicates pin 1.
2. Dimensions are in inches.
3. Metric equivalents are given for information only.
4. Lead identification numbers are for reference only.
5. Lead spacing dimensions apply only at seating plane.

FIGURE 1. Case outline(s).

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Case outline Y.



Symbol	Millimeters		Inches	
	Min	Max	Min	Max
A		5.33		0.210
b	0.41	0.51	0.016	0.020
c	0.41	0.51	0.016	0.020
D		48.26		1.900
e	2.54 BSC		0.100 BSC	
E		20.32		0.800
eA	15.11	15.37	0.595	0.605
L	6.10	6.60	0.240	0.260
Q		0.72		0.030
S1	2.18	2.44	0.086	0.096
X	43.18 BSC		1.700 BSC	

NOTES:

1. The U.S. government preferred system of measurement is the metric SI. This item was designed using inch-pound units of measurement. In case of problems involving conflicts between the metric and inch-pound units, the inch-pound units shall rule.

FIGURE 1. Case outline(s) - Continued.

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Device types	01, 02, 03, 04, 05, 06, 07, and 08	Device types	01, 02, 03, 04, 05, 06, 07, and 08
Case outlines	X and Y	Case outlines	X and Y
Terminal number	Terminal symbol	Terminal number	Terminal symbol
1	V (analog ground)	19	RH
2	+ Cosine	20	RL
3	+ Sine	21	BIT-15
4	N/C	22	BIT-16(LSB,16-BIT MODE)
5	BIT-1 (MSB)	23	VEL
6	BIT-2	24	CB
7	BIT-3	25	EL
8	BIT-4	26	EM
9	BIT-5	27	e
10	BIT-6	28	+5 V or (V_{DD})
11	BIT-7	29	GROUND
12	BIT-8	30	S
13	BIT-9	31	-15 V or (V_{EE})
14	BIT-10(LSB,10-BIT MODE)	32	+15 V or (V_{CC})
15	BIT-11	33	INH
16	BIT-12(LSB,12-BIT MODE)	34	BIT
17	BIT-13	35	A
18	BIT-14(LSB,14-BIT MODE)	36	B

FIGURE 2. Terminal connections.

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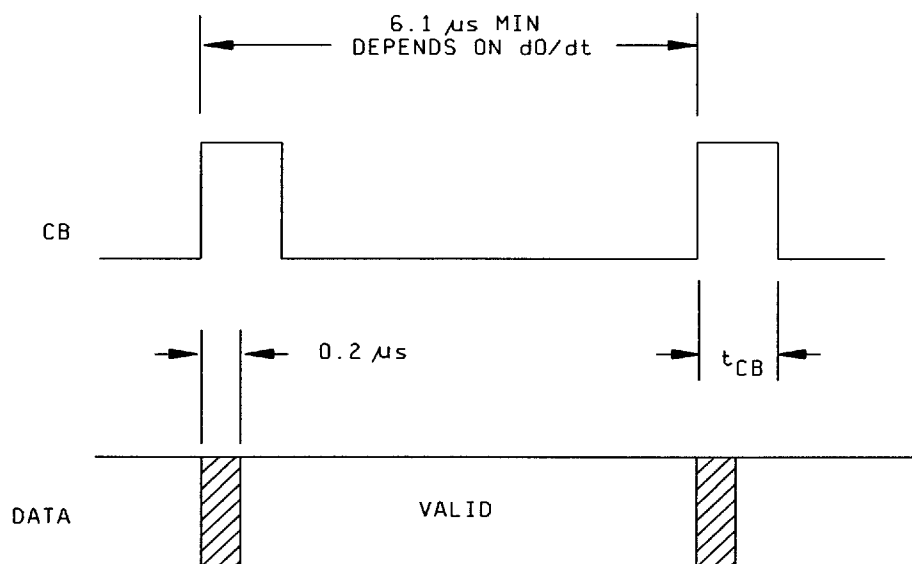


FIGURE 3. Converter busy timing diagram.

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TABLE II. Electrical test requirements.

MIL-PRF-38534 test requirements	Subgroups (in accordance with MIL-PRF-38534, group A test table)
Interim electrical parameters	1,4,7
Final electrical parameters	1*,2,3,4,5,6,7,8A,8B
Group A test requirements	1,2,3,4,5,6,7,8,A,8B
Group C end-point electrical parameters	1,2,3,4,5,6,7,8,A,8B
MIL-STD-883, group E end-point electrical parameters for RHA devices	Subgroups** (in accordance with method 5005, group A test table)

* PDA applies to subgroup 1.

** When applicable to this standard microcircuit drawing,
the subgroups shall be defined.

4.2 Screening. Screening shall be in accordance with MIL-PRF-38534. The following additional criteria shall apply:

a. Burn-in test, method 1015 of MIL-STD-883.

(1) Test condition A, B, C, or D. The test circuit shall be maintained by the manufacturer under document revision level control and shall be made available to either DSCC-VA or the acquiring activity upon request. Also, the test circuit shall specify the inputs, outputs, biases, and power dissipation, as applicable, in accordance with the intent specified in test method 1015 of MIL-STD-883.

(2) T_c as specified in accordance with table I of method 1015 of MIL-STD-883.

b. Interim and final electrical test parameters shall be as specified in table II herein, except interim electrical parameter tests prior to burn-in are optional at the discretion of the manufacturer.

4.3 Conformance and periodic inspections. Conformance inspection (CI) and periodic inspection (PI) shall be in accordance with MIL-PRF-38534 and as specified herein.

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4.3.1 Group A inspection (CI). Group A inspection shall be in accordance with MIL-PRF-38534 and as follows:

- a. Tests shall be as specified in table II herein.
- b. Subgroups 9, 10, and 11 shall be omitted.

4.3.2 Group B inspection (PI). Group B inspection shall be in accordance with MIL-PRF-38534.

4.3.3 Group C inspection (PI). Group C inspection shall be in accordance with MIL-PRF-38534 and as follows:

- a. End-point electrical parameters shall be as specified in table II herein.
- b. Steady-state life test, method 1005 of MIL-STD-883.
 - (1) Test condition A, B, C, or D. The test circuit shall be maintained by the manufacturer under document revision level control and shall be made available to either DSCC-VA or the acquiring activity upon request. Also, the test circuit shall specify the inputs, outputs, biases, and power dissipation, as applicable, in accordance with the intent specified in test method 1005 of MIL-STD-883.
 - (2) T_c as specified in accordance with table I of method 1005 of MIL-STD-883.
 - (3) Test duration: 1,000 hours, except as permitted by method 1005 of MIL-STD-883.

4.3.4 Group D inspection (PI). Group D inspection shall be in accordance with MIL-PRF-38534.

4.3.5 Group E inspection. Group E inspection is required only for parts intended to be marked as radiation hardness assured (see 3.5 herein). RHA levels shall be M, D, R, and H. RHA quality conformance inspection sample tests shall be performed at the RHA level specified in the acquisition document.

- a. RHA tests for levels M, D, R, and H shall be performed through each level to determine at what levels the devices meet the RHA requirements. These RHA tests shall be performed for initial qualification and after design or process changes which may affect the RHA performance of the device.
- b. End-point electrical parameters shall be as specified in table II herein.
- c. Prior to total dose irradiation, each selected sample shall be assembled in its qualified package. It shall pass the specified group A electrical parameters in table I for subgroups specified in table II herein.
- d. The devices shall be subjected to radiation hardness assured tests as specified in MIL-PRF-38534 for RHA level being tested, and meet the postirradiation end-point electrical parameter limits as defined in table I at $T_A = +25^\circ\text{C} \pm 5$ percent, after exposure.
- e. Prior to and during total dose irradiation testing, the devices shall be biased to establish a worst case condition as specified in the radiation exposure circuit.
- f. For device classes H and K, subgroups 1 and 2 in table V, method 5005 of MIL-STD-883 shall be tested as appropriate for device construction.
- g. When specified in the purchase order or contract, a copy of the RHA delta limits shall be supplied.

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5. PACKAGING

5.1 Packaging requirements. The requirements for packaging shall be in accordance with MIL-PRF-38534.

6. NOTES

6.1 Intended use. Microcircuits conforming to this drawing are intended for use for Government microcircuit applications (original equipment), design applications, and logistics purposes.

6.2 Replaceability. Microcircuits covered by this drawing will replace the same generic device covered by a contractor-prepared specification or drawing.

6.3 Configuration control of SMD's. All proposed changes to existing SMD's will be coordinated with the users of record for the individual documents. This coordination will be accomplished in accordance with MIL-STD-973 using DD Form 1692, Engineering Change Proposal.

6.4 Record of users. Military and industrial users shall inform Defense Supply Center Columbus when a system application requires configuration control and the applicable SMD. DSCC will maintain a record of users and this list will be used for coordination and distribution of changes to the drawings. Users of drawings covering microelectronic devices (FSC 5962) should contact DSCC-VA, telephone (614) 692-7603.

6.5 Comments. Comments on this drawing should be directed to DSCC-VA, P. O. Box 3990, Columbus, Ohio 43216-5000, or telephone (614) 692-0512.

6.6 Sources of supply. Sources of supply are listed in QML-38534. The vendors listed in QML-38534 have submitted a certificate of compliance (see 3.7 herein) to DSCC-VA and have agreed to this drawing.

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STANDARD MICROCIRCUIT DRAWING SOURCE APPROVAL BULLETIN

DATE: 97-07-14

Approved sources of supply for SMD 5962-90551 are listed below for immediate acquisition only and shall be added to QML-38534 during the next revision. QML-38534 will be revised to include the addition or deletion of sources. The vendors listed below have agreed to this drawing and a certificate of compliance has been submitted to and accepted by DSCC-VA. This bulletin is superseded by the next dated revision of QML-38534.

Standard microcircuit drawing PIN 1/	Vendor CAGE number	Vendor similar PIN 2/
5962-9055101YX	3/	SDC14567-111
5962-9055101XA 5962-9055101XC 5962-9055101XA 5962-9055101XC	S7631 S7631 19645 19645	SDC14567-141 SDC14567-111 SDC14567-141 SDC14567-111
5962-9055102YX	3/	SDC14567-112
5962-9055102XA 5962-9055102XC 5962-9055102XA 5962-9055102XC	S7631 S7631 19645 19645	SDC14567-142 SDC14567-112 SDC14567-142 SDC14567-112
5962-9055103YX	3/	SDC14567-114
5962-9055103XA 5962-9055103XC 5962-9055103XA 5962-9055103XC	S7631 S7631 19645 19645	SDC14567-144 SDC14567-114 SDC14567-144 SDC14567-114
5962-9055104YX	3/	SDC14567-115
5962-9055104XA 5962-9055104XC 5962-9055104XA 5962-9055104XC	S7631 S7631 19645 19645	SDC14567-145 SDC14567-115 SDC14567-145 SDC14567-115
5962-9055105YX	3/	SDC14569-111
5962-9055105XA 5962-9055105XC 5962-9055105XA 5962-9055105XC	S7631 S7631 19645 19645	SDC14569-141 SDC14569-111 SDC14569-141 SDC14569-111

STANDARD MICROCIRCUIT DRAWING SOURCE APPROVAL BULLETIN - Continued.

DATE: 97-07-14

Standard microcircuit drawing PIN 1/	Vendor CAGE number	Vendor similar PIN 2/
5962-9055106YX	3/	SDC14569-112
5962-9055106XA 5962-9055106XC 5962-9055106XA 5962-9055106XC	S7631 S7631 19645 19645	SDC14569-142 SDC14569-112 SDC14569-142 SDC14569-112
5962-9055107YX	3/	SDC14569-114
5962-9055107XA 5962-9055107XC 5962-9055107XA 5962-9055107XC	S7631 S7631 19645 19645	SDC14569-144 SDC14569-114 SDC14569-144 SDC14569-114
5962-9055108YX	3/	SDC14569-115
5962-9055108XA 5962-9055108XC 5962-9055108XA 5962-9055108XC	S7631 S7631 19645 19645	SDC14569-145 SDC14569-115 SDC14569-145 SDC14569-115

- 1/ The lead finish shown for each PIN, representing a hermetic package, is the most readily available from the manufacturer listed for that part. If the desired lead finish is not listed contact the Vendor to determine its availability.
- 2/ Caution. Do not use this number for item acquisition. Items acquired to this number may not satisfy the performance requirements of this drawing.
- 3/ Not available from a QML source.

Vendor CAGE
numberVendor name
and address

S7631

DDC Ireland LTD.
Cork Business and Technology Park
Model Farm Road
Cork, Ireland

19645

ILC Data Device Corporation
105 Wilbur Place
Bohemia, NY 11716-2482

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