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LTR	DESCRIPTION	DATE (YR-MO-DA)	APPROVED

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	SHEET	1	2	3	4	5	6	7	8	9	10	11	12	13	14

PMIC N/A

STANDARD MICROCIRCUIT DRAWING

THIS DRAWING IS AVAILABLE FOR USE BY ALL DEPARTMENTS AND AGENCIES OF THE DEPARTMENT OF DEFENSE

AMSC N/A

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DRAWING APPROVAL DATE
95-04-14

REVISION LEVEL

DEFENSE ELECTRONICS SUPPLY CENTER
DAYTON, OHIO 45444

MICROCIRCUIT, LINEAR, 16-BIT, 7 VOLT AMP OUTPUT DRIVE, DIGITAL TO SYNCHRO CONVERTER, HYBRID

SIZE	CAGE CODE	5962-90760
A	67268	

SHEET 1 OF 16

DESC FORM 193
JUL 94

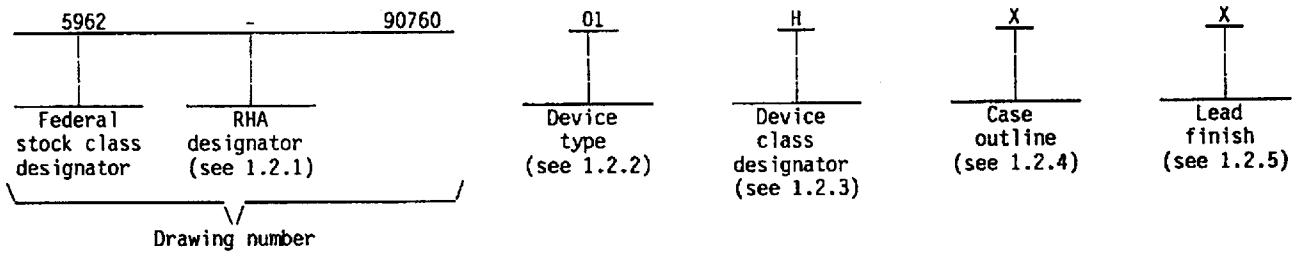
5962-E166-95

DISTRIBUTION STATEMENT A. Approved for public release; distribution is unlimited.

1. SCOPE

1.1 Scope. This drawing forms a part of a one part - one part number documentation system (see 6.6 herein). This drawing describes device requirements for hybrid microcircuits to be processed in accordance with MIL-H-38534. Two product assurance classes, military high reliability (device class H) and space application (device class K) and a choice of case outlines and lead finishes are available and are reflected in the Part or Identifying Number (PIN). When available, a choice of radiation hardness assurance levels are reflected in the PIN.

1.2 PIN. The PIN shall be as shown in the following example:



1.2.1 Radiation hardness assurance (RHA) designator. Device classes H and K RHA marked devices shall meet the MIL-H-38534 specified RHA levels and shall be marked with the appropriate RHA designator. A dash (-) indicates a non-RHA device.

1.2.2 Device type(s). The device type(s) shall identify the circuit function as follows:

Device type	Generic number	Circuit function	Accuracy
01	DSC-10510-113	D/S converter, 16-bit	±4 minutes
02	DSC-10510-114	D/S converter, 16-bit	±2 minutes

1.2.3 Device class designator. This device class designator shall be a single letter identifying the product assurance level as follows:

Device class	Device requirements documentation
H or K	Certification and qualification to MIL-H-38534

1.2.4 Case outline(s). The case outline(s) shall be as designated in MIL-STD-1835 and as follows:

Outline letter	Descriptive designator	Terminals	Package style
X	See figure 1	40	Dual-in-line

1.2.5 Lead finish. The lead finish shall be as specified in MIL-H-38534 for classes H and K. Finish letter "X" shall not be marked on the microcircuit or its packaging. The "X" designation is for use in specifications when lead finishes A, B, and C are considered acceptable and interchangeable without preference.

1.3 Absolute maximum ratings. 1/

Positive supply voltage (V_{CC})	+18 V dc
Negative supply voltage (V_{EE})	-18 V dc
Power stage supply voltage (±V)	±25 Vpk
Reference input voltage (R_H, R_L)	75 V rms
Reference input voltage ($R_{H'}$, $R_{L'}$)	10 V rms
Digital input voltage range (BITS 1-16)	-0.3 V dc to +6.5 V dc
Power dissipation at T_A = +125°C (P_D)	25 W
Storage temperature range	-65°C to +150°C
Lead temperature (soldering 10 seconds)	+300°C
Thermal resistance, junction to case (θ_{JC})	6°C/W
Thermal resistance, case to ambient (θ_{CA})	17.6°C/W

1.4 Recommended operating conditions.

Positive supply voltage range (V_{CC})	+14.25 V dc to +15.75 V dc
Negative supply voltage range (V_{EE})	-14.25 V dc to -15.75 V dc
Power stage supply voltage (±V)	±15 V dc or pulsating supply, (20 V peak, 3 V minimum, see figure 5)

2. APPLICABLE DOCUMENTS

2.1 Government specification, standards, and handbook. Unless otherwise specified, the following specification, standards, and handbook of the issue listed in that issue of the Department of Defense Index of Specifications and Standards specified in the solicitation, form a part of this drawing to the extent specified herein.

SPECIFICATION

MILITARY

MIL-H-38534 - Hybrid Microcircuits, General Specification for.

STANDARDS

MILITARY

MIL-STD-883 - Test Methods and Procedures for Microelectronics.
MIL-STD-973 - Configuration Management.
MIL-STD-1835 - Microcircuit Case Outlines.

HANDBOOK

MILITARY

MIL-HDBK-780 - Standardized Military Drawings.

(Copies of the specification, standards, and handbook required by manufacturers in connection with specific acquisition functions should be obtained from the contracting activity or as directed by the contracting activity.)

2.2 Order of precedence. In the event of a conflict between the text of this drawing and the references cited herein, the text of this drawing shall take precedence.

1/ Stresses above the absolute maximum rating may cause permanent damage to the device. Extended operation at the maximum levels may degrade performance and affect reliability.

3. REQUIREMENTS

3.1 Item requirements. The individual item requirements shall be in accordance with MIL-H-38534 and as specified herein.

3.2 Design, construction, and physical dimensions. The design, construction, and physical dimensions shall be as specified in MIL-H-38534 and herein.

3.2.1 Case outline(s). The case outline(s) shall be in accordance with 1.2.4 herein and figure 1.

3.2.2 Terminal connections. The terminal connections shall be as specified on figure 2.

3.2.3 Block diagram. The block diagram shall be as specified on figure 3.

3.2.4 Timing diagram. The Timing diagram shall be as specified on figure 4.

3.2.5 Pulsating power source diagram. The pulsating power source diagram shall be as specified on figure 5.

3.2.6 Pin functions. The pin function shall be as specified on table III.

3.3 Electrical performance characteristics. Unless otherwise specified herein, the electrical performance characteristics are as specified in table I and shall apply over the full specified operating temperature range.

3.4 Electrical test requirements. The electrical test requirements shall be the subgroups specified in table II. The electrical tests for each subgroup are described in table I.

3.5 Marking. Marking shall be in accordance with MIL-H-38534. The part shall be marked with the PIN listed in 1.2 herein. In addition, the manufacturer's PIN may also be marked as listed in QML-38534.

3.6 Manufacturer eligibility. In addition to the general requirements of MIL-H-38534, the manufacturer of the part described herein shall maintain the electrical test data (variables format) from the initial quality conformance inspection group A lot sample, produced on the certified line, for each device type listed herein. The data should also include a summary of all parameters manually tested, and for those which, if any, are guaranteed. This data shall be maintained under document revision level control by the manufacturer and be made available to the preparing activity (DESC-EC) upon request.

3.7 Certificate of compliance. A certificate of compliance shall be required from a manufacturer in order to supply to this drawing. The certificate of compliance submitted to DESC-EC shall affirm that the manufacturer's product meets the requirements of MIL-H-38534 and the requirements herein.

3.8 Certificate of conformance. A certificate of conformance as required in MIL-H-38534 shall be provided with each lot of microcircuits delivered to this drawing.

4. QUALITY ASSURANCE PROVISIONS

4.1 Sampling and inspection. Sampling and inspection procedures shall be in accordance with MIL-H-38534.

4.2 Screening. Screening shall be in accordance with MIL-H-38534. The following additional criteria shall apply:

a. Burn-in test, method 1015 of MIL-STD-883.

(1) Test condition A, B, C, or D. The test circuit shall be maintained by the manufacturer under document revision level control and shall be made available to either DESC-EC or the acquiring activity upon request. Also, the test circuit shall specify the inputs, outputs, biases, and power dissipation, as applicable, in accordance with the intent specified in test method 1015 of MIL-STD-883.

(2) T_A as specified in accordance with table I of method 1015 of MIL-STD-883.

b. Interim and final electrical test parameters shall be as specified in table II herein, except interim electrical parameter tests prior to burn-in are optional at the discretion of the manufacturer.

TABLE I. Electrical performance characteristics.

Test	Symbol	Conditions 1/ $-55°C \le T_C \le +125°C$ unless otherwise specified	Group A subgroups	Device type	Limits		Unit
					Min	Max	
Resolution, 16-bit	RES	MSB = 180 degrees LSB = .0055 degrees	7,8	All		.33	Arcmin
Output accuracy	A_{OUT}		7,8	01	-4	+4	min
				02	-2	+2	
Differential linearity 2/	DL		7,8	All	-1	+1	LSB
Radius accuracy 2/	RA	3/	7,8	All	-.1	+.1	%
Output settling time	t_S	For any digital input step change (passive loads)	9,10,11	All		40	µS
Logic 0 digital input voltage	V_{IL}		1,2,3	All	0.0	1.25	V dc
Logic 1 digital input voltage	V_{IH}		1,2,3	All	2.0	5.0	V dc
Digital input load 2/ current	I_{IN}	Bits 1-16, V_{IL} = 0 V dc	1,2,3	All		-20	µA
		$\overline{LL}$, $\overline{LH}$, and $\overline{LA}$, V_{IH} = 5.0 V dc	1,2,3	All		+20	µA
Standard reference input voltage	V_{IN}	RH and RL	4,5,6	All	23.4	28.6	V rms
	V_{IN1}	RH' and RL'			3.06	3.74	
Reference input frequency	f_{IN}		4,5,6	All	dc	1.0	kHz
Standard reference 2/ input impedance	Z_{IN}	RH and RL, single ended	4,5,6	All	99.5	100.5	kΩ
		RH and RL, differential			199	201	
	Z_{IN1}	RH' and RL', differential	4,5,6	All	25.87	26.13	kΩ
		RH' and RL', single ended			12.94	13.07	
Analog output current	I_{OUT}	short circuit protected	4,5,6	All		2	mA rms

See footnotes at end of table.

TABLE I. Electrical performance characteristics - Continued.

Test	Symbol	Conditions 1/ $-55°C \le T_C \le +125°C$ unless otherwise specified	Group A subgroups	Device type	Limits		Unit
					Min	Max	
Analog output voltage (ground based)	V_{OUT}	synchro, (26 V reference input)	4,5,6	All	11.74	11.86	V rms L-L
Analog output 2/ transformation ratio	AOTR		4,5,6	All	-.5	+.5	%
TR load 2/	Z_{SS}	maximum load	4,5,6	All	2		Ω
CT or CDX load 2/	Z_{SO}		4,5,6	All		7	VA
Analog output offset voltage 2/	V_{OS}	each line to ground, (varies with angle)	1,2,3	All	-15	+15	mV
Analog output scale 2/ factor varation	SPV		7,8	All	-0.1	+0.1	%
Register latch control	Logic 0	$\overline{LL}$, $\overline{LM}$, and $\overline{LA}$, data latched	7,8	All			pass/ fail
	Logic 1	$\overline{LL}$, $\overline{LM}$, and $\overline{LA}$, data tranparent	7,8	All			
Register control pulse width	t_{PW}	For data transfer, see figure 4	9,10,11	All	200		ns
Register control data setup time	t_{SU}	Before data transfer, see figure 4	9,10,11	All	50		ns
Register control data hold time	t_H	Hold time after low edge of $\overline{LL}$, $\overline{LM}$, and $\overline{LA}$, see figure 4	9,10,11	All	100		ns
Positive supply current (V_{CC})	I_{CC}	V_{CC} = +15 V dc, no load	1,2,3	All		+25	mA
Negative supply current (V_{EE})	I_{EE}	V_{EE} = -15 V dc, no load	1,2,3	All		-25	mA
Power stage supply current	+V	Full load	1,2,3	All		+700	mA rms
	-V	Full load	1,2,3	All		-700	mA rms

See footnotes at end of table.

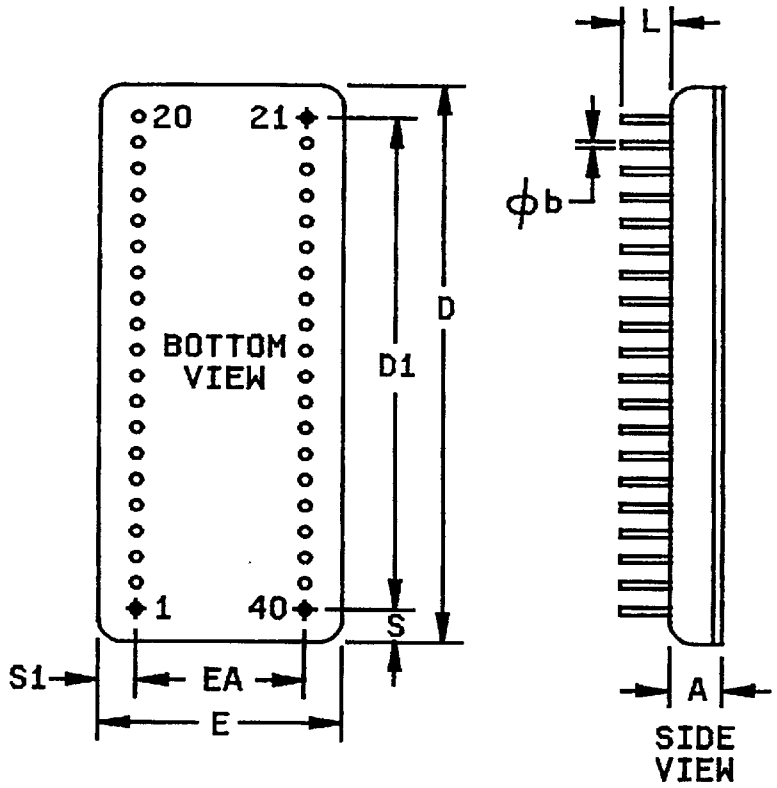
TABLE I. Electrical performance characteristics - Continued.

Test	Symbol	Conditions 1/ $-55°C \le T_C \le +125°C$ unless otherwise specified	Group A subgroups	Device type	Limits		Unit
					Min	Max	
Digital BITE output	BIT	Logic 1 at rated synchro load, I = 0, -0.4 mA	9,10,11	All	2.8	5.5	V
		Logic 0 at short circuit at 45.000°, I = 1.6 mA	9,10,11	All	0.0	0.4	V

1/ Unless otherwise specified, $+14.25$ V dc $\le V_{CC} \le +15.75$ V dc, -14.25 V dc $\le V_{EE} \le -15.75$ V dc.

2/ Parameter shall be tested as part of device initial characterization and after design and process changes. Parameter shall be guaranteed to the limits specified in table I for all lots not specifically tested.

3/ Radius accuracy is defined as the simultaneous amplitude variation in both outputs as a function of digital angle.



Symbol	Millimeters		Inches	
	Min	Max	Min	Max
A		5.08		.200
ϕb	.41	.51	.016	.020
D	54.22	54.48	2.135	2.145
D1	48.13	48.38	1.895	1.905
	non-cummulative		non-cummulative	
E	28.82	29.08	1.135	1.145
EA	22.73	22.98	.895	.905
L	4.31		.170	
S	2.99	3.09	.118	.122
S1	2.99	3.09	.118	.122

NOTES:
1. The case outline X was originally designed using inch-pound units of measurement, in the event of conflict between the metric and inch-pound units, the inch pound units shall take precedence.
2. Lead identification numbers are for reference only.

FIGURE 1. Case outline.

Device types	01 and 02	
Case outline	X	
Pin number	Name	Pin Function
1	D01	Digital input 01 (MSB) logic "1" enables
2	D02	Digital input 02
3	D03	Digital input 03
4	D04	Digital input 04
5	D05	Digital input 05
6	D06	Digital input 06
7	D07	Digital input 07
8	D08	Digital input 08
9	D09	Digital input 09
10	D010	Digital input 10
11	D011	Digital input 11
12	D012	Digital input 12
13	D013	Digital input 13
14	D014	Digital input 14
15	D015	Digital input 15
16	D016	Digital input 16 (LSB)
17	RL	26V rms reference low input
18	RH	26V rms reference high input
19	S1'	Synchro S1 remote sense output
20	S1	Synchro S1 output
21	S2	Synchro S2 output
22	S3	Synchro S3 output
23	+V	Power stage positive voltage supply
24	-V	Power stage negative voltage supply
25	S2'	Synchro S2 remote sense output
26	S3'	Synchro S3 remote sense output
27	NC	No connection
28	GND	Ground
29	V_{EE}	Negative power supply
30	V_{CC}	Positive power supply
31	$\overline{LA}$	2nd latch all enable. Input enables dual latch
32	$\overline{LL}$	1st latch LSB's enable. Enables bits 9-16
33	$\overline{LM}$	1st latch MSB's enable. Enables bits 1-8
34	RL'	3.4V rms reference low input
35	RH'	3.4V rms reference high input
36	$\overline{-R(TP)}$	No connection. Factory test point
37	$\overline{EN}$	Enable. Power stage enable input allows for digital shutdown of power stage. Gives complete control of converter to digital system.
38	$\overline{BS}$	Battle short input. Logic"0" overrides over-temperature protection.
39	$\overline{BIT}$	Built-in-test output. Logic"0" when loss of reference, loss of ±15V dc supply, case temperature of +140°C, $\overline{EN}$ input signal, an output over-current or short circuit has been detected. Power output stage is turned off unless $\overline{BS}$ is at "0".
40	$\overline{K}$	Kick. Input used for reducing continual short circuit current flow in torque receiver loads at false null.

FIGURE 2. Terminal connections.

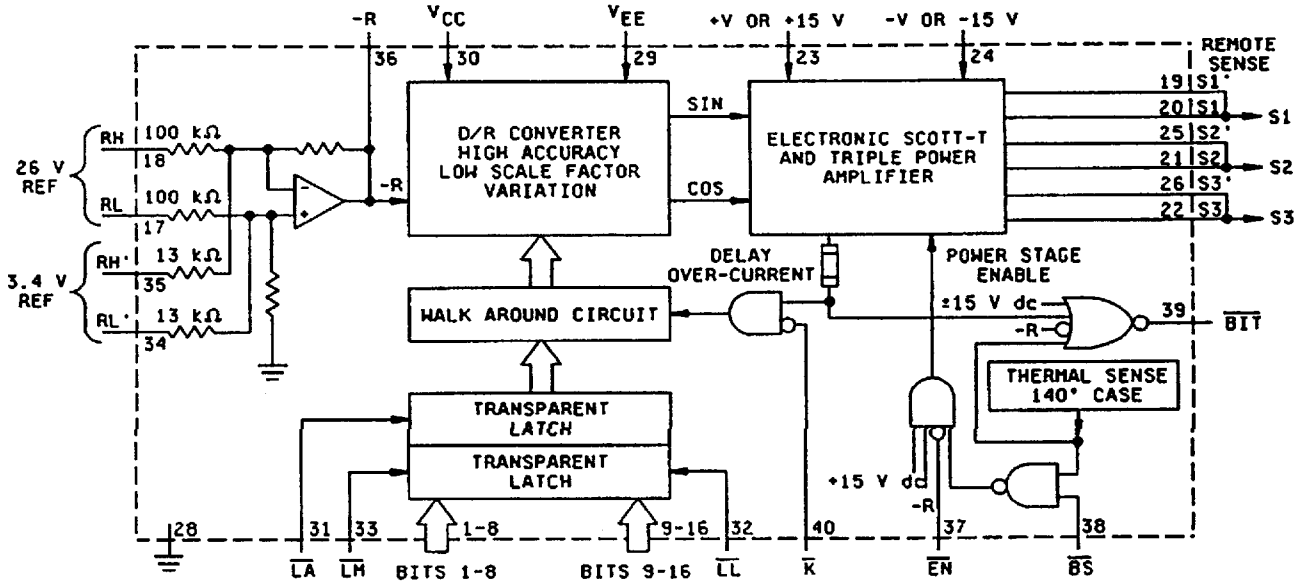


FIGURE 3. Block diagram.

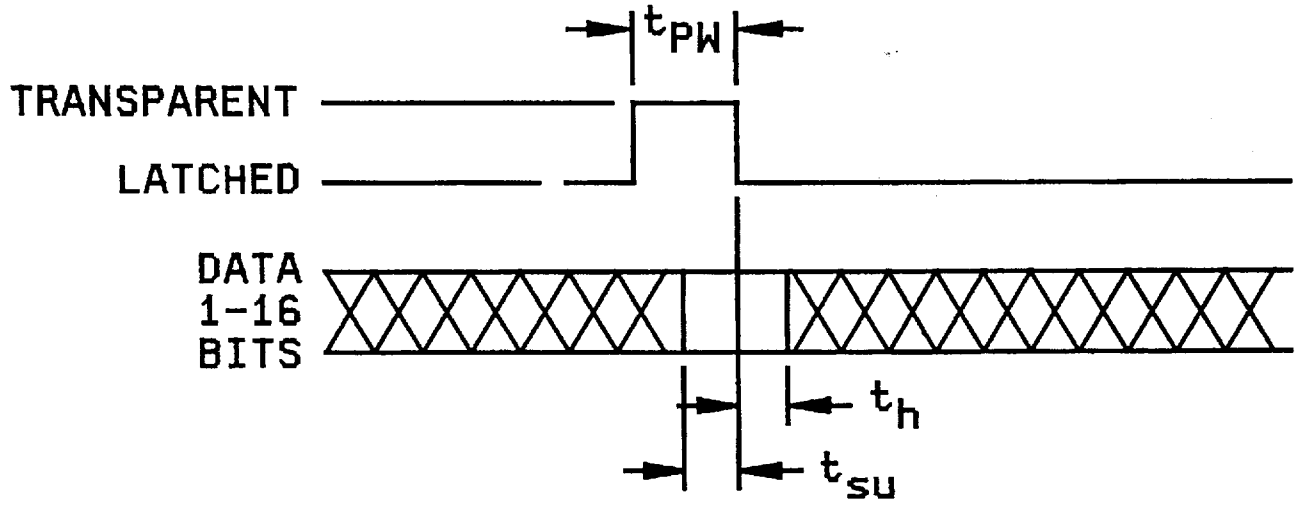


FIGURE 4. Timing diagram.

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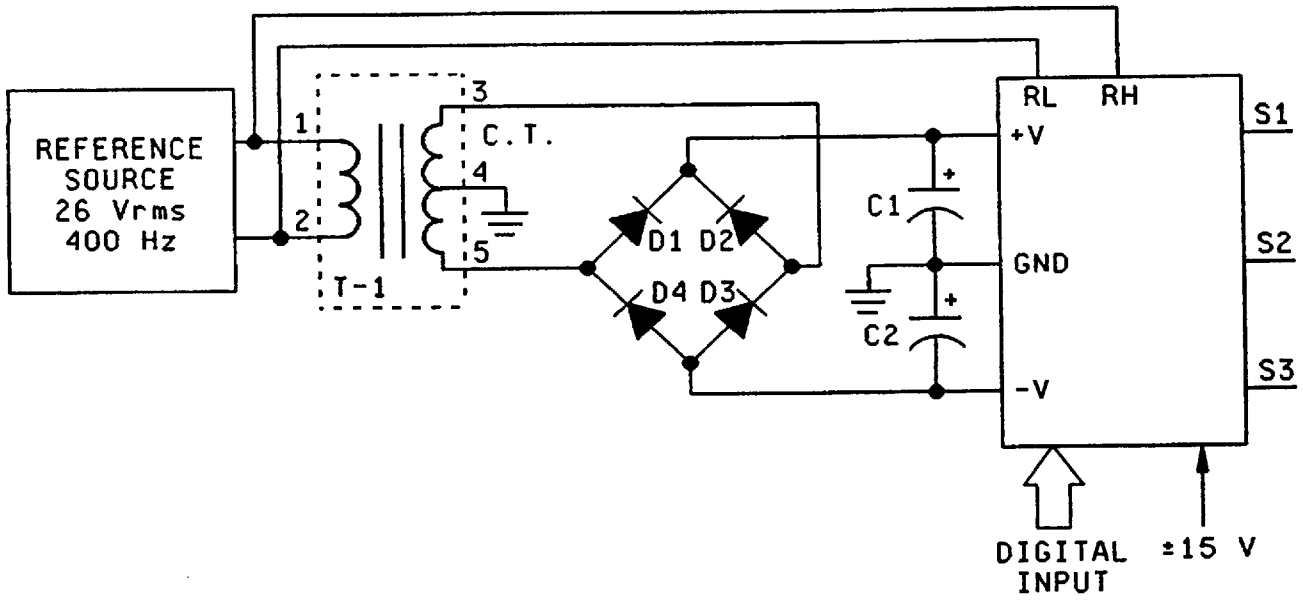

NOTES:
1. D1 through D4 are IN4004.
2. C1 and C2 are 22 µf, 35 V dc cpacitors.

FIGURE 5. Pulsating power source diagram.

TABLE II. Electrical test requirements.

MIL-H-38534 test requirements	Subgroups (in accordance with MIL-H-38534, group A test table)
Interim electrical parameters	1,4,7,9
Final electrical test parameters	1*,2,3,4,5,6,7,8,9, 10,11
Group A test requirements	1,2,3,4,5,6,7,8,9, 10,11
Group C end-point electrical parameters	1,2,3,4,5,6,7,8,9, 10,11
MIL-STD-883, group E end-point electrical parameters for RHA devices	Subgroups ** (in accordance with method 5005, group A test table)

* PDA applies to subgroup 1.
** When applicable to this standard microcircuit drawing, the subgroups shall be defined.

4.3 Quality conformance inspection. Quality conformance inspection shall be in accordance with MIL-H-38534 and as specified herein.

4.3.1 Group A inspection. Group A inspection shall be in accordance with MIL-H-38534 and as follows:

a. Tests shall be as specified in table II herein.

4.3.2 Group B inspection. Group B inspection shall be in accordance with MIL-H-38534.

4.3.3 Group C inspection. Group C inspection shall be in accordance with MIL-H-38534 and as follows:

a. End-point electrical parameters shall be as specified in table II herein.

b. Steady-state life test, method 1005 of MIL-STD-883.

(1) Test condition A, B, C, or D. The test circuit shall be maintained by the manufacturer under document revision level control and shall be made available to either DESC-EC or the acquiring activity upon request. Also, the test circuit shall specify the inputs, outputs, biases, and power dissipation, as applicable, in accordance with the intent specified in test method 1005 of MIL-STD-883.

(2) T_A as specified in accordance with table I of method 1005 of MIL-STD-883.

(3) Test duration: 1,000 hours, except as permitted by method 1005 of MIL-STD-883.

4.3.4 Group D inspection. Group D inspection shall be in accordance with MIL-H-38534.

4.3.5 Group E inspection. Group E inspection is required only for parts intended to be marked as radiation hardness assured (see 3.5 herein). RHA levels for device classes H and K shall be M, D, R, and H. RHA quality conformance inspection sample tests shall be performed at the RHA level specified in the acquisition document.

a. RHA tests for device classes H and K for levels M, D, R, and H shall be performed through each level to determine at what levels the devices meet the RHA requirements. These RHA tests shall be performed for initial qualification and after design or process changes which may affect the RHA performance of the device.

b. End-point electrical parameters shall be as specified in table II herein.

c. Prior to total dose irradiation, each selected sample shall be assembled in its qualified package. It shall pass the specified group A electrical parameters in table I for subgroups specified in table II herein.

d. For device classes H and K, the devices shall be subjected to radiation hardness assured tests as specified in MIL-H-38534 for RHA level being tested, and meet the postirradiation end-point electrical parameter limits as defined in table I at T_A = +25°C ±5 percent, after exposure.

e. Prior to and during total dose irradiation testing, the devices shall be biased to establish a worst case condition as specified in the radiation exposure circuit.

f. For device classes H and K, subgroups 1 and 2 in table V, method 5005 of MIL-STD-883 shall be tested as appropriate for device construction.

g. When specified in the purchase order or contract, a copy of the RHA delta limits shall be supplied.

5. PACKAGING

5.1 Packaging requirements. The requirements for packaging shall be in accordance with MIL-H-38534.

6. NOTES

6.1 Intended use. Microcircuits conforming to this drawing are intended for use for Government microcircuit applications (original equipment), design applications, and logistics purposes.

6.2 Replaceability. Microcircuits covered by this drawing will replace the same generic device covered by a contractor-prepared specification or drawing.

6.3 Configuration control of SMD's. All proposed changes to existing SMD's will be coordinated with the users of record for the individual documents. This coordination will be accomplished in accordance with MIL-STD-973 using DD Form 1692, Engineering Change Proposal.

6.4 Record of users. Military and industrial users shall inform Defense Electronics Supply Center when a system application requires configuration control and the applicable SMD. DESC will maintain a record of users and this list will be used for coordination and distribution of changes to the drawings. Users of drawings covering microelectronic devices (FSC 5962) should contact DESC-EC, telephone (513) 296-6047.

6.5 Comments. Comments on this drawing should be directed to DESC-EC, Dayton, Ohio 45444, or telephone (513) 296-5373.

6.6 One part - one part number system. The one part - one part number system described below has been developed to allow for transitions between identical generic devices covered by the three major microcircuit requirements documents (MIL-H-38534, MIL-I-38535, and 1.2.1 of MIL-STD-883) without the necessity for the generation of unique PIN's. The three military requirements documents represent different class levels, and previously when a device manufacturer upgraded military product from one class level to another, the benefits of the upgraded product were unavailable to the Original Equipment Manufacturer (OEM), that was contractually locked into the original unique PIN. By establishing a one part number system covering all three documents, the OEM can acquire to the highest class level available for a given generic device to meet system needs without modifying the original contract parts selection criteria.

Military documentation format	Example PIN under new system	Manufacturing source listing	Document listing
New MIL-H-38534 Standard Microcircuit Drawings	5962-XXXXXZZ(H or K)YY	QML-38534	MIL-BUL-103
New MIL-I-38535 Standard Microcircuit Drawings	5962-XXXXXZZ(Q or V)YY	QML-38535	MIL-BUL-103
New 1.2.1 of MIL-STD-883 Standard Microcircuit Drawings	5962-XXXXXZZ(M)YY	MIL-BUL-103	MIL-BUL-103

6.7 Sources of supply for device classes H and K. Sources of supply for device classes H and K are listed in QML-38534. The vendors listed in QML-38534 have submitted a certificate of compliance (see 3.7 herein) to DESC-EC and have agreed to this drawing.

Table III. Pin function, case X (dual-in-line).

Pin definitions:

GND	Power supply ground, Digital ground, and analog input ground.
D01-D016	Digital input bits, Bit 1 = MSB = 180 degrees, Bit 16 = LSB = .0055 degrees.
$\overline{LA}$	Logic high transfers, 8 bit input registers data into 16 bit holding register. Logic high for transparent operation, low latches.
$\overline{LM}$	High byte enable (Bits 1-8) for MSB's 8 bit input register. Logic high for transparent operation, low latches.
$\overline{LL}$	Low byte enable (Bits 9-16) for LSB's 8 bit input register. Logic high for transparent operation, low latches.
+V, -V	Power supply voltage for power stages.
V_{CC}, V_{EE}	Power supply voltages. **Caution:** REVERSAL OF POWER SUPPLIES WILL CAUSE DAMAGE TO THE CONVERTER
RH, RL	26V rms reference inputs.
RH', RL'	3.4V rms reference inputs.
S1, S2, S3	Synchro outputs.
S1', S2', S3'	Synchro output remote sense.
$\overline{BIT}$	Built-in-test output. Logic "0" indicates failure when loss of reference, loss of ±15V dc supply, case temperature of +140°C or an output over-current or short circuit has been detected. Logic "0" indicates over-current condition.
$\overline{K}$	Kick. Input used for reducing continual short circuit current flow in torque receiver loads at false null.
$\overline{BS}$	Battle short input. Power output stage is turned off if overtemp condition is detected. Logic "0" overrides over-temperature protection, and restores output.
$\overline{EN}$	Enable signal. Power stage enable control line input allows for digital shutdown of power stage. Gives complete control of converter to digital system.