| REVISIONS | | | |
|---|---|---|---|
| LTR | DESCRIPTION | DATE (YR-MO-DA) | APPROVED |
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| REV | | | | | | | | | | | | | | | | | | | |
| SHEET | 35 | 36 | 37 | 38 | 39 | 40 | 41 | 42 | 43 | 44 | 45 | | | | | | | | |
| REV | | | | | | | | | | | | | | | | | | | |
| SHEET | 15 | 16 | 17 | 18 | 19 | 20 | 21 | 22 | 23 | 24 | 25 | 26 | 27 | 28 | 29 | 30 | 31 | 32 | 33 | 34 |

| REV STATUS OF SHEETS | REV | | | | | | | | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | SHEET | 1 | 2 | 3 | 4 | 5 | 6 | 7 | 8 | 9 | 10 | 11 | 12 | 13 | 14 |

PMIC N/A

**STANDARDIZED MILITARY DRAWING**

THIS DRAWING IS AVAILABLE FOR USE BY ALL DEPARTMENTS AND AGENCIES OF THE DEPARTMENT OF DEFENSE

AMSC N/A

PREPARED BY
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APPROVED BY

DRAWING APPROVAL DATE
92-03-05

REVISION LEVEL

DEFENSE ELECTRONICS SUPPLY CENTER
DAYTON, OHIO 45444

MICROCIRCUIT, MEMORY, DIGITAL, CMOS
4M x 1 DYNAMIC RANDOM ACCESS MEMORY
(DRAM) MONOLITHIC SILICON

| SIZE | CAGE CODE | 5962-90622 |
|---|---|---|
| A | 67268 | |

SHEET 1 OF 45

DESC FORM 193
JUL 91

5962-E246

DISTRIBUTION STATEMENT A. Approved for public release; distribution is unlimited.

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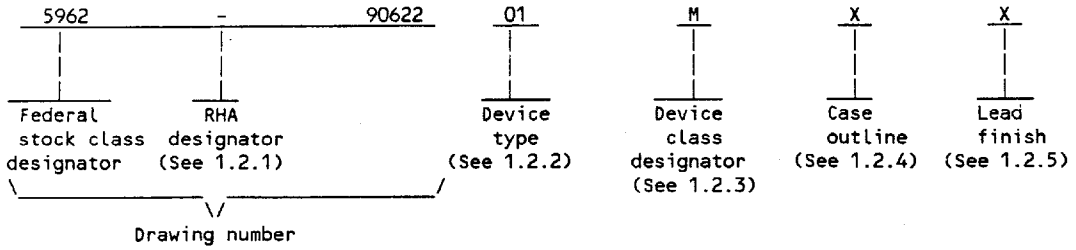
1. SCOPE

1.1 Scope. This drawing forms a part of a one part - one part number documentation system (see 6.6 herein). Two product assurance classes consisting of military high reliability (device classes B, Q, and M) and space application (device classes S and V), and a choice of case outlines and lead finishes are available and are reflected in the Part or Identifying Number (PIN). Device class M microcircuits represent non-JAN class B microcircuits in accordance with 1.2.1 of MIL-STD-883, "Provisions for the use of MIL-STD-883 in conjunction with compliant non-JAN devices". When available, a choice of radiation hardness assurance (RHA) levels are reflected in the PIN.

1.2 PIN. The PIN shall be as shown in the following example:




1.2.1 Radiation hardness assurance (RHA) designator. Device classes M, B, and S RHA marked devices shall meet the MIL-M-38510 specified RHA levels and shall be marked with the appropriate RHA designator. Device classes Q or V devices shall meet or exceed the electrical performance characteristics specified in table IA herein after exposure to the specified irradiation levels specified in the absolute maximum ratings herein and the RHA marked device shall be marked in accordance with MIL-I-38535. A dash (-) indicates a non RHA device.

1.2.2 Device type(s). The device type(s) shall identify the circuit function as follows:

| Device type | Generic number 1/ | Circuit function | Access time |
|---|---|---|---|
| 01 | | 4M x 1 Dynamic random access memory | 120 ns |
| 02 | | 4M x 1 Dynamic random access memory | 100 ns |
| 03 | | 4M x 1 Dynamic random access memory | 80 ns |

1.2.3 Device class designator. The device class designator shall be a single letter identifying the product assurance level (see 6.7 herein) as follows:

| Device class | Device requirements documentation |
|---|---|
| M | Vendor self-certification to the requirements for non-JAN class B microcircuits in accordance with 1.2.1 of MIL-STD-883 |
| B or S | Certification and qualification to MIL-M-38510 |
| Q or V | Certification and qualification to MIL-I-38535 |

1.2.4 Case outline(s). For device classes M, B, and S, case outline(s) shall meet the requirements in appendix C of MIL-M-38510 and as listed below. For device classes Q and V, case outline(s) shall meet the requirements of MIL-I-38535, appendix C of MIL-M-38510, and as listed below.

| Outline letter | Case outline |
|---|---|
| X | See figure 1, (20-lead, 0.710" x 0.497" x 0.100"), flat package (top brazed) |
| Y | See figure 1, (26/20-terminal, .710" x .407" x .092"), rectangular chip carrier package |
| Z | See figure 1, (26/20-terminal, .685" x .370" x .160"), rectangular chip carrier J-leaded package |
| U | See figure 1, (26/20-terminal, .685" x .357" x .080"), rectangular chip carrier package |
| T | See figure 1, (18-lead, .910" x .410" x .140"), dual in-line package |
| N | See figure 1, (20-lead, 1.050" x .395" x .105"), zig-zag in-line package |
| V | D-6 (18-lead, .960" x .310" x .200"), dual-in-line package |
| M | See figure 1, (20-lead, .708" x .415" x .117"), flat package (bottom brazed) |

1/ Generic numbers are listed on the Standardized Military Drawing Source Approval Bulletin at the end of this document and will also be listed in MIL-BUL-103 (see 6.7.3 herein).

1.2.5 Lead finish. The lead finish shall be as specified in MIL-M-38510 for classes M, B, and S or MIL-I-38535 for classes Q and V. Finish letter "X" shall not be marked on the microcircuit or its packaging. The "X" designation is for use in specifications when lead finishes A, B, and C are considered acceptable and interchangeable without preference.

1.3 Absolute maximum ratings. 2/

| | |
|---|---|
| Voltage range on any pin | -1.0 V dc to 7.0 V dc |
| Voltage range on $V_{CC}$ | -1.0 V dc to 7.0 V dc |
| Short circuit output current | 50 mA |
| Maximum power dissipation ($P_D$) | 1 W |
| Storage temperature range | -65°C to +150°C |
| Thermal resistance, junction-to-case ($\theta_{JC}$): | |
| Case outline V | See MIL-M-38510, appendix C |
| Case outlines X, Y, Z, U, T, N, and M | 20°C/ 3/ |
| Junction temperature ($T_J$) 4/ | +175°C |

1.4 Recommended operating conditions.

| | |
|---|---|
| Supply voltage range ($V_{CC}$) 5/ | +4.5 V dc to +5.5 V dc |
| High level input voltage range ($V_{IH}$) | 2.4 V dc minimum to 6.5 V dc maximum |
| Low level input voltage range ($V_{IL}$) 6/ | -1.0 V dc minimum to 0.8 V dc maximum |
| Case operating temperature range ($T_C$) | -55°C to +125°C |

1.5 Logic testing for device classes Q and V.

| | |
|---|---|
| Fault coverage measurement of manufacturing logic tests (MIL-STD-883, test method 5012) | 7/ percent |

2. APPLICABLE DOCUMENTS

2.1 Government specifications, standards, bulletin, and handbook. Unless otherwise specified, the following specifications, standards, bulletin, and handbook of the issue listed in that issue of the Department of Defense Index of Specifications and Standards specified in the solicitation, form a part of this drawing to the extent specified herein.

SPECIFICATIONS

MILITARY

MIL-M-38510 - Microcircuits, General Specification for.
MIL-I-38535 - Integrated Circuits, Manufacturing, General Specification for

STANDARDS

MILITARY

MIL-STD-480 - Configuration Control-Engineering Changes, Deviations and Waivers.
MIL-STD-883 - Test Methods and Procedures for Microelectronics.

2/ Stresses above the absolute maximum rating may cause permanent damage to the device. Extended operation at the maximum levels may degrade performance and affect reliability.

3/ When a thermal resistance for this case is specified in MIL-M-38510, appendix C, that value shall supercede the value indicated herein.

4/ Maximum junction temperature shall not be exceeded except for allowable short duration burn-in screening conditions in accordance with method 5004 of MIL-STD-883.

5/ All voltage values in this drawing are with respect to $V_{SS}$.

6/ The algebraic convention, where the more negative (less positive) limit is designated as a minimum, is used in this drawing for logic voltage levels only.

7/ When a QML source exists, a value shall be provided.

BULLETIN

MILITARY

MIL-BUL-103 - List of Standardized Military Drawings (SMD's).

HANDBOOK

MILITARY

MIL-HDBK-780 - Military Drawings

(Copies of the specifications, standards, bulletin, and handbook required by manufacturers in connection with specific acquisition functions should be obtained from the contracting activity or as directed by the contracting activity.)

2.2 Non-Government publications. The following documents form a part of this document to the extent specified herein. Unless otherwise specified, the issues of the documents which are DoD adopted are those listed in the issue of the DODISS cited in the solicitation. Unless otherwise specified, the issues of documents not listed in the DODISS are the issues of the documents cited in the solicitation.

ELECTRONICS INDUSTRIES ASSOCIATION (EIA)

JEDEC Standard No. 17 - A Standardized Test Procedure for the Characterization of LATCH-UP in CMOS Integrated Circuits.

(Applications for copies should be addressed to the Electronics Industries Association, 2001 Pennsylvania Street, N.W., Washington, DC 20006.)

AMERICAN SOCIETY FOR TESTING AND MATERIALS (ASTM)

ASTM Standard F1192-88 - Standard Guide for the Measurement of Single Event Phenomena from Heavy Ion Irradiation of Semiconductor Devices.

(Applications for copies of ASTM publications should be addressed to the American Society for Testing and Materials, 1916 Race Street, Philadelphia, Pennsylvania 19103).

(Non-Goverment standards and other publications are normally available from the organizations that prepare or distribute the documents. These documents also may be available in or through libraries or other informational services.)

2.3 Order of precedence. In the event of a conflict between the text of this drawing and the references cited herein, the text of this drawing shall take precedence.

3. REQUIREMENTS

3.1 Item requirements. The individual item requirements for device class M shall be in accordance with 1.2.1 of MIL-STD-883, "Provisions for the use of MIL-STD-883 in conjunction with compliant non-JAN devices" and as specified herein. The individual item requirements for device classes B and S shall be in accordance with MIL-M-38510 and as specified herein. This is a fully characterized military detail specification and is suitable for qualification of device classes B and S to the requirements of MIL-M-38510. The individual item requirements for device classes Q and V shall be in accordance with MIL-I-38535, the device manufacturer's Quality Management (QM) plan, and as specified herein.

3.2 Design, construction, and physical dimensions. The design, construction, and physical dimensions shall be as specified in MIL-M-38510 for device classes M, B, and S and MIL-I-38535 for device classes Q and V and herein.

3.2.1 Case outline. The case outline shall be in accordance with 1.2.4 herein and figure 1.

3.2.2 Terminal connections. The terminal connections shall be as specified on figure 2.

3.2.3 Truth table. The truth table shall be as specified on figure 3.

3.2.4 Radiation exposure circuit. The radiation exposure circuit shall be as specified in 4.4.5e.

3.2.5 Functional tests. Various functional tests used to test this device are contained in the appendix. If the test patterns cannot be implemented due to test equipment limitations, alternate test patterns to accomplish the same results shall be submitted to DESC-ECS for device class M. For device classes B and S, the test patterns shall be submitted to the qualifying activity for approval. For device classes Q and V, the test patterns shall be submitted to DESC-ECS and shall also be under the control of the device manufacturer's technical review board (TRB) in accordance with MIL-I-38535.

3.2.6 Die overcoat. For device classes B and S, polyimide and silicone coatings are allowable as an overcoat on the die for alpha particle protection provided that each coated microcircuit inspection lot (see MIL-M-38510, inspection lot - class B) shall be subjected to and pass the internal moisture content test at 5000 ppm (method 1018 of MIL-STD-883). The frequency of the internal water vapor testing shall not be decreased unless approved by the preparing activity. Samples may be pulled any time after seal.

3.3 Electrical performance characteristics and postirradiation parameter limits. Unless otherwise specified herein, the electrical performance characteristics and postirradiation parameter limits are as specified in table IA and shall apply over the full case operating temperature range.

3.4 Electrical test requirements. The electrical test requirements shall be the subgroups specified in table IIA. The electrical tests for each subgroup are defined in table IA.

3.5 Marking. The part shall be marked with the PIN listed in 1.2 herein. Marking for device class M shall be in accordance with MIL-STD-883 (see 3.1 herein). In addition, the manufacturer's PIN may also be marked as listed in MIL-BUL-103. Marking for device classes B and S shall be in accordance with MIL-M-38510. Marking for device classes Q and V shall be in accordance with MIL-I-38535.

3.5.1 Certification/compliance mark. The compliance mark for device class M shall be a "C" as required in MIL-STD-883 (see 3.1 herein). The certification mark for device classes B and S shall be a "J" or "JAN" as required in MIL-M-38510. The certification mark for device classes Q and V shall be a "QML" as required in MIL-I-38535.

3.6 Certificate of compliance. For device class M, a certificate of compliance shall be required from a manufacturer in order to be listed as an approved source of supply in MIL-BUL-103 (see 6.7.3 herein). For device classes Q and V, a certificate of compliance shall be required from a QML-38535 listed manufacturer in order to supply to the requirements of this drawing (see 6.7.2 herein). The certificate of compliance submitted to DESC-ECS prior to listing as an approved source of supply for this drawing shall affirm that the manufacturer's product meets, for device class M the requirements of MIL-STD-883 (see 3.1 herein), or for device classes Q and V, the requirements of MIL-I-38535 and the requirements herein.

3.7 Certificate of conformance. A certificate of conformance as required for device class M in MIL-STD-883 (see 3.1 herein) or device classes B and S in MIL-M-38510 or for device classes Q and V in MIL-I-38535 shall be provided with each lot of microcircuits delivered to this drawing.

3.8 Notification of change for device class M. For device class M, notification to DESC-ECS of change of product (see 6.2 herein) involving devices acquired to this drawing is required for any change as defined in MIL-STD-480.

3.9 Verification and review for device class M. For device class M, DESC, DESC's agent, and the acquiring activity retain the option to review the manufacturer's facility and applicable required documentation. Offshore documentation shall be made available onshore at the option of the reviewer.

3.10 Microcircuit group assignment for device classes M, B, and S. Device classes M, B, and S devices covered by this drawing shall be in microcircuit group number 41 (see MIL-M-38510, appendix E).

3.11 Serialization for device class S. All device class S devices shall be serialized in accordance with MIL-M-38510.

4. QUALITY ASSURANCE PROVISIONS

4.1 Sampling and inspection. For device class M, sampling and inspection procedures shall be in accordance with section 4 of MIL-M-38510 to the extent specified in MIL-STD-883 (see 3.1 herein). For device classes B and S sampling and inspection procedures shall be in accordance with MIL-M-38510 and method 5005 of MIL-STD-883, except as modified herein. For device classes Q and V sampling and inspection procedures shall be in accordance with MIL-I-38535 and the device manufacturer's QM plan.

4.2 Screening. For device class M, screening shall be in accordance with method 5004 of MIL-STD-883, and shall be conducted on all devices prior to quality conformance inspection. For device classes B and S, screening shall be in accordance with method 5004 of MIL-STD-883, and shall be conducted on all devices prior to qualification and quality conformance inspection. For device classes Q and V, screening shall be in accordance with MIL-I-38535, and shall be conducted on all devices prior to qualification and technology conformance inspection.

4.2.1 Additional criteria for device classes M, B, and S.

a. Delete the sequence specified as initial (pre-burn-in) electrical parameters through interim (post-burn-in) electrical parameters of method 5004 and substitute lines 1 through 6 of table IIA herein.

b. For device class M, the burn-in test circuit shall be submitted to DESC-ECS for review with the certificate of compliance. For device classes B and S, the burn-in test circuit shall be submitted to the qualifying activity.

(1) Static burn-in for device class S (method 1015 of MIL-STD-883, test condition A).

(a) All inputs shall be connected to GND. Outputs may be open or connected to 4.5 V minimum. Resistors R1 are optional on both inputs and outputs, and required on outputs connected to $V_{CC}$±0.5 V. R1 = 220 ohms to 47 kilohms. For static II burn-in, reverse all input connections (i.e. $V_{SS}$ to $V_{CC}$).

(b) $V_{CC}$ = 4.5 V minimum.

(c) Ambient temperature ($T_A$) shall be +125°C minimum.

(d) Test duration for the static test shall be 48 hours minimum. The 48 hour burn-in shall be broken into two sequences of 24 hours each (Static I and Static II) followed by interim electrical measurements.

(2) Dynamic burn-in for device classes M, B, and S (method 1015 of MIL-STD-883, test condition D) using the circuit submitted (see 4.2b herein).

c. Interim and final electrical parameters shall be as specified in table IIA herein.

d. For classes S and B devices, post dynamic burn-in electrical parameter measurements may, at the manufacturer's option, be performed separately or included in the final electrical parameter requirements.

4.2.2 Additional criteria for device classes Q and V.

a. The burn-in test duration, test condition and test temperature or approved alternatives shall be as specified in the device manufacturer's QM plan in accordance with MIL-I-38535. The burn-in test circuit shall be submitted to DESC-ECS with the certificate of compliance and shall be under the control of the device manufacturer's Technology Review Board (TRB) in accordance with MIL-I-38535.

b. Interim and final electrical test parameters shall be as specified in table IIA herein.

c. Additional screening for device class V beyond the requirements of device class Q shall be as specified in appendix B of MIL-I-38535 and as detailed in table IIB herein.

d. Additional requirements beyond MIL-I-38535 for classes Q and V are specified in table IIA herein.

4.2.3 Percent defective allowable (PDA).

a. The PDA for class S devices shall be 5 percent for static burn-in and 5 percent for dynamic burn-in, based on the exact number of devices submitted to each seperate burn-in.

b. The PDA for class B devices shall be in accordance with MIL-M-38510 for dynamic burn-in.

c. Static burn-in I and II failures shall be cumulative for determining PDA.

d. Those devices whose measured characteristics, after burn-in, exceed the specified delta ($\Delta$) limits or electrical parameter limits specified in table IA, subgroup 1, are defective and shall be removed from the lot. The verified failures divided by the total number of devices in the lot initially submitted to burn-in shall be used to determine the percent defective for the lot and the lot shall be accepted or rejected based on the specifed PDA.

e. The PDA for device classes Q and V shall be in accordance with MIL-I-38535 for dynamic burn-in.

4.3 Qualification inspection.

4.3.1 Qualification inspection for device classes B and S. Qualification inspection for device classes B and S shall be in accordance with MIL-M-38510. Inspections to be performed shall be those specified in method 5005 of MIL-STD-883 and herein for groups A, B, C, D, and E inspections (see 4.4.1 through 4.4.5). Qualification data for subgroups 7, 8A, and 8B shall be attributes only.

4.3.1.1 Qualification extension for device class B and S. When authorized by the qualifying activity, if a manufacturer qualifies one device type which is identical (i.e., same die) to other device types on this specification, the slower device types may be part I qualified, upon the request of the manufacturer, without any further testing. The faster device types may be part I qualified by performing only group A qualification testing.

4.3.2 Qualification inspection for device classes Q and V. Qualification inspection for device classes Q or V shall be in accordance with MIL-I-38535. Inspections to be performed shall be those specified in MIL-I-38535 and herein for groups A, B, C, D, and E inspections (see 4.4.1 through 4.4.5).

4.3.3 Electrostatic discharge sensitivity inspection. Electrostatic discharge sensitivity (ESDS) testing shall be performed in accordance with MIL-STD-883, method 3015. ESDS testing shall be measured only for initial qualification and after process or design changes which may affect ESDS classification.

4.4 Conformance inspection. Quality conformance inspection for device class M shall be in accordance with MIL-STD-883 (see 3.1 herein) and as specified herein. Quality conformance inspection for device classes B and S shall be in accordance with MIL-M-38510 and as specified herein. Inspections to be performed for device classes M, B, and S shall be those specified in method 5005 of MIL-STD-883 and herein for groups A, B, C, D, and E inspections (see 4.4.1 through 4.4.5). Technology conformance inspection for classes Q and V shall be in accordance with MIL-I-38535 including groups A, B, C, D, and E inspections and as specified herein except where option 2 of MIL-I-38535 permits alternate in-line control testing.

TABLE IA. Electrical performance characteristics.

| Test | Symbol | Conditions<br>$-55°C \le T_C \le +125°C$<br>$4.5\ V \le V_{CC} \le 5.5\ V$<br>unless otherwise specified | Group A subgroups | Device type | Limits | | Unit |
|---|---|---|---|---|---|---|---|
| | | | | | Min | Max | |
| High level output voltage | $V_{OH}$ | $V_{CC}$ = 4.5 V, $I_{OH}$ = -5 mA,<br>$V_{IL}$ = .8 V, $V_{IH}$ = 2.4 V | 1,2,3 | All | 2.4 | | V |
| Low level output voltage | $V_{OL}$ | $V_{CC}$ = 4.5 V, $I_{OL}$ = 4.2 mA,<br>$V_{IL}$ = .8 V, $V_{IH}$ = 2.4 V | 1,2,3 | All | | 0.4 | V |
| Input leakage current | $I_I$ | $V_I$ = 0 V to 6.5 V,<br>$V_{CC}$ = 5.5 V,<br>All other pins = 0 V to $V_{CC}$ | 1,2,3 | All | | ±10 | µA |
| Output leakage current | $I_O$ | $V_{CC}$ = 5.5 V, $\overline{CAS}$ high,<br>$V_O$ = $V_{CC}$ to 0 V | 1,2,3 | All | | ±10 | µA |
| Power supply current read or write cycle | $I_{CC1}$ | Minimum cycle,<br>$V_{CC}$ = 5.5 V<br>Measured for a maximum of one address transition while<br>$\overline{RAS}$ = $V_{IL}$ | 1,2,3 | 01 | | 70 | mA |
| | | | | 02 | | 80 | |
| | | | | 03 | | 85 | |
| Power supply current standby | $I_{CC2}$ | After 1 memory cycle,<br>$\overline{RAS}$ and $\overline{CAS}$ high,<br>$V_{IH}$ = 2.4 V | 1,2,3 | All | | 4 | mA |
| Power supply current average refresh ($\overline{RAS}$-only or CBR) | $I_{CC3}$ | $V_{CC}$ = 5.5 V, minimum cycle,<br>$\overline{RAS}$ cycling, $\overline{CAS}$ high ($\overline{RAS}$-only)<br>$\overline{RAS}$ low after $\overline{CAS}$ low (CBR)<br>Measured for a maximum of one address transition while<br>$\overline{RAS}$ = $V_{IL}$ | 1,2,3 | 01 | | 65 | mA |
| | | | | 02 | | 75 | |
| | | | | 03 | | 85 | |
| Power supply current average page | $I_{CC4}$ | $\overline{RAS}$ low, $\overline{CAS}$ cycling,<br>$t_{PC}$ = minimum,<br>$V_{CC}$ = 5.5 V<br>Measured for a maximum of one address transition while<br>$\overline{CAS}$ = $V_{IH}$ | 1,2,3 | 01 | | 40 | mA |
| | | | | 02 | | 50 | |
| | | | | 03 | | 60 | |

See footnotes at end of table.

TABLE IA. Electrical performance characteristics - Continued.

| Test | Symbol | Conditions<br>$-55°C \le T_C \le +125°C$<br>$4.5\ V \le V_{CC} \le 5.5\ V$<br>unless otherwise specified | Group A subgroups | Device type | Limits | | Unit |
|---|---|---|---|---|---|---|---|
| | | | | | Min | Max | |
| Input capacitance, address inputs | $C_I(A)$ | f = 1 MHz See 4.4.1e<br>Bias on pins under test = 0 V | 4 | All | | 7 | pF |
| Input capacitance, data inputs | $C_I(D)$ | $V_{CC}$ = 5.0 V nominal | 4 | All | | 7 | pF |
| Input capacitance, strobe inputs | $C_I(S)$ | | 4 | All | | 10 | pF |
| Input capacitance, write-enable inputs | $C_I(W)$ | | 4 | All | | 10 | pF |
| Output capacitance | $C_O$ | | 4 | All | | 10 | pF |
| Access time from column address | $t_{AA}$ | See figures 4 and 5<br>1/ | 9,10,11 | 01 | | 55 | ns |
| | | | | 02 | | 50 | |
| | | | | 03 | | 40 | |
| Access time from $\overline{CAS}$ low | $t_{CAC}$ | | 9,10,11 | 01 | | 30 | ns |
| | | | | 02 | | 25 | |
| | | | | 03 | | 20 | |
| Access time from column precharge | $t_{CPA}$ | | 9,10,11 | 01 | | 55 | ns |
| | | | | 02 | | 50 | |
| | | | | 03 | | 45 | |
| Access time from $\overline{RAS}$ low | $t_{RAC}$ | | 9,10,11 | 01 | | 120 | ns |
| | | | | 02 | | 100 | |
| | | | | 03 | | 80 | |
| Output disable time after $\overline{CAS}$ high 2/ | $t_{OFF}$ | | 9,10,11 | 01 | | 30 | ns |
| | | | | 02 | | 25 | |
| | | | | 03 | | 20 | |
| Cycle time, random read or write 3/ | $t_{RC}$ | | 9,10,11 | 01 | 210 | | ns |
| | | | | 02 | 180 | | |
| | | | | 03 | 150 | | |

See footnotes at end of table.

TABLE IA. Electrical performance characteristics - Ccontinued.

| Test | Symbol | Conditions<br>$-55°C \le T_C \le +125°C$<br>$4.5\ V \le V_{CC} \le 5.5\ V$<br>unless otherwise specified | Group A subgroups | Device type | Limits | | Unit |
|---|---|---|---|---|---|---|---|
| | | | | | Min | Max | |
| Cycle time, read-write | $t_{RWC}$ | See figures 4 and 5<br>1/ | 9,10,11 | 01 | 255 | | ns |
| | | | | 02 | 220 | | |
| | | | | 03 | 205 | | |
| Cycle time, page-mode read or write 4/ | $t_{PC}$ | | 9,10,11 | 01 | 65 | | ns |
| | | | | 02 | 60 | | |
| | | | | 03 | 50 | | |
| Cycle time, page-mode read-write | $t_{PRWC}$ | | 9,10,11 | 01 | 135 | | ns |
| | | | | 02 | 115 | | |
| | | | | 03 | 100 | | |
| Pulse duration, page-mode, $\overline{RAS}$ low 5/ | $t_{RASP}$ | | 9,10,11 | 01 | 120 | | ns |
| | | | | 02 | 100 | | |
| | | | | 03 | 80 | | |
| | | | | All | | 100 | µs |
| Pulse duration, non-page-mode, $\overline{RAS}$ low 5/ | $t_{RAS}$ | | 9,10,11 | 01 | 120 | | ns |
| | | | | 02 | 100 | | |
| | | | | 03 | 80 | | |
| | | | | All | | 10 | µs |
| Pulse duration, $\overline{CAS}$ low 6/ | $t_{CAS}$ | | 9,10,11 | 01 | 30 | | ns |
| | | | | 02 | 25 | | |
| | | | | 03 | 20 | | |
| | | | | All | | 10 | µs |
| Pulse duration, $\overline{CAS}$ high | $t_{CP}$ | | 9,10,11 | 01 | 15 | | ns |
| | | | | 02 | 12 | | |
| | | | | 03 | 12 | | |

See footnotes at end of table.

TABLE IA. Electrical performance characteristics - Continued.

| Test | Symbol | Conditions<br>$-55°C \le T_C \le +125°C$<br>$4.5\ V \le V_{CC} \le 5.5\ V$<br>unless otherwise specified | Group A subgroups | Device type | Limits | | Unit |
|---|---|---|---|---|---|---|---|
| | | | | | Min | Max | |
| Pulse duration, RAS high (precharge) | $t_{RP}$ | See figures 4 and 5<br>1/ | 9,10,11 | 01 | 80 | | ns |
| | | | | 02 | 70 | | |
| | | | | 03 | 60 | | |
| Pulse duration, write | $t_{WP}$ | | 9,10,11 | 01 | 25 | | ns |
| | | | | 02 | 20 | | |
| | | | | 03 | 15 | | |
| Setup time, column-address before CAS low | $t_{ASC}$ | | 9,10,11 | All | 0 | | ns |
| Setup time, row-address before RAS low | $t_{ASR}$ | | 9,10,11 | All | 0 | | ns |
| Setup time, data 7/ | $t_{DS}$ | | 9,10,11 | All | 0 | | ns |
| Setup time, read before CAS low | $t_{RCS}$ | | 9,10,11 | All | 0 | | ns |
| Setup time, W low before CAS high | $t_{CWL}$ | | 9,10,11 | 01 | 30 | | ns |
| | | | | 02 | 25 | | |
| | | | | 03 | 20 | | |
| Setup time, W low before RAS high | $t_{RWL}$ | | 9,10,11 | 01 | 30 | | ns |
| | | | | 02 | 25 | | |
| | | | | 03 | 20 | | |
| Setup time, W low before CAS low (Early write operation only) | $t_{WCS}$ | | 9,10,11 | All | 0 | | ns |
| Setup time, W high (CAS before RAS refresh only) | $t_{WSR}$ | | 9,10,11 | All | 10 | | ns |
| Hold time, column-address after CAS low | $t_{CAH}$ | | 9,10,11 | 01 | 20 | | ns |
| | | | | 02 | 20 | | |
| | | | | 03 | 15 | | |

See footnotes at end of table.

TABLE IA. Electrical performance characteristics - Continued.

| Test | Symbol | Conditions<br>$-55°C \le T_C \le +125°C$<br>$4.5\ V \le V_{CC} \le 5.5\ V$<br>unless otherwise specified | Group A subgroups | Device type | Limits | | Unit |
|---|---|---|---|---|---|---|---|
| | | | | | Min | Max | |
| Hold time, data 7/ | $t_{DH}$ | See figures 4 and 5 1/ | 9,10,11 | 01 | 25 | | ns |
| | | | | 02 | 20 | | |
| | | | | 03 | 15 | | |
| Hold time, data after RAS low | $t_{DHR}$ | | 9,10,11 | 01 | 90 | | ns |
| | | | | 02 | 75 | | |
| | | | | 03 | 60 | | |
| Hold time, column address after RAS low 8/ | $t_{AR}$ | | 9,10,11 | 01 | 90 | | ns |
| | | | | 02 | 75 | | |
| | | | | 03 | 60 | | |
| Hold time, row-address after RAS low | $t_{RAH}$ | | 9,10,11 | 01 | 15 | | ns |
| | | | | 02 | 15 | | |
| | | | | 03 | 10 | | |
| Hold time, read after CAS high 9/ | $t_{RCH}$ | | 9,10,11 | All | 0 | | ns |
| Hold time, read after RAS high 9/ | $t_{RRH}$ | | 9,10,11 | All | 0 | | ns |
| Hold time, write after CAS low (Early write operation only) | $t_{WCH}$ | | 9,10,11 | 01 | 25 | | ns |
| | | | | 02 | 20 | | |
| | | | | 03 | 15 | | |
| Hold time, write after RAS low 6/ | $t_{WCR}$ | | 9,10,11 | 01 | 90 | | ns |
| | | | | 02 | 75 | | |
| | | | | 03 | 60 | | |
| Hold time, $\overline{W}$ high (CAS-before-RAS refresh only) | $t_{WHR}$ | | 9,10,11 | All | 10 | | ns |
| Delay time, column address to $\overline{W}$ low (Read-write operation only) | $t_{AWD}$ | | 9,10,11 | 01 | 60 | | ns |
| | | | | 02 | 50 | | |
| | | | | 03 | 40 | | |

See footnotes at end of table.

TABLE IA. Electrical performance characteristics - Continued.

| Test | Symbol | Conditions $-55°C \le T_C \le +125°C$, $4.5\ V \le V_{CC} \le 5.5\ V$ unless otherwise specified | Group A subgroups | Device type | Limits | | Unit |
|---|---|---|---|---|---|---|---|
| | | | | | Min | Max | |
| Delay time, $\overline{CAS}$ high to $\overline{RAS}$ low | $t_{CRP}$ | See figures 4 and 5 1/ | 9,10,11 | 01 | 10 | | ns |
| | | | | 02,03 | 5 | | |
| Delay time, $\overline{RAS}$ low to $\overline{CAS}$ high ($\overline{CAS}$-before-$\overline{RAS}$ refresh only) | $t_{CHR}$ | | 9,10,11 | 01 | 25 | | ns |
| | | | | 02 | 20 | | |
| | | | | 03 | 20 | | |
| Delay time, $\overline{RAS}$ low to $\overline{CAS}$ high | $t_{CSH}$ | | 9,10,11 | 01 | 120 | | ns |
| | | | | 02 | 100 | | |
| | | | | 03 | 80 | | |
| Delay time, $\overline{CAS}$ low to $\overline{RAS}$ low ($\overline{CAS}$-before-$\overline{RAS}$ refresh only) | $t_{CSR}$ | | 9,10,11 | All | 10 | | ns |
| Delay time, $\overline{CAS}$ low to $\overline{W}$ low (Read-write operation only) | $t_{CWD}$ | | 9,10,11 | 01 | 30 | | ns |
| | | | | 02 | 25 | | |
| | | | | 03 | 20 | | |
| Delay time, $\overline{RAS}$ low to column-address 10/ | $t_{RAD}$ | | 9,10,11 | 01 | 20 | 65 | ns |
| | | | | 02 | 20 | 50 | |
| | | | | 03 | 15 | 40 | |
| Delay time, column-address to $\overline{RAS}$ high | $t_{RAL}$ | | 9,10,11 | 01 | 55 | | ns |
| | | | | 02 | 50 | | |
| | | | | 03 | 40 | | |
| Delay time, column-address to $\overline{CAS}$ high | $t_{CAL}$ | | 9,10,11 | 01 | 55 | | ns |
| | | | | 02 | 50 | | |
| | | | | 03 | 40 | | |
| Delay time, $\overline{RAS}$ low to $\overline{CAS}$ low 10/ | $t_{RCD}$ | | 9,10,11 | 01 | 25 | 90 | ns |
| | | | | 02 | 25 | 75 | |
| | | | | 03 | 20 | 60 | |
| Delay time, $\overline{CAS}$ low to $\overline{RAS}$ high | $t_{RSH}$ | | 9,10,11 | 01 | 30 | | ns |
| | | | | 02 | 25 | | |
| | | | | 03 | 20 | | |

See footnotes at end of table.

TABLE IA. Electrical performance characteristics - Continued.

| Test | Symbol | Conditions $-55°C \le T_C \le +125°C$, $4.5\ V \le V_{CC} \le 5.5\ V$ unless otherwise specified | Group A subgroups | Device type | Limits | | Unit |
|---|---|---|---|---|---|---|---|
| | | | | | Min | Max | |
| Delay time, RAS high to CAS low | $t_{RPC}$ | See figures 4 and 5 1/ | 9,10,11 | All | 0 | | ns |
| Delay time, RAS low to W low (Read-write operation only) | $t_{RWD}$ | | 9,10,11 | 01 | 120 | | ns |
| | | | | 02 | 100 | | |
| | | | | 03 | 80 | | |
| CAS to output in low Z | $t_{CLZ}$ | | 9,10,11 | All | | See 11/ | ns |
| Refresh time interval | $t_{REF}$ | | 9,10,11 | All | | 16 | ms |

1/ Transition times (rise and fall) for RAS and CAS are to be a minimum of 3 ns and a maximum of 50 ns.

2/ $t_{OFF}$ is specified when the output is no longer driven. The output is disabled when CAS is brought high.
3/ All cycle times assume $t_T$ = 5 ns.
4/ To assure $t_{PC}$ minimum, $t_{ASC}$ should be greater than or equal to $t_{CP}$.
5/ In a read-write cycle, $t_{RWD}$ and $t_{RWL}$ must be observed.
6/ In a read-write cycle, $t_{CWD}$ and $t_{CWL}$ must be observed.

7/ Referenced to the later of CAS or W in write operations.
8/ The minimum value is measured when $t_{RCD}$ is set to $t_{RCD}$ minimum as a reference.
9/ Either $t_{RRH}$ or $t_{RCH}$ must be satisfied for a read cycle.
10/ Maximum value specified only to guarantee access time.
11/ Valid data is presented at the output after all access times are satisfied but may go from three-state to an invalid data state prior to the specified access times as the outputs are driven when CAS goes low.

TABLE IB. Single event phenomena (SEP) test limits. 1/ 2/

| Device type | Temperature (±10°C) | Memory pattern | $V_{CC}$ = 4.5 V Effective threshold LET no upsets, (Mev/(mg/cm$^2$) | $V_{CC}$ = 4.5 V Maximum device cross section ($\mu m^2$) | Bias for latchup test $V_{CC}$ = 5.5 V (minimum) no latchup LET = 100 3/ |
|---|---|---|---|---|---|
| | | | | | |

1/ This blank table will be filled in when a qualified vendor exists.
2/ For SEP test conditions, see 4.4.5 herein.
3/ Worst case temperature $T_A$ = +125°C

TABLE IIA. Electrical test requirements. 1/ 2/ 3/ 4/ 5/ 6/

| Line no. | Test requirements | Subgroups (per method 5005 table I) | | | Subgroups (per MIL-I-38535, table III) | |
|---|---|---|---|---|---|---|
| | | Device class M | Device class B | Device class S | Device class Q | Device class V |
| 1 | Interim electrical parameters (see 4.2) | | 1,7,9 or 2,8A,10 | 1,7,9 or 1,2,8A,10 | 1,7,9 or 2,8A,10 | 1,7,9 or 1,2,8A,10 |
| 2 | Static burn-in I and II method 1015 | Not required | Not required | Required | Not required | Required |
| 3 | Same as line 1 | | | 1*,7* Δ | | 1*,7* Δ |
| 4 | Dynamic burn-in (method 1015) | Required | Required | Required | Required | Required |
| 5 | Same as line 1 | | | 1*,7* Δ | | 1*,7* Δ |
| 6 | Final electrical parameters | 1*,2,3,7*, 8A,8B,9,10, 11 | 1*,2,3,7*, 8A,8B,9,10, 11 | 1*,2,3,7*, 8A,8B,9, 10,11 | 1*,2,3,7*, 8A,8B,9,10, 11 | 1*,2,3,7*, 8A,8B,9, 10,11 |
| 7 | Group A test requirements | 1,2,3,4**,5, 6,7,8A, 8B,9,10,11 | 1,2,3,4**,5, 6,7,8A, 8B,9,10,11 | 1,2,3,4**,5, 6,7,8A, 8B,9,10,11 | 1,2,3,4**,5, 6,7,8A, 8B,9,10,11 | 1,2,3,4**,5, 6,7,8A, 8B,9,10,11 |
| 8 | Group B end-point electrical parameters | | | 1,2,3,7, 8A,8B,9, 10,11 Δ | | 1,2,3,7, 8A,8B,9, 10,11 Δ |
| 9 | Group C end-point electrical parameters | 2,3,7, 8A,8B | 1,2,3,7, 8A,8B Δ | | 1,2,3,7, 8A,8B Δ | |
| 10 | Group D end-point electrical parameters | 2,3, 8A,8B | 2,3, 8A,8B | 2,3, 8A,8B | 2,3, 8A,8B | 2,3, 8A,8B |
| 11 | Group E end-point electrical parameters | 1, 7, 9 | 1, 7, 9 | 1, 7, 9 | 1, 7, 9 | 1, 7, 9 |

1/ Blank spaces indicate tests are not applicable.
2/ Any or all subgroups may be combined when using high-speed testers.
3/ Subgroups 7 and 8 functional tests shall verify the truth table.
4/ * indicates PDA applies to subgroup 1 and 7.
5/ ** see 4.4.1e.
6/ Δindicates delta limit (see table IIC) shall be required where specified, and the delta values shall be computed with reference to the previous electrical parameters (see table IIC).

TABLE IIB. Additional screening for device class V.

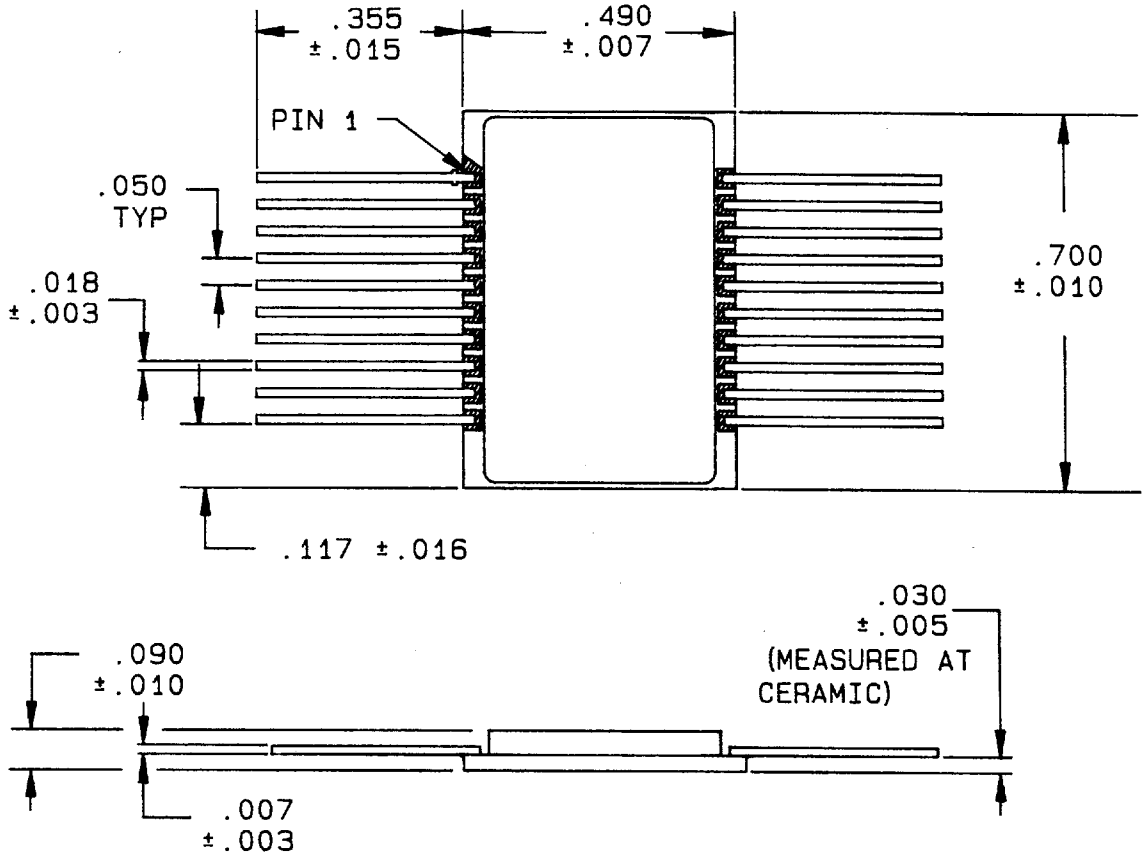
| Test | MIL-STD-883, test method | Lot requirement |
|---|---|---|
| Particle impact noise detection | 2020 | 100% |
| Internal visual | 2010, condition A or approved alternate | 100% |
| Nondestructive bond pull | 2023 or approved alternate | 100% |
| Reverse bias burn-in | 1015 | 100% |
| Burn-in | 1015, total of 240 hours at +125°C | 100% |
| Radiographic | 2012 | 100% |

TABLE IIC. Delta limits at +25°C.

| Parameter 1/ | Device types |
|---|---|
| | All |
| $I_{CC2}$ standby | ±10% of specified value in table IA |
| $I_I$, $I_O$ | ±10% of specified value in table IA |

1/ The above parameter shall be recorded before and after the required burn-in and life tests to determine the delta Δ

Case X

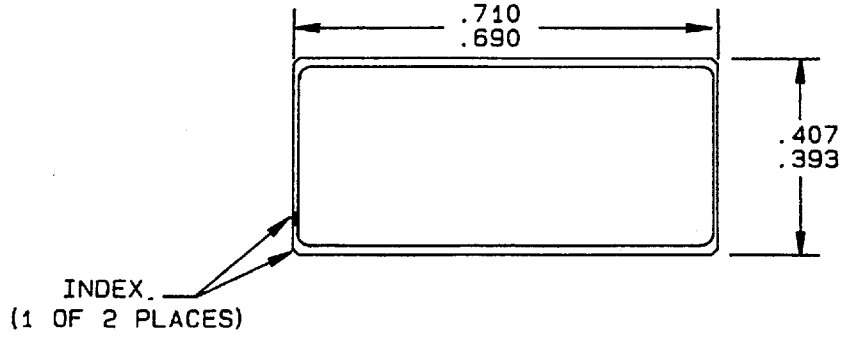


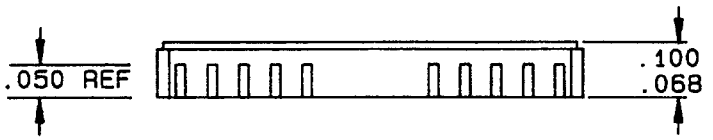

| Inches | mm | Inches | mm |
|---|---|---|---|
| .003 | 0.08 | .030 | 0.76 |
| .005 | 0.13 | .050 | 1.27 |
| .007 | 0.18 | .090 | 2.29 |
| .010 | 0.25 | .117 | 2.97 |
| .015 | 0.38 | .355 | 9.02 |
| .016 | 0.41 | .490 | 12.45 |
| .018 | 0.46 | .700 | 17.78 |

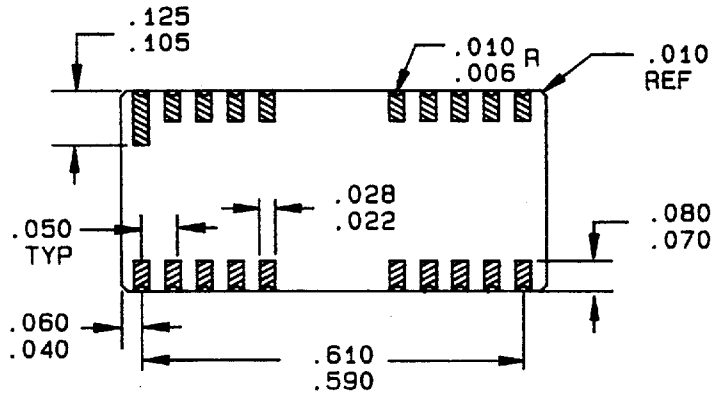
20 Pin flat pack

FIGURE 1. Case outlines.

Case Y



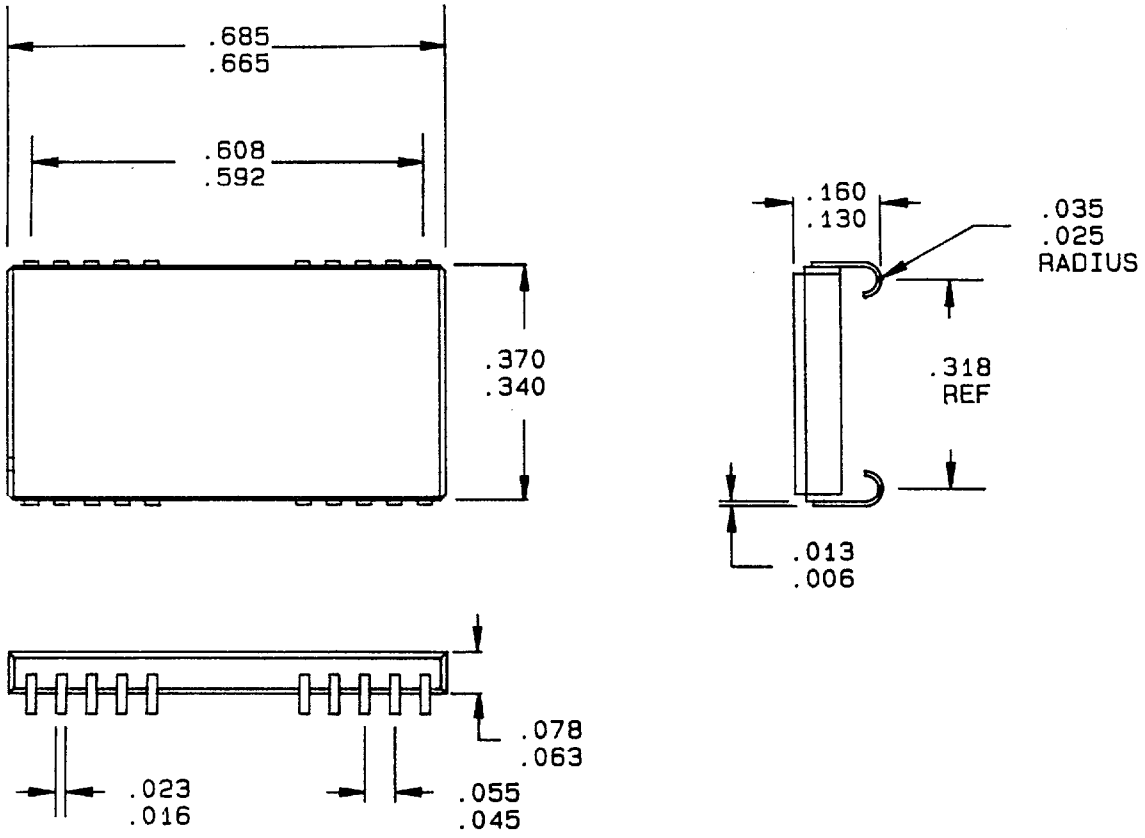




| Inches | mm | Inches | mm |
|---|---|---|---|
| .006 | 0.15 | .080 | 2.03 |
| .010 | 0.25 | .100 | 2.54 |
| .022 | 0.56 | .105 | 2.68 |
| .028 | 0.71 | .125 | 3.18 |
| .040 | 1.02 | .393 | 9.98 |
| .050 | 1.27 | .407 | 10.34 |
| .060 | 1.52 | .590 | 14.98 |
| .068 | 1.72 | .610 | 15.49 |
| .070 | 1.78 | .690 | 17.52 |
| | | .710 | 18.03 |

20-Pin, small-outline leadless ceramic chip carrier

FIGURE 1. Case outlines - Continued.

Case Z

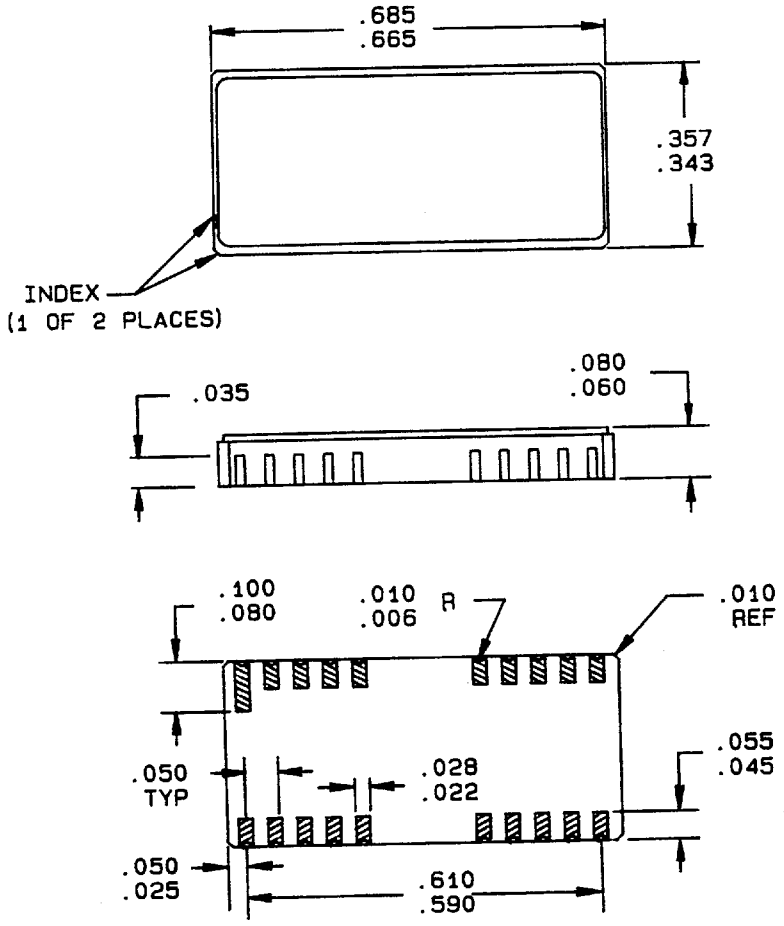



| Inches | mm | Inches | mm |
|---|---|---|---|
| .006 | 0.15 | .130 | 3.30 |
| .013 | 0.33 | .160 | 4.06 |
| .016 | 0.41 | .318 | 8.08 |
| .023 | 0.58 | .340 | 8.64 |
| .025 | 0.63 | .370 | 9.40 |
| .035 | 0.89 | .592 | 15.04 |
| .045 | 1.14 | .608 | 15.44 |
| .055 | 1.40 | .665 | 16.89 |
| .063 | 1.60 | .685 | 17.40 |
| .078 | 1.98 | | |

20/26 Pin, ceramic small-outline, j-leaded chip carrier, 350 mil

FIGURE 1. Case outlines - Continued.

Case U

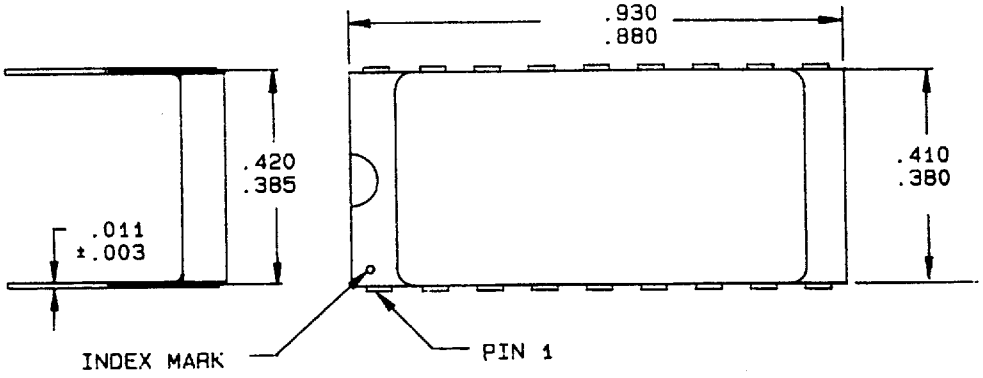


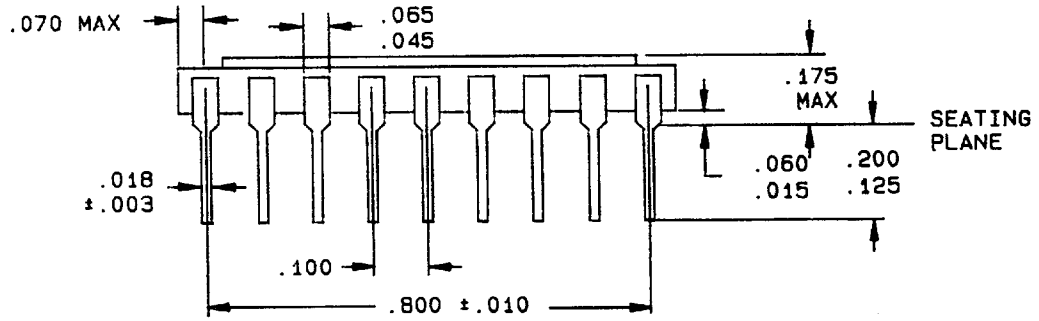

| Inches | mm | Inches | mm |
|---|---|---|---|
| .006 | 0.15 | .080 | 2.03 |
| .010 | 0.25 | .100 | 2.54 |
| .022 | 0.56 | .343 | 8.71 |
| .025 | 0.64 | .357 | 9.06 |
| .028 | 0.71 | .590 | 14.98 |
| .035 | 0.89 | .610 | 15.49 |
| .045 | 1.14 | .665 | 16.89 |
| .050 | 1.27 | .685 | 17.40 |
| .055 | 1.40 | | |
| .060 | 1.52 | | |

20-Pin, (350 mil) small-outline, leadless ceramic chip carrier

FIGURE 1. Case outlines - Continued.

Case T



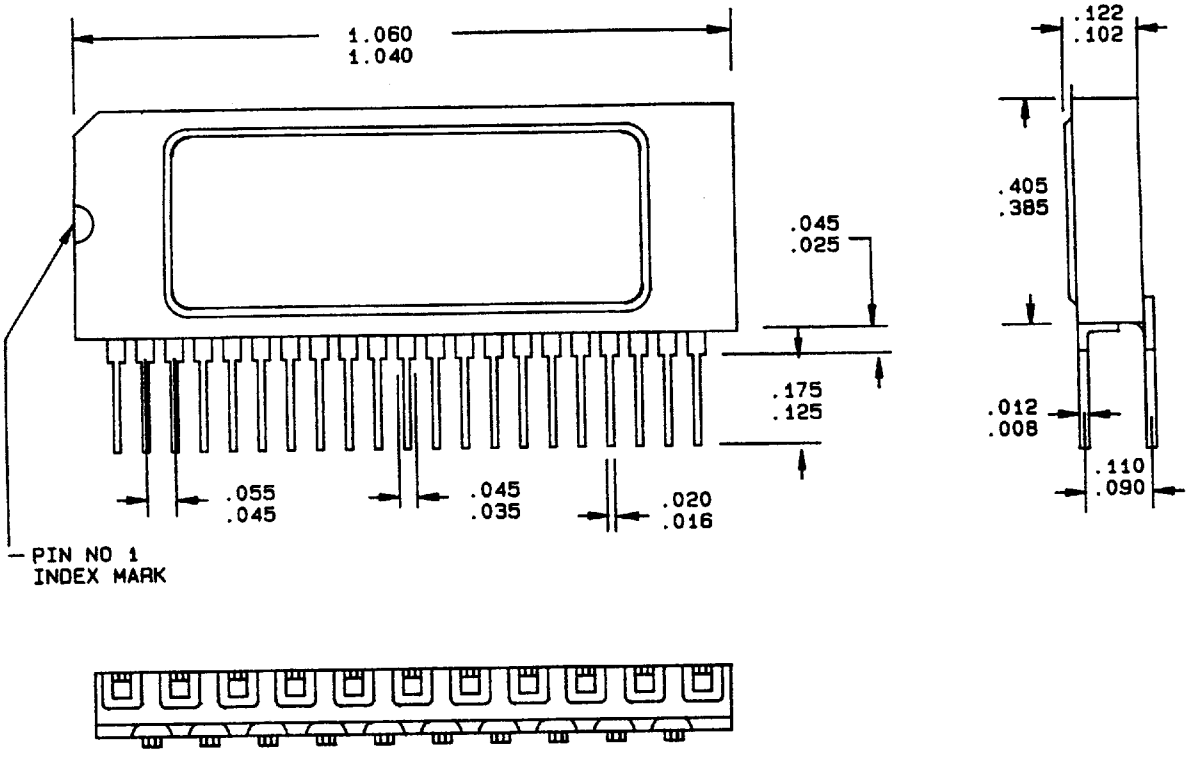




| Inches | mm | Inches | mm |
|---|---|---|---|
| .003 | 0.08 | .125 | 3.18 |
| .010 | 0.25 | .175 | 4.44 |
| .011 | 0.28 | .200 | 5.08 |
| .015 | 0.38 | .380 | 9.65 |
| .018 | 0.46 | .385 | 9.78 |
| .045 | 1.14 | .410 | 10.41 |
| .060 | 1.52 | .420 | 10.68 |
| .065 | 1.65 | .800 | 20.32 |
| .070 | 1.78 | .880 | 22.35 |
| .100. | 2.54 | .930 | 23.62 |

18-Pin, ceramic side brazed, dual-in-line package

FIGURE 1. Case outlines - Continued.

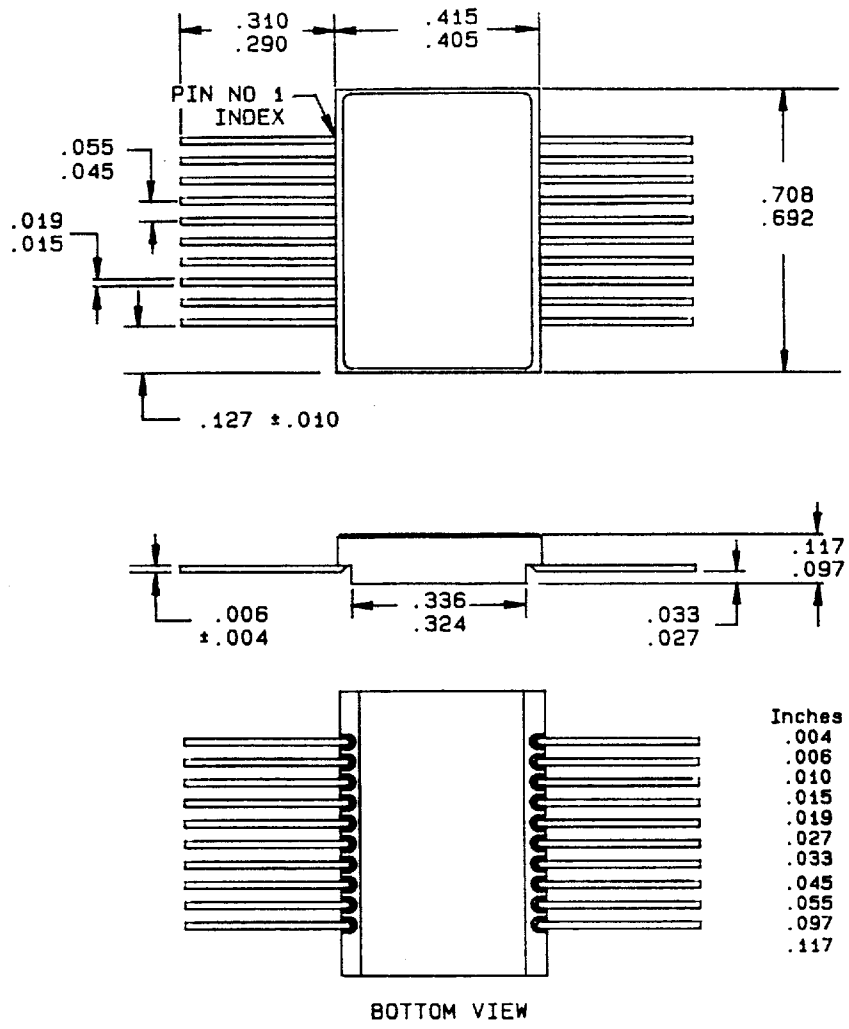
Case N




| Inches | mm | Inches | mm |
|---|---|---|---|
| .008 | 0.20 | .102 | 2.59 |
| .012 | 0.30 | .110 | 2.79 |
| .016 | 0.41 | .122 | 3.10 |
| .025 | 0.64 | .125 | 3.18 |
| .020 | 0.51 | .175 | 4.45 |
| .035 | 0.89 | .385 | 9.78 |
| .045 | 1.14 | .405 | 10.29 |
| .055 | 1.40 | 1.040 | 26.42 |
| .090 | 2.29 | 1.060 | 26.92 |

FIGURE 1. Case outlines - Continued.

Case M




| Inches | mm | Inches | mm |
|---|---|---|---|
| .004 | 0.10 | .127 | 3.23 |
| .006 | 0.15 | .290 | 7.37 |
| .010 | 0.25 | .310 | 7.87 |
| .015 | 0.38 | .324 | 8.23 |
| .019 | 0.48 | .336 | 8.53 |
| .027 | 0.69 | .405 | 10.29 |
| .033 | 0.84 | .415 | 10.54 |
| .045 | 1.14 | .435 | 11.05 |
| .055 | 1.40 | .455 | 11.56 |
| .097 | 2.46 | .692 | 17.58 |
| .117 | 2.97 | .708 | 17.98 |

20 Pin flat pack.

FIGURE 1. Case outlines - Continued.

| Device types | 01, 02, 03 | | | |
|---|---|---|---|---|
| Case outlines | T, V | X, M | Y, U, Z | N |
| Terminal number | Terminal symbol | | | |
| 1 | $\overline{D}$ | $\overline{D}$ | $\overline{D}$ | $A_9$ |
| 2 | $\overline{W}$ | $\overline{W}$ | $\overline{W}$ | $\overline{CAS}$ |
| 3 | $\overline{RAS}$ | $\overline{RAS}$ | $\overline{RAS}$ | Q |
| 4 | $A_{10}$ | NC | NC | $V_{SS}$ |
| 5 | $A_0$ | $A_{10}$ | $A_{10}$ | $\overline{D}$ |
| 6 | $A_1$ | $A_0$ | -- | $\overline{W}$ |
| 7 | $A_2$ | $A_1$ | -- | $\overline{RAS}$ |
| 8 | $A_3$ | $A_2$ | -- | $A_{10}$ |
| 9 | $V_{CC}$ | $A_3$ | $A_0$ | NC |
| 10 | $A_4$ | $V_{CC}$ | $A_1$ | NC |
| 11 | $A_5$ | $A_4$ | $A_2$ | $A_0$ |
| 12 | $A_6$ | $A_5$ | $A_3$ | $A_1$ |
| 13 | $A_7$ | $A_6$ | $V_{CC}$ | $A_2$ |
| 14 | $A_8$ | $A_7$ | $A_4$ | $A_3$ |
| 15 | $A_9$ | $A_8$ | $A_5$ | $V_{CC}$ |
| 16 | $\overline{CAS}$ | $A_9$ | $A_6$ | $A_4$ |
| 17 | Q | $\overline{NC}$ | $A_7$ | $A_5$ |
| 18 | $V_{SS}$ | $\overline{CAS}$ | $A_8$ | $A_6$ |
| 19 | -- | Q | -- | $A_7$ |
| 20 | -- | $V_{SS}$ | -- | $A_8$ |
| 21 | -- | -- | -- | -- |
| 22 | -- | -- | $A_9$ | -- |
| 23 | -- | -- | $\overline{NC}$ | -- |
| 24 | -- | -- | $\overline{CAS}$ | -- |
| 25 | -- | -- | Q | -- |
| 26 | -- | -- | $V_{SS}$ | -- |

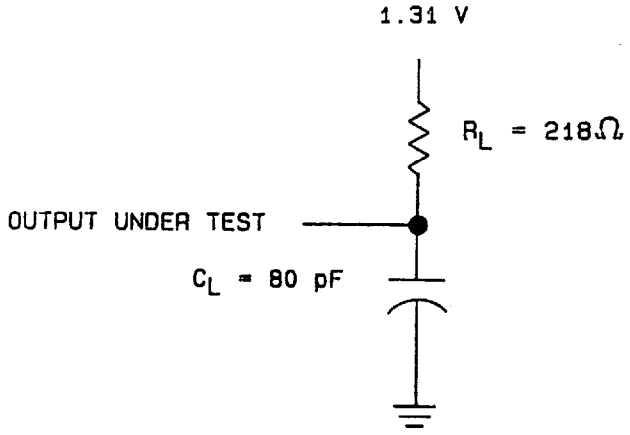
FIGURE 2. Terminal connections.

| Operation | Inputs | | | | | Input | Output |
|---|---|---|---|---|---|---|---|
| | $\overline{RAS}$ | $\overline{CAS}$ | $\overline{W}$ | Row address | Column address | D | Q |
| Read | ACT | ACT | NAC | APD | APD | DNC | VLD |
| Write (early write) | ACT | ACT | ACT | APD | APD | VLD | OPN |
| Write (late write) | ACT | ACT | ACT | APD | APD | VLD | IVD 1/ |
| Read-modify-write | ACT | ACT | ACT | APD | APD | VLD | VLD |
| $\overline{RAS}$-only refresh | ACT | NAC | DNC | APD 2/ | DNC | DNC | OPN |
| Hidden refresh | ACT | ACT | NAC | APD | DNC | DNC | VLD |
| $\overline{CAS}$ before $\overline{RAS}$ refresh | ACT | ACT | NAC | DNC | DNC | DNC | OPN |
| Standby | NAC | NAC | DNC | DNC | DNC | DNC | OPN |

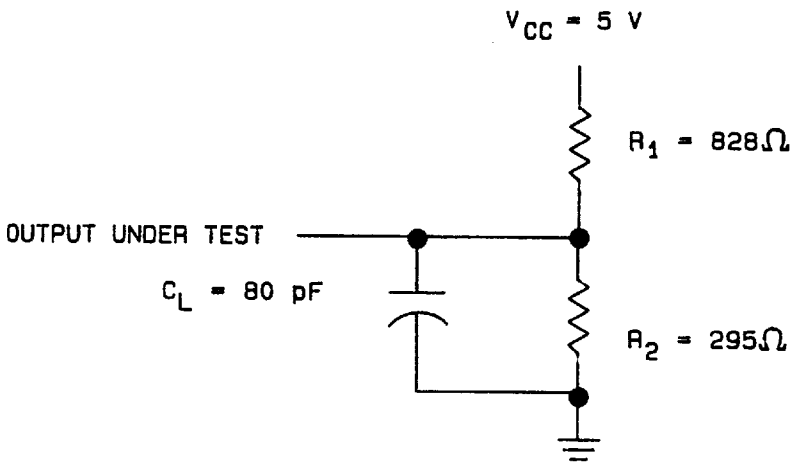
1/Output may go from high impedance to an invalid data state prior to the specified access time as the output is driven when $\overline{CAS}$ goes low.
2/A10 is a don't care.

ACT = active
NAC = nonactive
DNC = don't care
VLD = valid
ILD = invalid
APD = applied
OPN = open

FIGURE 3. Truth table.



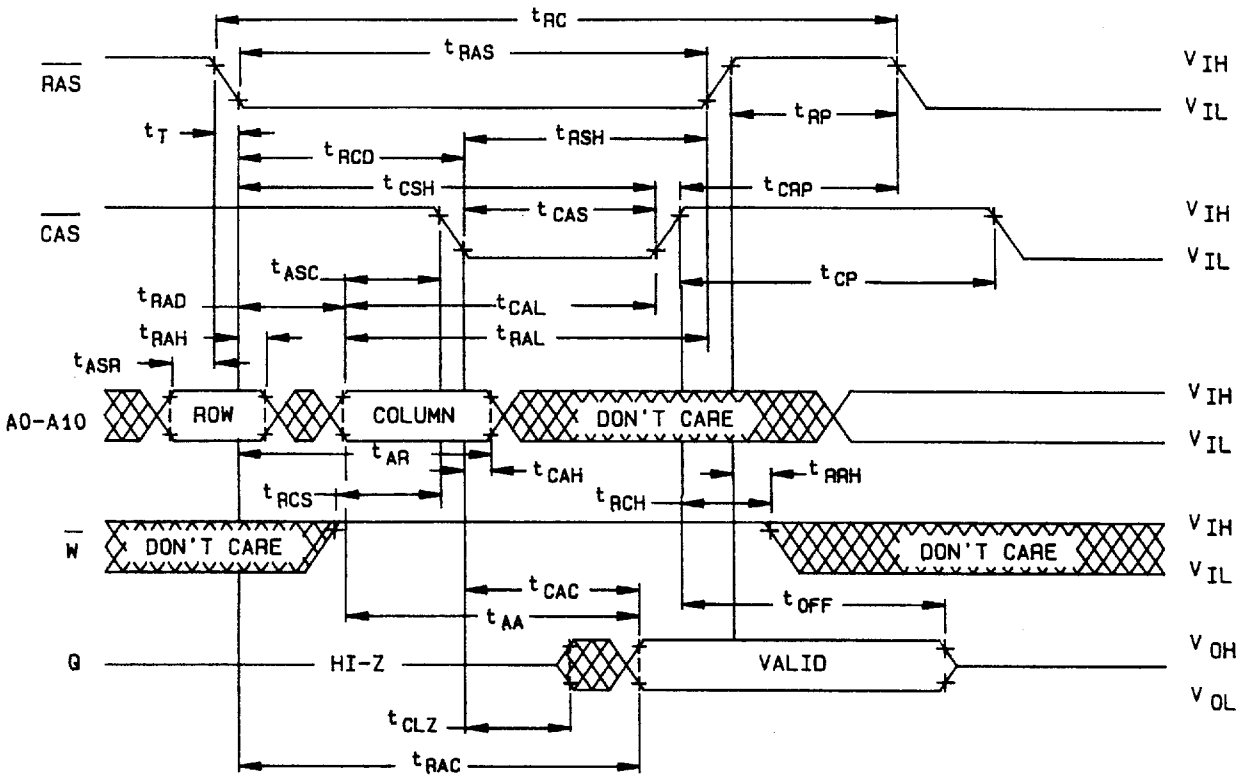

(A) LOAD CIRCUIT




(B) ALTERNATE LOAD CIRCUIT

FIGURE 4. Load circuits.

Read cycle timing




NOTE: Output may go from three-state to an invalid state prior to the specified access time.

FIGURE 5. Timing wavwform diagrams.

Early write cycle timing

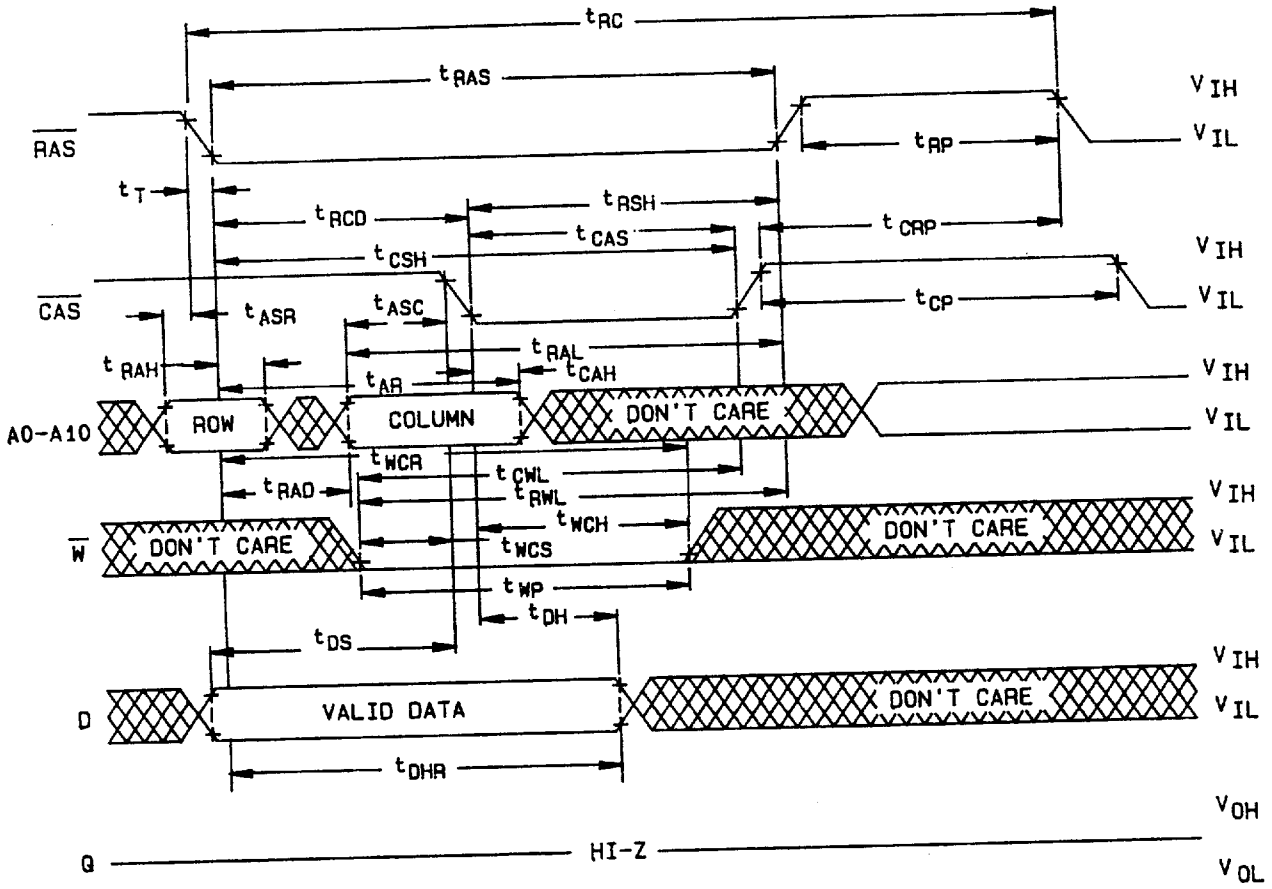



FIGURE 5. Timing wave diagrams - Continued.

Write cycle timing

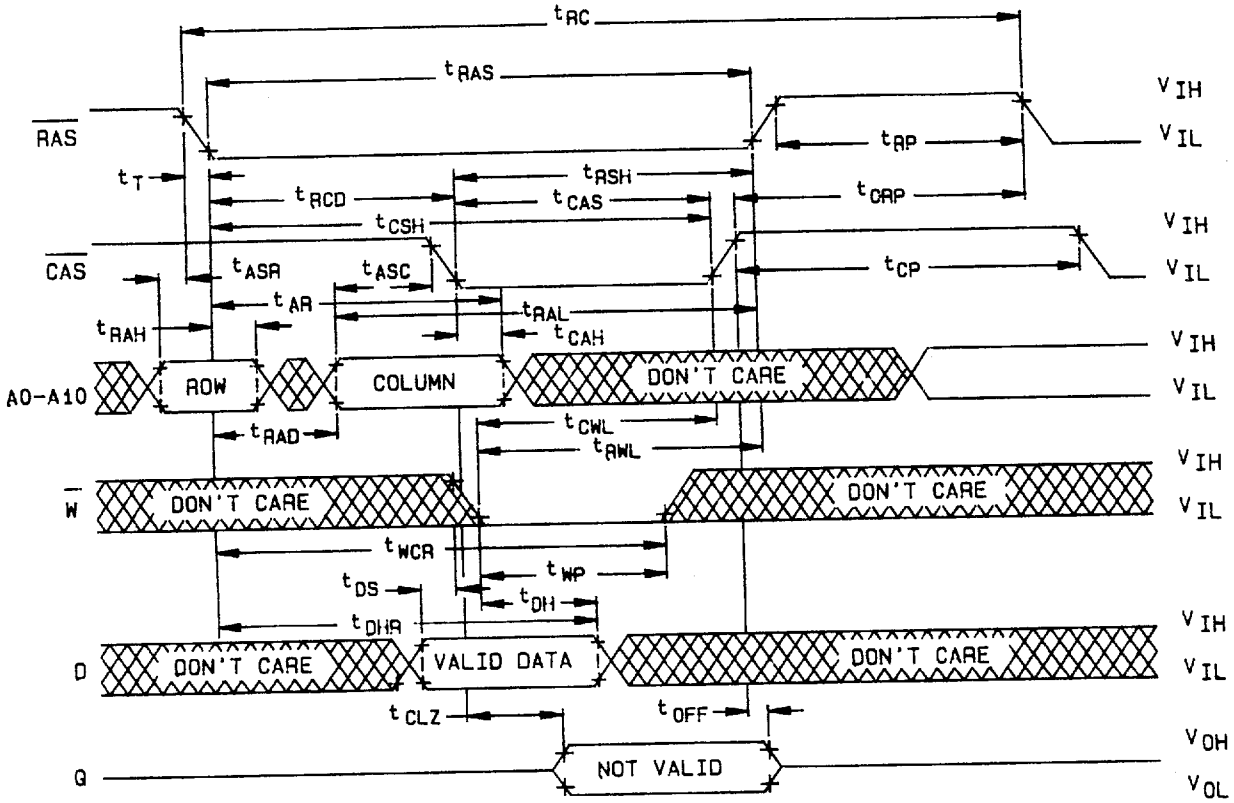
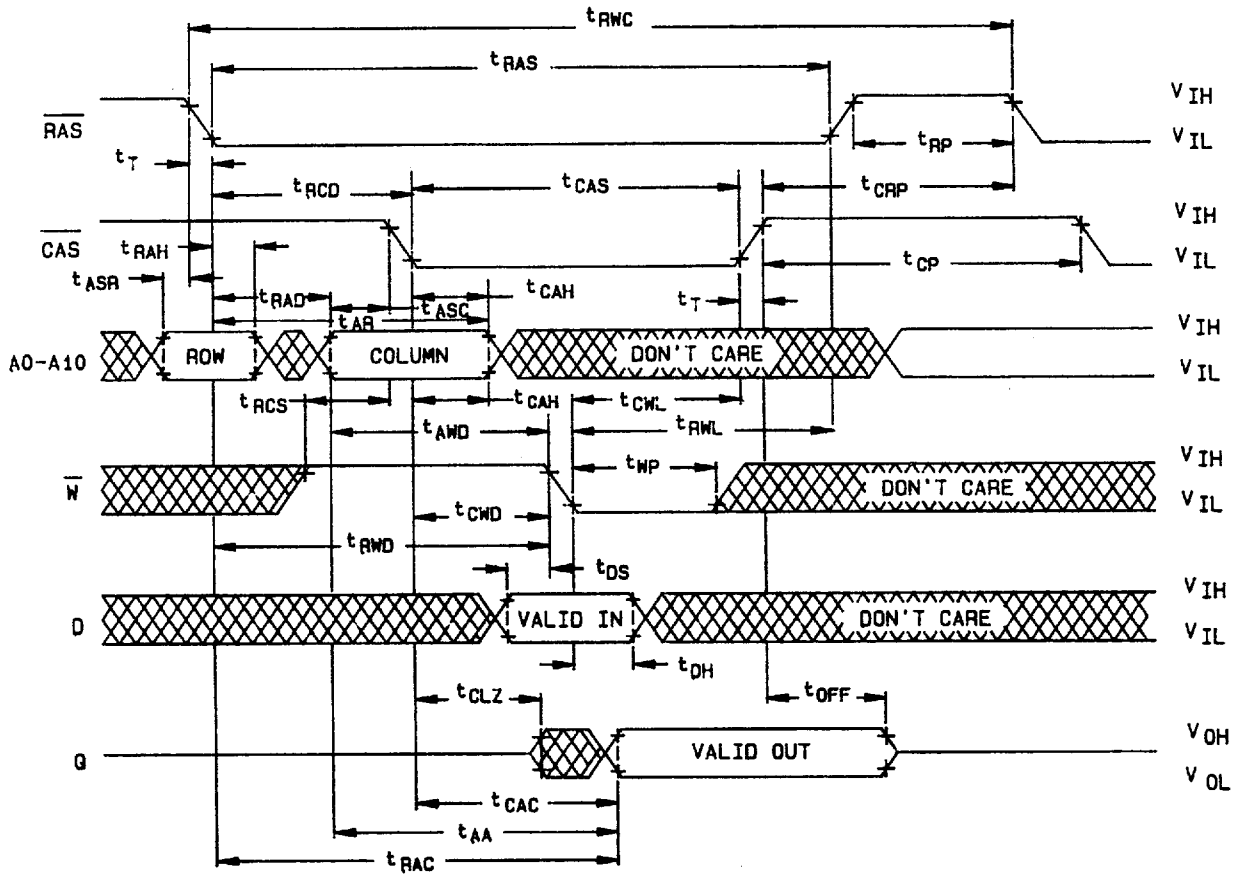



FIGURE 5. Timing wave diagrams - Continued.

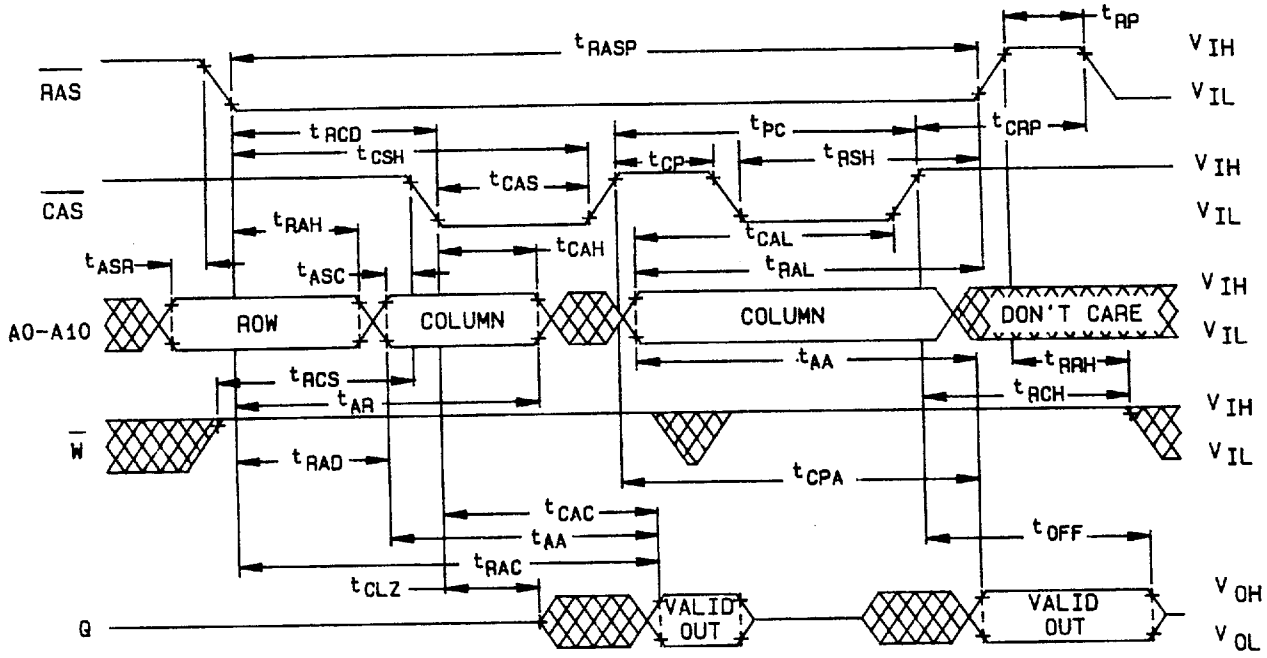
Read-write cycle timing




NOTE: Output may go from three-state to an invalid state prior to the specified access time.

FIGURE 5. Timing wave diagrams - Continued.

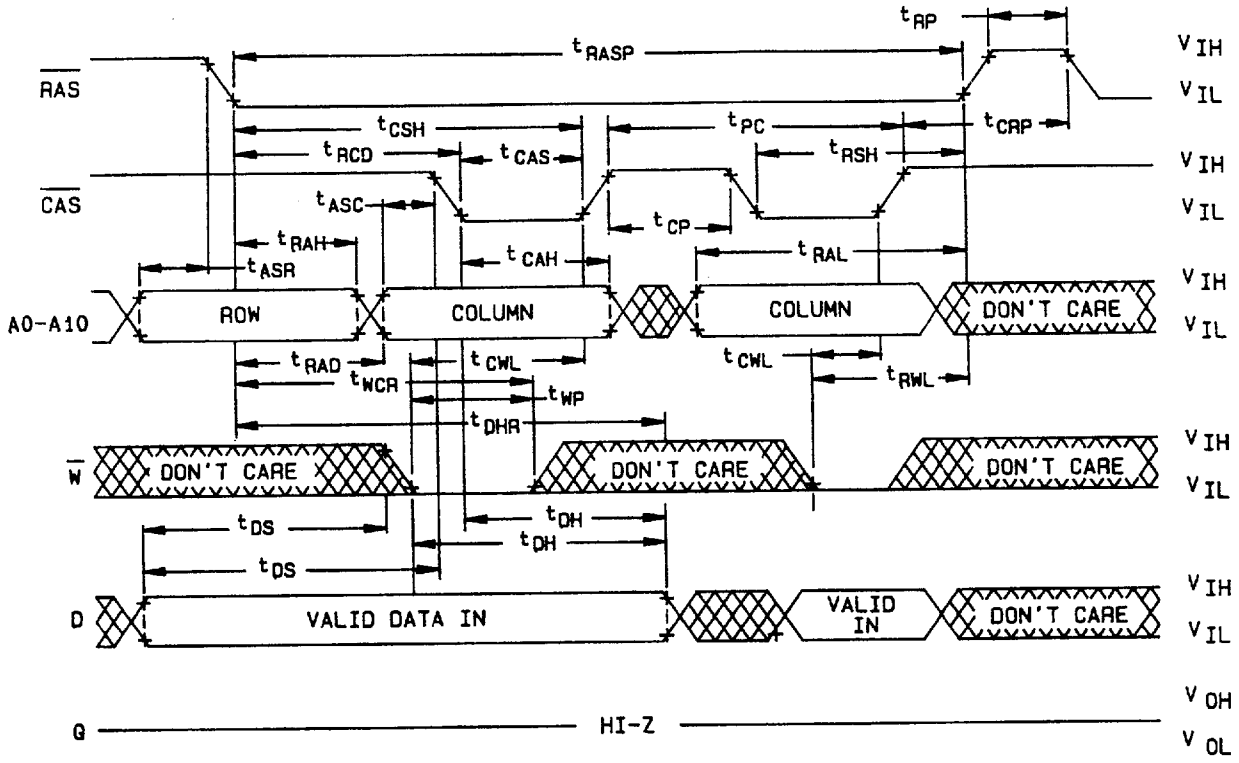
Enhanced page-mode read cycle timing




NOTES:
1. Output may go from three-state to an invalid state prior to the specified access time.
2. Access time is $t_{CPA}$ or $t_{AA}$ dependent.

FIGURE 5. Timing wave diagrams - Continued.

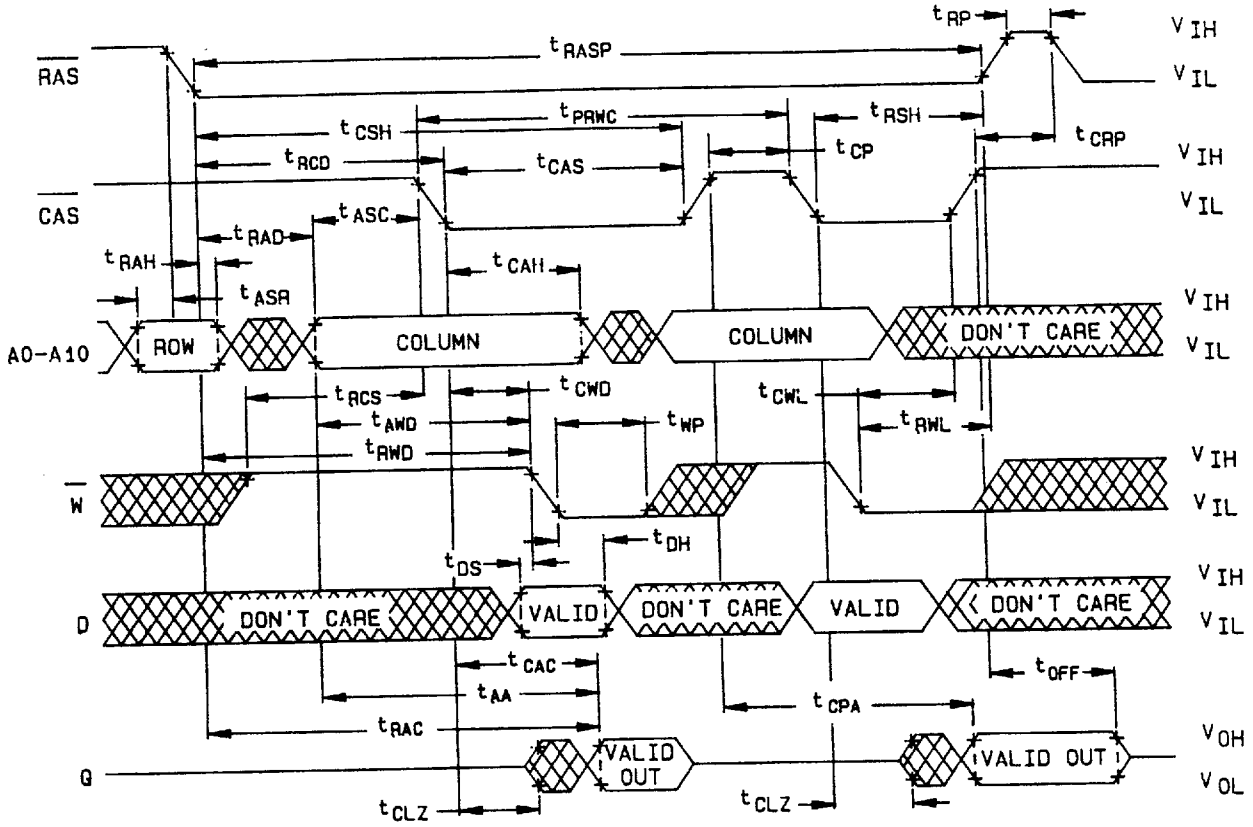
Enhanced page-mode write cycle timing




NOTES:
1. $t_{DS}$ and $t_{DH}$ are referenced to $\overline{CAS}$ or $\overline{W}$, whichever occurs last.
2. A read cycle or a read-write cycle can be intermixed with write write cycle as long as the read and read-write timing specification are not violated.

FIGURE 5. Timing wave diagrams - Continued.

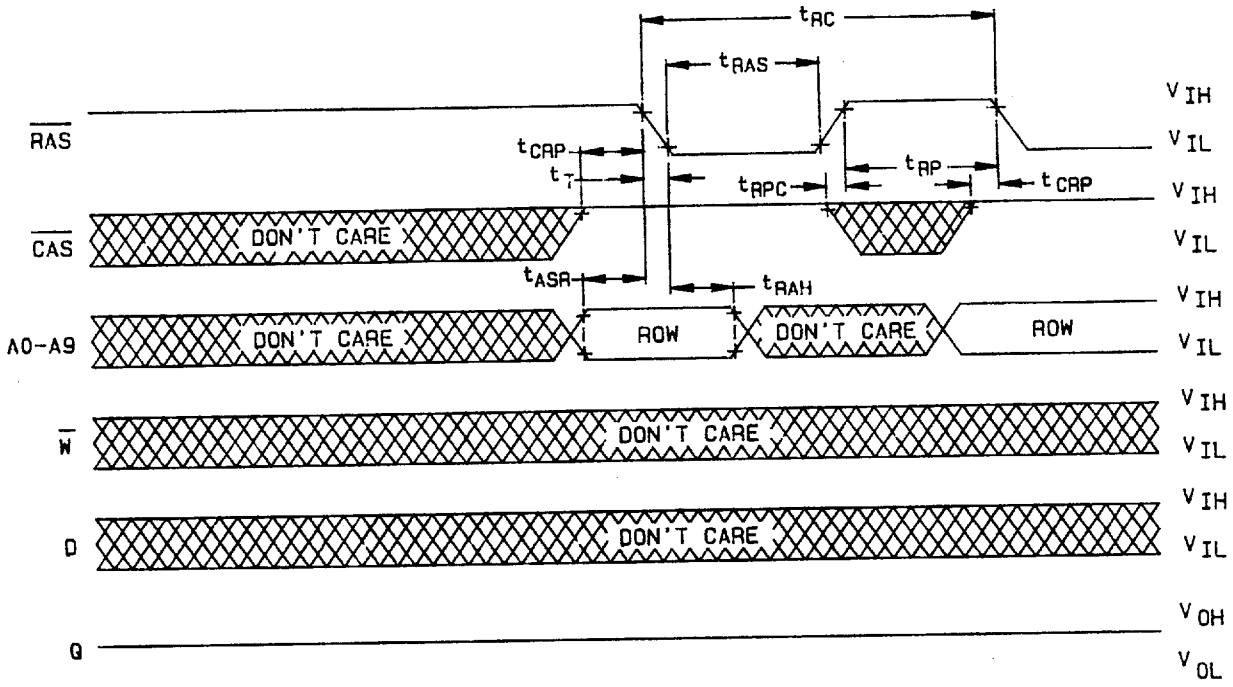
Enhanced page-mode read-write cycle timing




NOTES:
1. Output may go from three-state to an invalid state prior to the specified access time.
2. A read or read-write cycle can be intermixed with read-write cycles as long as the read and write timing specification are not violated.

FIGURE 5. Timing wave diagrams - Continued.

$\overline{RAS}$-only refresh timing




NOTE: A10 is a don't care.

FIGURE 5. Timing wave diagrams - Continued.

| STANDARDIZED MILITARY DRAWING DEFENSE ELECTRONICS SUPPLY CENTER DAYTON, OHIO 45444 | SIZE A | | 5962-90622 |
|---|---|---|---|
| | | REVISION LEVEL | SHEET 34 |

Automatic ($\overline{CAS}$-before-$\overline{RAS}$)
refresh cycle timing

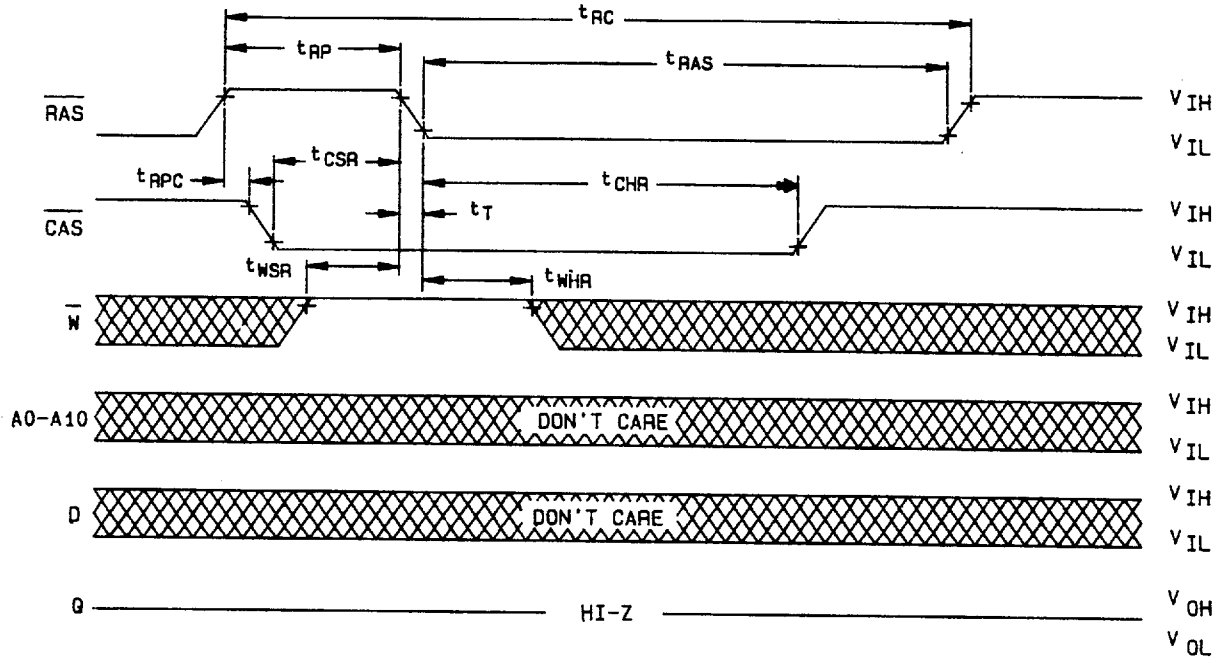



FIGURE 5. Timing wave diagrams - Continued.

Hidden refresh cycle (read)

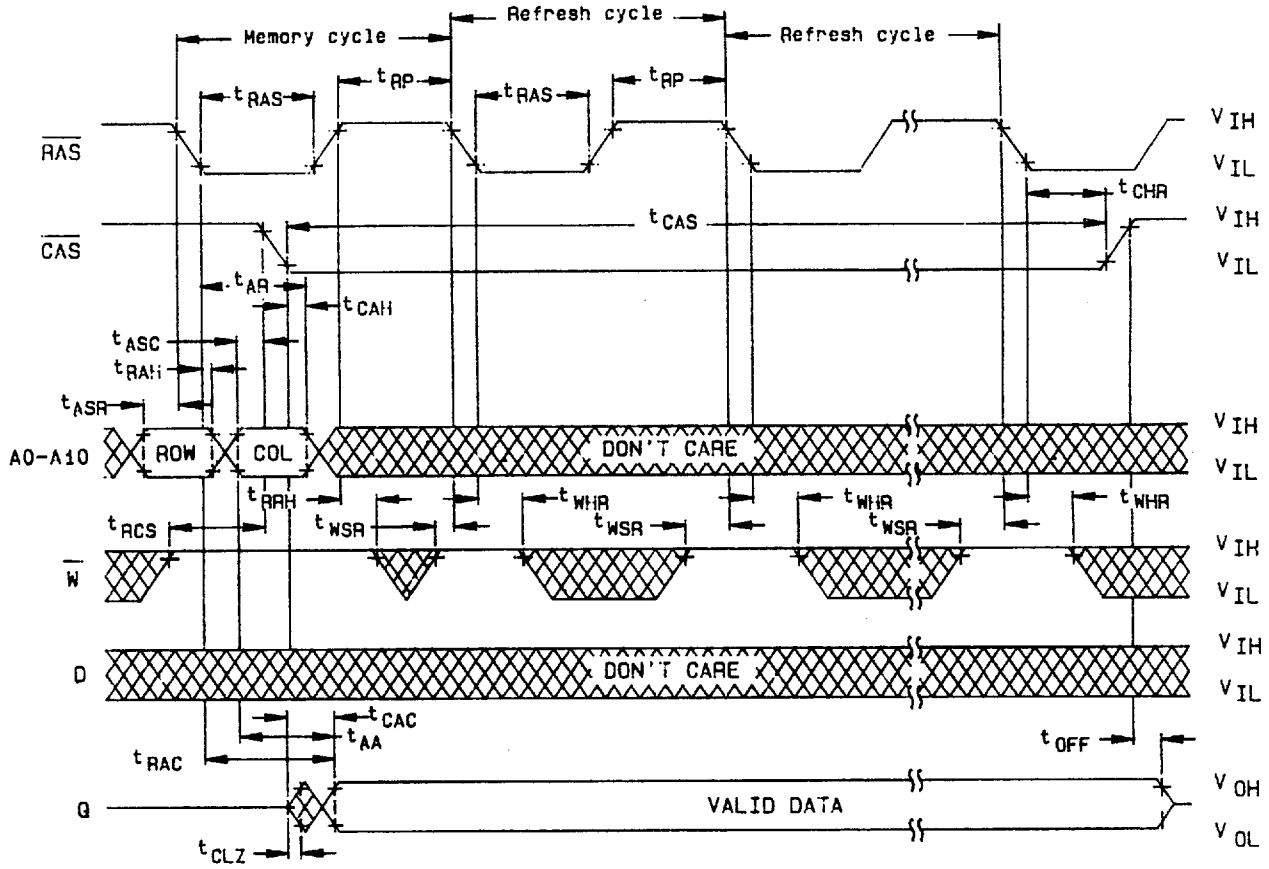



FIGURE 5. Timing wave diagrams - Continued.

Hidden refresh cycle (write)

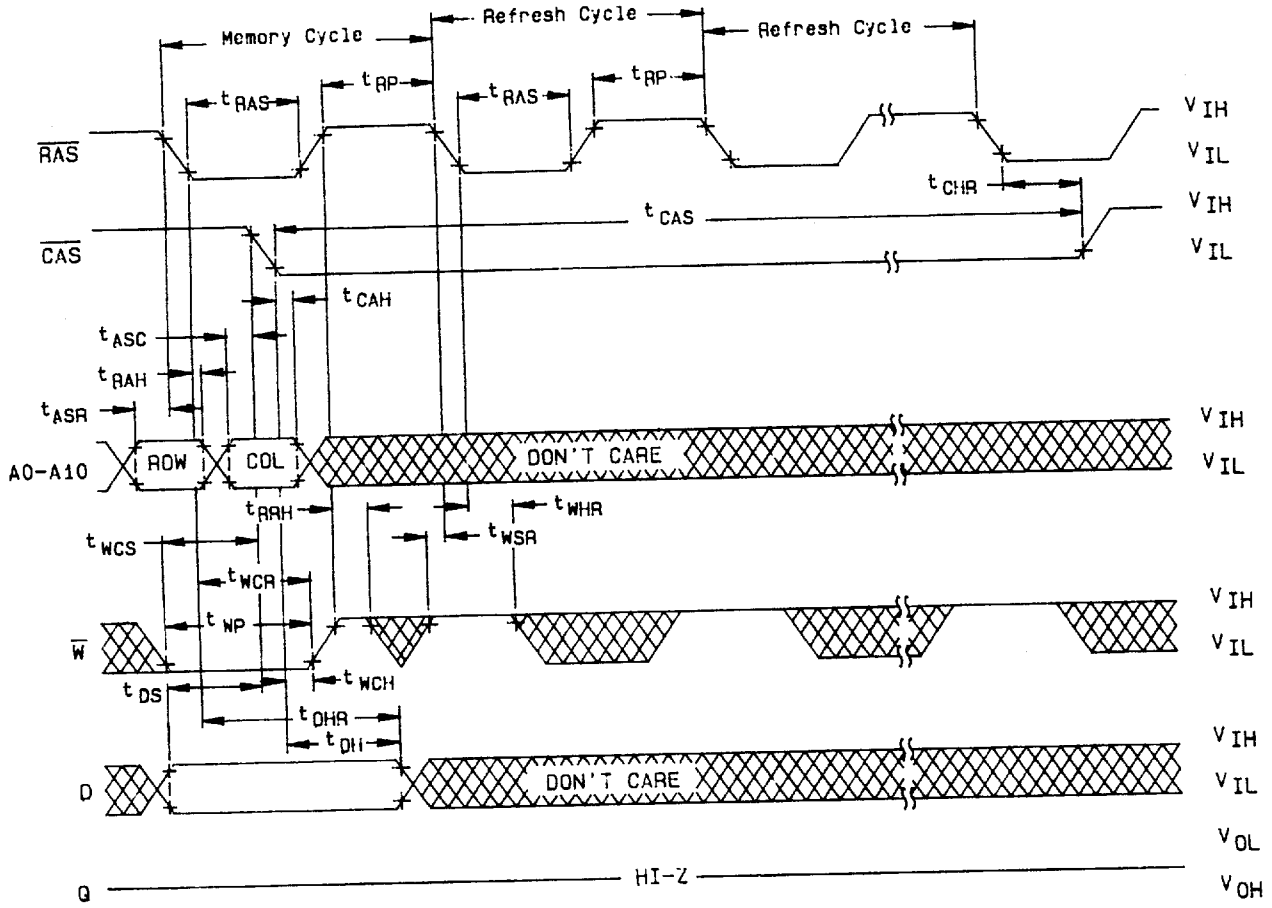



FIGURE 5. Timing wave diagrams - Continued.

| | | | |
|---|---|---|---|
| STANDARDIZED MILITARY DRAWING DEFENSE ELECTRONICS SUPPLY CENTER DAYTON, OHIO 45444 | SIZE A | | 5962-90622 |
| | | REVISION LEVEL | SHEET 37 |

NOTE: When a qualified source exists, a circuit shall be provided and placed on this page.

FIGURE 6. Radiation hardness bias circuit.

4.4.1 Group A inspection.

a. Tests shall be as specified in table IIA herein.

b. Subgroups 5 and 6 of table I of method 5005 of MIL-STD-883 shall be omitted.

c. For device class M subgroups 7 and 8 tests shall be sufficient to verify the truth table. For device classes B and S subgroups 7 and 8 tests shall be sufficient to verify the truth table as approved by the qualifying activity. For device classes Q and V subgroups 7 and 8 shall include verifying the functionality of the device; these tests shall have been fault graded in accordance with MIL-STD-883, test method 5012 (see 1.5 herein).

d. O/V (latch-up) tests shall be measured only for initial qualification and after any design or process changes which may affect the performance of the device. Procedures and circuits shall be submitted to DESC-ECS for class M devices. For classes B and S, the procedures and circuits shall be submitted to the qualifying activity. For classes Q and V, the procedures and circuits shall be submitted to DESC-ECS and will be under the control of the device manufacturer's technical review board (TRB). Testing shall be on all pins, on 5 devices with zero failures. Latch-up test shall be considered destructive.

e. Subgroup 4 ($C_{IN}$ and $C_{OUT}$ measurements) shall be measured only for initial qualification and after any process or design changes which may affect input or output capacitance. Capacitance shall be measured between the designated terminal and GND at a frequency of 1 MHz. Sample size is 15 devices with no failures, and all input and output terminals tested.

4.4.2 Group B inspection. The group B inspection end-point electrical parameters shall be as specified in table IIA herein.

a. For device class S, steady-state life test circuits shall be conducted using test condition D and the circuit described in 4.2b herein, or equivalent as approved by the qualifying activity.

b. For device class S only, end-point electrical parameters shall be as specified in table IIA herein. Delta limits shall apply only to subgroup 5 of group B inspections and shall consist of tests specified in table IIC herein.

4.4.3 Group C inspection. The group C inspection end-point electrical parameters shall be as specified in table IIA herein. Delta limits shall apply only to subgroup 1 of group C inspection and shall consist of tests specified in table IIC herein.

4.4.3.1 Additional criteria for device classes M, B, and S. Steady-state life test conditions, method 1005 of MIL-STD-883:

a. Test condition D. For device class M, the test circuit shall be submitted to DESC-ECS for review with the certificate of compliance. For device classes B and S, the test circuit shall be submitted to the qualifying activity.

b. $T_A$ = +125°C, minimum.

c. Test duration: 1,000 hours, except as permitted by method 1005 of MIL-STD-883.

4.4.3.2 Additional criteria for device classes Q and V. The steady-state life test duration, test condition and test temperature or approved alternatives shall be as specified in the device manufacturer's QM plan in accordance with MIL-I-38535. The steady-state life test circuit shall be submitted to DESC-ECS with the certificate of compliance and shall be under the control of the device manufacturer's TRB in accordance with MIL-I-38535.

4.4.4 Group D inspection. The group D inspection end-point electrical parameters shall be as specified in table IIA herein.

4.4.5 Group E inspection. Group E inspection is required only for parts intended to be marked as radiation hardness assured (see 3.5 herein). RHA levels for device classes B, S, Q, and V shall be M, D, R, or H and for device class M, shall be M or D. RHA quality conformance inspection sample tests shall be performed at the RHA level specified in the acquisiton document. RHA tests for device classes Q and V shall be performed in accordance with MIL-I-38535 and 1.2.1 herein.

a. RHA tests for device classes B and S for levels M, D, R, and H or for device class M for levels M and D shall be performed through each level to determine at what levels the devices meet the RHA requirements. These RHA tests shall be performed for initial qualification and after design or process changes which may affect the RHA performance of the device.

b. End-point electrical parameters shall be as specified in table IA herein. RHA samples need not be tested at -55°C or +125°C prior to total dose irradiation.

c. Prior to total dose irradiation, each selected sample shall be assembled in its qualified package. The samples shall pass the specified group A electrical parameters for subgroups specified in table IIA herein. Additionally classes Q and V, for quality conformance inspection may be at wafer level.

d. The devices shall be subjected to radiation hardness assurance tests as specified in MIL-M-38510 (device classes M, B, and S) and MIL-I-38535 (device classes Q and V) for the RHA level being tested, and meet the postirradiation end-point electrical parameter limits as defined in table IA at $T_A$ = +25°C ±5°C, after exposure.

e. Prior to and during total dose irradiation, the devices shall be biased to the worst case conditions established during characterization, see figure 6 herein.

f. SEP testing shall be performed on all class S and V devices. SEP testing shall be performed at initial qualification and after any design or process changes which may affect the upset or latchup characteristics of the device. Test four devices with zero failures. ASTM standard F1192-88 may be used as a guideline when performing SEP testing. For device class V, the device parametrics that influence single event upset immunity shall be monitored at the wafer level as part of a TRB approved wafer level hardness plan. The test conditions for SEP are as follows:

(1) The ion beam angle of incidence shall be between normal to the die surface and 60° to the normal, inclusive (i.e., 0° ≤ angle ≤ 60°). No shadowing of the ion beam due to fixturing or package related effects is allowed.

(2) The fluence shall be greater than 100 errors or $\geq 10^7$ ions/cm$^2$.

(3) The flux shall be between $10^2$ and $10^5$ ion/cm$^2$/s. The cross section shall be verified to be flux independent by measuring the cross section at two flux rates which differ by at least an order of magnitude.

(4) The particle range shall be ≥ 20 microns in silicon.

(5) The test temperature shall be +25°C and the maximum rated operating temperature ±10°C.

(6) Bias conditions shall be $V_{CC}$ = 4.5 V dc for the upset measurements and $V_{CC}$ =5.5 V dc for the latchup measurements.

(7) For SEP test limits, see table IB herein.

g. For device classes M, B, and S subgroups 1 and 2 of table V method 5005 of MIL-STD-883 shall be tested as appropriate for device construction.

h. Transient dose rate upset testing for class Q and V devices shall be performed as specified by a TRB approved radiation hardness assurance plan and MIL-I-38535. Device parametric parameters that influence upset immunity shall be monitored at the wafer level in accordance with the wafer level hardness assurance plan and MIL-I-38535.

i. Transient dose rate survivability testing for class Q and V devices shall be performed as specified by a TRB approved radiation hardness assurance plan and MIL-I-38535. Device parametric parameters that influence latch-up and device burn-out shall be monitored at the wafer level in accordance with the wafer level hardness assurance plan and MIL-I-38535.

j. When specified in the purchase order or contract, a copy of the following additional data shall be supplied.

(1) RHA delta limits.

(2) RHA upset levels.

(3) Test conditions (SEP).

(4) Number of upsets (SEP).

(5) Number of transients.

(6) Occurence of latch-up.

4.5 Delta measurements for device classes S and V. Delta measurements, as specified in table IIA, shall be made and recorded before and after the required burn-in screens and steady-state life tests to determine delta compliance. The electrical parameters to be measured, with associated delta limits are listed in table IIC. The device manufacturer may, at his option, either perform delta measurements or within 24 hours after life test perform final electrical parameter tests, subgroups 1, 7, and 9.

## 5. PACKAGING

5.1 Packaging requirements. The requirements for packaging shall be in accordance with MIL-M-38510 for device classes M, B, and S and MIL-I-38535 for device classes Q and V.

## 6. NOTES

(This section contains information of a general or explanatory nature that may be helpful, but is not mandatory.)

6.1 Intended use. Microcircuits conforming to this drawing are intended for use for Government microcircuit applications (original equipment), design applications, and logistics purposes.

6.1.1 Replaceability. Microcircuits covered by this drawing will replace the same generic device covered by a contractor-prepared specification or drawing.

6.1.2 Substitutability. Device classes B or Q devices will replace device class M devices.

6.2 Configuration control of SMD's. All proposed changes to existing SMD's will be coordinated with the users of record for the individual documents. This coordination will be accomplished in accordance with MIL-STD-481 using DD Form 1693, Engineering Change Proposal (Short Form).

6.3 Record of users. Military and industrial users shall inform Defense Electronics Supply Center when a system application requires configuration control and which SMD's are applicable to that system. DESC will maintain a record of users and this list will be used for coordination and distribution of changes to the drawings. Users of drawings covering microelectronic devices (FSC 5962) should contact DESC-ECS, telephone (513) 296-6022.

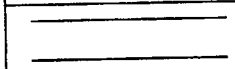
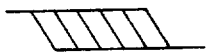
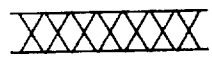
6.4 Comments. Comments on this drawing should be directed to DESC-ECS, Dayton, Ohio 45444, or telephone (513) 296-5375.

6.5 Abbreviations, symbols, and definitions. The abbreviations, symbols, and definitions used herein are defined in MIL-M-38510, MIL-STD-1331, and as follows:

| | |
|---|---|
| $C_{IN}$ $C_{OUT}$ | Input and bidirectional output, terminal-to-GND capacitance. |
| GND | Ground zero voltage potential. |
| $I_{CC}$ | Supply current. |
| $I_{IL}$ | Input current low |
| $I_{IH}$ | Input current high |
| $T_C$ | Case temperature. |
| $T_A$ | Ambient temperature |
| $V_{CC}$ | Positive supply voltage. |
| $V_{IC}$ | Positive input clamp voltage |
| O/V | Latch-up over-voltage |
| O/I | Latch-up over-current |

6.5.1 Timing limits. The table of timing values shows either a minimum or a maximum limit for each parameter. Input requirements are specified from the external system point of view. Thus, address setup time is shown as a minimum since the system must supply at least that much time (even though most devices do not require it). On the other hand, responses from the memory are specified from the device point of view. Thus, the access time is shown as a maximum since the device never provides data later than that time.

6.5.2 Waveforms.

| WAVEFORM SYMBOL | INPUT | OUTPUT |
|---|---|---|
|  | MUST BE VALID | WILL BE VALID |
|  | CHANGE FROM H TO L | WILL CHANGE FROM H TO L |
|  | CHANGE FROM L TO H | WILL CHANGE FROM L TO H |
|  | DON'T CARE ANY CHANGE PERMITTED | CHANGING STATE UNKNOWN |
|  | | HIGH IMPEDANCE |

6.6 One part - one part number system. The one part - one part number system described below has been developed to allow for transitions between identical generic devices covered by the four major microcircuit requirements documents (MIL-M-38510, MIL-H-38534, MIL-I-38535, and 1.2.1 of MIL-STD-883) without the necessity for the generation of unique PIN'S. The four military requirements documents represent different class levels, and previously when a device manufacturer upgraded military product from one class level to another, the benefits of the upgraded product were unavailable to the Original Equipment Manufacturer (OEM), that was contractually locked into the original unique PIN. By establishing a one part number system covering all four documents, the OEM can acquire to the highest class level available for a given generic device to meet system needs without modifying the original contract parts selection criteria.

| Military documentation format | Example PIN under new system | Manufacturing source listing | Document listing |
|---|---|---|---|
| New MIL-M-38510 Military Detail Specifications (in the SMD format) | 5962-XXXXXZZ(B or S)YY | QPL-38510 (Part 1 or 2) | MIL-BUL-103 |
| New MIL-H-38534 Standardized Military Drawings | 5962-XXXXXZZ(H or K)YY | QML-38534 | MIL-BUL-103 |
| New MIL-I-38535 Standardized Military Drawings | 5962-XXXXXZZ(Q or V)YY | QML-38535 | MIL-BUL-103 |
| New 1.2.1 of MIL-STD-883 Standardized Military Drawings | 5962-XXXXXZZ(M)YY | MIL-BUL-103 | MIL-BUL-103 |

6.7 Sources of supply.

6.7.1 Sources of supply for device classes B and S. Sources of supply for device classes B and S are listed in QPL-38510.

6.7.2 Sources of supply for device classes Q and V. Sources of supply for device classes Q and V are listed in QML-38535. The vendors listed in QML-38535 have submitted a certificate of compliance (see 3.6 herein) to DESC-ECS and have agreed to this drawing.

6.7.3 Approved sources of supply for device class M. Approved sources of supply for class M are listed in MIL-BUL-103. The vendors listed in MIL-BUL-103 have agreed to this drawing and a certificate of compliance (see 3.6 herein) has been submitted to and accepted by DESC-ECS.

APPENDIX

FUNCTIONAL ALGORITHMS

10. SCOPE

10.1 Scope. Functional algorithms are test patterns which define the exact sequence of events used to verify proper operation of a random access memory (RAM). Each algorithm serves a specific purpose for the testing of the device. It is understood that all manufacturers do not have the same test equipment; therefore, it becomes the responsibility of each manufacturer to guarantee that the test patterns described herein are followed as closely as possible, or equivalent patterns be used that serve the same purpose. Each manufacturer should demonstrate that this condition will be met. Algorithms shall be applied to the device in a topologically pure fashion. This appendix is a mandatory part of the specification. The information contained herein is intended for compliance.

20. APPLICABLE DOCUMENTS

This section is not applicable to this appendix.

30. ALGORITHMS

30.1 Algorithm A (pattern 1).

30.1.1 Output high impedance ($t_{OFF}$). This pattern verifies the output buffer switches to high impedence (three-state) within the specified $t_{OFF}$ after the rise of CAS. It is performed in the following manner:

Step 1: Perform 8 pump cycles.
Step 2: Load address location with data.
Step 3: Raise CAS and read address location and guarantee $V_{OL} < V_{OUT} < V_{OH}$ after $t_{OFF}$ delay.

30.2 Algorithm B (pattern 2).

30.2.1 Vcc Slew. This pattern indicates sense amplifier margin by slewing the supply voltage between memory writing and reading. It is performed in the following manner:

Step 1: Perform 8 pump cycles.
Step 2: Load memory with background data with Vcc at 5.0 V.
Step 3: Change Vcc to 5.5 V.
Step 4: Read memory with background data.
Step 5: Load memory with background data complement.
Step 6: Change Vcc to 4.5 V.
Step 7: Read memory with background data complement.

30.3 Algorithm C (pattern 3).

30.3.1 March data. This pattern tests for address uniqueness and multiple selection. It is performed in the following manner:

Step 1: Perform 8 pump cycles.
Step 2: Load memory with background data.
Step 3: Read location 0.
Step 4: Write data complement in location 0.
Step 5: Repeat step 3 and 4 for all other locations in the memory (sequentially).
Step 6: Read data complement in maximum address location.
Step 7: Write data in maximum address location.
Step 8: Repeat step 6 and 7 for all other locations in the memory from maximum to minimum address.
Step 9: Read data in maximum address location.
Step 10: Write data complement in maximum address location.
Step 11: Repeat step 6 and 7 for all other locations in the memory from maximum to minimum address.
Step 12: Read memory with data complement.

30.4 Algorithm D (pattern 4).

30.4.1 Refresh test (cell retention) +125°C only. This test is used to check the retention time of the memory cells. It is performed in the following manner:

Step 1: Perform 8 pump cycles.
Step 2: Load memory with background data.
Step 3: Pause $T_{REF}$ (stop all clocks).
Step 4: Read memory with background data.
Step 5: Repeat steps 2-4 with data complement.

30.5 Algorithm E (pattern 5).

30.5.1 Read-modify-write (RMW). This pattern verifies the Read-modify-write mode for the memory. It is performed in the following manner:

Step 1: Perform 8 pump cycles.
Step 2: Load memory with background data.
Step 3: Read memory with data and load with data complement using RMW cycle.
Step 4: Repeat step 3 for all address locations.
Step 5: Repeat steps 2 and 3 using data complement.

30.6 Algorithm F (pattern 6).

30.6.1 Page mode. This pattern verifies the Page mode for the memory. It is performed in the following manner:

Step 1: Perform 8 pump cycles.
Step 2: Load first page of memory with background data using Page mode cycle.
Step 3: Read first page of memory with data and load with data complement using Page mode cycle.
Step 4: Read first page of memory with data complement and load with data using Page mode cycle.
Step 5: Repeat steps 2-4 for remaining memory locations.

30.7 Algorithm G (pattern 7).

30.7.1 $\overline{\text{CAS}}$-Before-$\overline{\text{RAS}}$ refresh test. This test is used to verify the functionality of the $\overline{\text{CAS}}$ before RAS mode of cell refreshing. It is done at +125°C only and is performed in the following manner:

Step 1: Perform 8 pump cycles.
Step 2: Load memory with background data.
Step 3: Perform 1024 $\overline{\text{CAS}}$-before-$\overline{\text{RAS}}$ cycles while attempting to modify data.
Step 4: Read memory with background data.

30.8 Algorithm H (pattern 8).

30.8.1 RAS-Only refresh test. This test is used to verify the functionality of the RAS-only mode of cell refreshing. It is done at +125°C only and is performed in the following manner:

Step 1: Perform 8 pump cycles.
Step 2: Load memory with background data.
Step 3: Perform 1024 RAS-only cycles while attempting to modify data.
Step 4: Repeat step 3 for 1 second.
Step 5: Read memory with background data.