REVISIONS			
LTR	DESCRIPTION	DATE (YR-MO-DA)	APPROVED

REV																			
SHEET																			
REV																			
SHEET	15	16	17	18	19	20	21	22	23	24	25	26							

REV STATUS OF SHEETS	REV													
	SHEET	1	2	3	4	5	6	7	8	9	10	11	12	13	14

PMIC N/A

STANDARDIZED MILITARY DRAWING

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AMSC N/A

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DRAWING APPROVAL DATE
94-04-28

REVISION LEVEL

DEFENSE ELECTRONICS SUPPLY CENTER
DAYTON, OHIO 45444

MICROCIRCUIT, LINEAR,
10 BIT, ANALOG-TO-DIGITAL CONVERTER,
MONOLITHIC SILICON

SIZE	CAGE CODE	
A	67268	5962-90642

SHEET 1 OF 26

DESC FORM 193
JUL 91

5962-E152-94

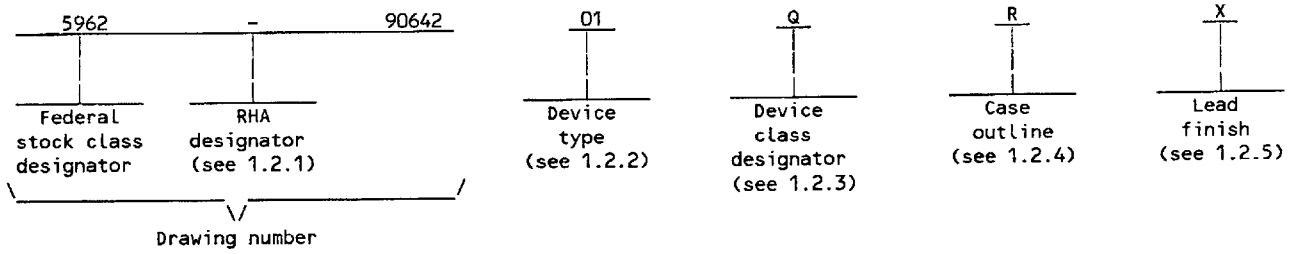
DISTRIBUTION STATEMENT A. Approved for public release; distribution is unlimited.

9004708 0001600 994

1. SCOPE

1.1 Scope. This drawing forms a part of a one part - one part number documentation system (see 6.6 herein). Two product assurance classes consisting of military high reliability (device classes Q and M) and space application (device class V), and a choice of case outlines and lead finishes are available and are reflected in the Part or Identifying Number (PIN). Device class M microcircuits represent non-JAN class B microcircuits in accordance with 1.2.1 of MIL-STD-883, "Provisions for the use of MIL-STD-883 in conjunction with compliant non-JAN devices". When available, a choice of Radiation Hardness Assurance (RHA) levels are reflected in the PIN.

1.2 PIN. The PIN shall be as shown in the following example:



1.2.1 RHA designator. Device class M RHA marked devices shall meet the MIL-I-38535 appendix A specified RHA levels and shall be marked with the appropriate RHA designator. Device classes Q and V RHA marked devices shall meet the MIL-I-38535 specified RHA levels and shall be marked with the appropriate RHA designator. A dash (-) indicates a non-RHA device.

1.2.2 Device type(s). The device type(s) shall identify the circuit function as follows:

Device type	Generic number	Circuit function
01	TLC1541	10 bit, A/D converter
02	TLC1542	10 bit, A/D converter

1.2.3 Device class designator. The device class designator shall be a single letter identifying the product assurance level as follows:

Device class	Device requirements documentation
M	Vendor self-certification to the requirements for non-JAN class B microcircuits in accordance with 1.2.1 of MIL-STD-883
Q or V	Certification and qualification to MIL-I-38535

1.2.4 Case outline(s). The case outline(s) shall be as designated in MIL-STD-1835 and as follows:

Outline letter	Descriptive designator	Terminals	Package style
R	GDIP1-T20 or CDIP2-T20	20	Dual-in-line
2	CQCC1-N20	20	Square leadless chip carrier

1.2.5 Lead finish. The lead finish shall be as specified in MIL-STD-883 (see 3.1 herein) for class M or MIL-I-38535 for classes Q and V. Finish letter "X" shall not be marked on the microcircuit or its packaging. The "X" designation is for use in specifications when lead finishes A, B, and C are considered acceptable and interchangeable without preference.

1.3 Absolute maximum ratings. 1/

Supply voltage (V_{CC})	-0.5 V to +6.0 V
Input voltage range (any input) (V_{IR})	-0.3 V to V_{CC} +0.3 V
Output voltage range (V_{OUT})	-0.3 V to V_{CC} +0.3 V
Positive reference voltage ($+V_{REF}$)	V_{CC} +0.1 V
Negative reference voltage ($-V_{REF}$)	-0.1 V
Peak input current range (any input):	
Device type 01	±10 mA
Device type 02	±20 mA
Peak total input current (all inputs)	±30 mA
Storage temperature range	-65°C to +150°C
Case temperature for 60 seconds:	
Case R	300°C
Case 2	260°C
Thermal resistance, junction-to-case (Θ_{JC})	See MIL-STD-1835

1.4 Recommended operating conditions.

Supply voltage (V_{CC}):	
Device type 01	+4.75 V to +5.5 V
Device type 02	+4.5 V to +5.5 V
Positive reference voltage ($+V_{REF}$)	V_{CC} 2/
Negative reference voltage ($-V_{REF}$)	0 V 2/
Differential reference voltage ($+V_{REF} - -V_{REF}$)	V_{CC} 2/
Analog input voltage	0 V to V_{CC} 2/
High level control input voltage (V_{IH})	2 V minimum
Low level control input voltage (V_{IL})	0.8 V maximum
Setup time, address bits at data before I/O CLK↑ (t_{SUA}):	
Device type 01	400 ns
Device type 02	100 ns
Hold time, address bits after I/O CLK↑ (t_{HA})	0 ns 3/
Hold time, CS low after 10th I/O CLK↓ (t_{HCS}):	
Device type 02 only	0 ns 3/
Setup time, CS low before clocking in first address bit (t_{SUCS}):	
Device type 01	4 system clock cycles 4/
Device type 02	1.425 µs 4/
Input/output clock frequency, $f_{CLK(I/O)}$:	
Device type 01	1.1 MHz
Device type 02	2.1 MHz
Input/output clock high, $t_{WH(I/O)}$:	
Device type 01	455 ns
Device type 02	190 ns
Input/output clock low, $t_{WL(I/O)}$:	
Device type 01	455 ns
Device type 02	190 ns
Input/output clock transition time:	
Device type 01	($f_{CLK(SYS)}$ ≤ 1048 kHz) = 30 ns 3/ ($f_{CLK(SYS)}$ > 1048 kHz) = 20 ns ($f_{CLK(SYS)}$ ≤ 525 kHz) = 100 ns ($f_{CLK(SYS)}$ > 525 kHz) = 40 ns
Device type 02	1 ms 3/
Ambient operating temperature (T_A)	-55°C to +125°C

2. APPLICABLE DOCUMENTS

2.1 Government specification, standards, bulletin, and handbook. Unless otherwise specified, the following specification, standards, bulletin, and handbook of the issue listed in that issue of the Department of Defense Index of Specifications and Standards specified in the solicitation, form a part of this drawing to the extent specified herein.

SPECIFICATION

MILITARY

MIL-I-38535 - Integrated Circuits, Manufacturing, General Specification for.

STANDARDS

MILITARY

MIL-STD-883 - Test Methods and Procedures for Microelectronics.
MIL-STD-973 - Configuration Management.
MIL-STD-1835 - Microcircuit Case Outlines.

BULLETIN

MILITARY

MIL-BUL-103 - List of Standardized Military Drawings (SMD's).

HANDBOOK

MILITARY

MIL-HDBK-780 - Standardized Military Drawings.

(Copies of the specification, standards, bulletin, and handbook required by manufacturers in connection with specific acquisition functions should be obtained from the contracting activity or as directed by the contracting activity.)

2.2 Order of precedence. In the event of a conflict between the text of this drawing and the references cited herein, the text of this drawing shall take precedence.

1/ Unless otherwise specified, all voltage values are with respect to digital ground with -REF and GND wired together.

2/ Analog input voltages greater than that applied to +REF convert as all ones (11111111), while input voltages less than that applied to -REF convert as well as all zeros (00000000). For proper operation, +REF voltage must be at least 1 volt higher than -REF voltage. Also, the total unadjusted error may increase as this differential reference voltage falls below 4.75 volts.

3/ This is the time required for the clock input signal to fall from V_{IH} minimum to V_{IL} maximum or to rise from V_{IL} maximum to V_{IH} minimum. In the vicinity of normal room temperature, the devices function with input clock transition time as slow as 2 microseconds for remote data acquisition application where the sensor and the A/D converter are placed several feet away from the controlling microprocessor. These parameters are test machine limited. The slope on drivers and comparators is approximately 1 ns/V, and therefore the clock transition is fixed at a maximum of 2 ns for all these parameters.

4/ To minimize errors caused by noise at the chip select input, the internal circuitry waits for three system clock cycles (or less) after chip select falling edge is detected before responding to control input signals. Therefore, no attempt should be made to clock-in address until the minimum chip select setup time has elapsed.

3. REQUIREMENTS

3.1 Item requirements. The individual item requirements for device class M shall be in accordance with 1.2.1 of MIL-STD-883, "Provisions for the use of MIL-STD-883 in conjunction with compliant non-JAN devices" and as specified herein. The individual item requirements for device classes Q and V shall be in accordance with MIL-I-38535, the device manufacturer's Quality Management (QM) plan, and as specified herein.

3.2 Design, construction, and physical dimensions. The design, construction, and physical dimensions shall be as specified in MIL-STD-883 (see 3.1 herein) for device class M and MIL-I-38535 for device classes Q and V and herein.

3.2.1 Case outline(s). The case outline(s) shall be in accordance with 1.2.4 herein.

3.2.2 Terminal connections. The terminal connections shall be as specified on figure 1.

3.2.3 Logic diagram(s). The logic diagram(s) shall be as specified on figure 2.

3.3 Electrical performance characteristics and postirradiation parameter limits. Unless otherwise specified herein, the electrical performance characteristics and postirradiation parameter limits are as specified in table I and shall apply over the full ambient operating temperature range.

3.4 Electrical test requirements. The electrical test requirements shall be the subgroups specified in table II. The electrical tests for each subgroup are defined in table I.

3.5 Marking. The part shall be marked with the PIN listed in 1.2 herein. Marking for device class M shall be in accordance with MIL-STD-883 (see 3.1 herein). In addition, the manufacturer's PIN may also be marked as listed in MIL-BUL-103. Marking for device classes Q and V shall be in accordance with MIL-I-38535.

3.5.1 Certification/compliance mark. The compliance mark for device class M shall be a "C" as required in MIL-STD-883 (see 3.1 herein). The certification mark for device classes Q and V shall be a "QML" or "Q" as required in MIL-I-38535.

3.6 Certificate of compliance. For device class M, a certificate of compliance shall be required from a manufacturer in order to be listed as an approved source of supply in MIL-BUL-103 (see 6.7.2 herein). For device classes Q and V, a certificate of compliance shall be required from a QML-38535 listed manufacturer in order to supply to the requirements of this drawing (see 6.7.1 herein). The certificate of compliance submitted to DESC-EC prior to listing as an approved source of supply for this drawing shall affirm that the manufacturer's product meets, for device class M, the requirements of MIL-STD-883 (see 3.1 herein), or for device classes Q and V, the requirements of MIL-I-38535 and the requirements herein.

3.7 Certificate of conformance. A certificate of conformance as required for device class M in MIL-STD-883 (see 3.1 herein) or for device classes Q and V in MIL-I-38535 shall be provided with each lot of microcircuits delivered to this drawing.

3.8 Notification of change for device class M. For device class M, notification to DESC-EC of change of product (see 6.2 herein) involving devices acquired to this drawing is required for any change as defined in MIL-STD-973.

3.9 Verification and review for device class M. For device class M, DESC, DESC's agent, and the acquiring activity retain the option to review the manufacturer's facility and applicable required documentation. Offshore documentation shall be made available onshore at the option of the reviewer.

3.10 Microcircuit group assignment for device class M. Device class M devices covered by this drawing shall be in microcircuit group number 57 (see MIL-I-38535, appendix A).

4. QUALITY ASSURANCE PROVISIONS

4.1 Sampling and inspection. For device class M, sampling and inspection procedures shall be in accordance with MIL-STD-883 (see 3.1 herein). For device classes Q and V, sampling and inspection procedures shall be in accordance with MIL-I-38535 and the device manufacturer's QM plan.

TABLE I. Electrical performance characteristics.

Test	Symbol	Conditions 1/ $-55°C \le T_A \le +125°C$ unless otherwise specified	Group A subgroups	Device type	Limits 2/ Min	Limits 2/ Max	Unit
High level output voltage	V_{OH}	V_{CC} = 4.75 V, I_{OH} = -360 µA	1,2,3	01	2.4		V
		V_{CC} = 4.5 V, I_{OH} = -1.6 mA		02	2.4		
		V_{CC} = 4.5 V to 5.5 V, I_{OH} = -20 µA			V_{CC} -0.1		
Low level output voltage	V_{OL}	V_{CC} = 4.75 V, I_{OL} = 3.2 mA	1,2,3	01		0.4	V
		V_{CC} = 4.5 V, I_{OL} = 1.6 mA		02		0.4	
		V_{CC} = 4.5 V to 5.5 V, I_{OH} = 20 µA				0.1	
Off-state (high-impedance state) output current	I_{OZ}	V_O = V_{CC}, $\overline{CS}$ at V_{CC}, V_{CC} = 5.5 V	1,2,3	All		10	µA
		V_O = 0 V, $\overline{CS}$ at V_{CC}, V_{CC} = 5.5 V				-10	
High level input current	I_{IH}	V_I = V_{CC}, V_{CC} = 5.5 V	1,2,3	All		2.5	µA
Low level input current	I_{IL}	V_I = 0 V, V_{CC} = 5.5 V	1,2,3	All		-2.5	µA
Operating supply current	I_{CC}	$\overline{CS}$ at 0 V	1,2,3	All		2.5	mA
Selected channel leakage current	I_{SCL}	Selected channel at V_{CC}, unselected channel at 0 V, V_{CC} = 5.5 V	1	All		1	µA
		Selected channel at 0 V, unselected channel at V_{CC}, V_{CC} = 5.5 V				-1	

See footnotes at end of table.

TABLE I. Electrical performance characteristics - Continued.

Test	Symbol	Conditions 1/ $-55°C \le T_A \le +125°C$ unless otherwise specified	Group A subgroups	Device type	Limits 2/		Unit
					Min	Max	
Selected channel leakage current	I_{SCL}	Selected channel at V_{CC}, unselected channel at 0 V, V_{CC} = 5.5 V	2,3	02		2.5	µA
		Selected channel at 0 V, unselected channel at V_{CC}, V_{CC} = 5.5 V				-2.5	
Supply and reference current	I_{CC} + I_{REF}	$V_{REF+} = V_{CC}$, $\overline{CS}$ at 0 V, V_{CC} = 5.5 V	1,2,3	01		3	mA
Maximum static analog reference current into REF+	I_{REF}	$V_{REF+} = V_{CC}$, V_{REF-} = GND	1,2,3	02		100	µA
Input capacitance	C_{IN}	Analog inputs, see 4.4.1c	4	All		55	pF
		Control inputs, see 4.4.1c				20	
Linearity error	LE	3/	4,5,6	01		±1	LSB
			4	02		±0.5	
			5,6			±1	
Zero error	ZE	4/ 5/	4,5,6	01		±1	LSB
			4	02		±0.5	
			5,6			±1	
Full-scale error	FSE	4/ 5/	4,5,6	01		±1	LSB
			4	02		±0.5	
			5,6			±1	

See footnotes at end of table.

TABLE I. Electrical performance characteristics - Continued.

Test	Symbol	Conditions 1/ $-55°C \le T_A \le +125°C$ unless otherwise specified	Group A subgroups	Device type	Limits 2/ Min	Limits 2/ Max	Unit
Total unadjusted error	TUE	6/	4,5,6	01		±1	LSB
			4	02		±0.5	
			5,6			±1	
Conversion time	t_{CONV}	See figure 4, V_{CC} = 5.0 V	9,10,11	All		21	µs
Total access and conversion time	t_{CYCLE}	See figure 4, V_{CC} = 5.0 V	9,10,11	01		31	µs
				02		21 +10 I/O clock cycles	
Channel acquistion time (sample cycle)	t_{ACQ}	See figure 4, V_{CC} = 5.0 V	9,10,11	All		6	I/O clock cycles
Time output data remains valid after I/O clock ↓	t_V	V_{CC} = 5.0 V	9,10,11	02	10		ns
Delay time, I/O clock ↓ to data output valid	t_D (I/O-DATA)	See figure 5, V_{CC} = 5.0 V	9,10,11	02		240	ns
Delay time, 10th I/O clock ↓ to EOC ↓	t_D (I/O-EOC)	See figure 5, V_{CC} = 5.0 V	9,10,11	02		1.35	µs
Delay time, $\overline{EOC}$ ↑ to data out (MSB)	t_D (EOC-DATA)	See figure 5, V_{CC} = 5.0 V	9,10,11	02		100	ns
Delay time, $\overline{CS}$ ↑ to data out (MSB)	t_{PZH}, t_{PZL}	See figure 5, V_{CC} = 5.0 V	9,10,11	02		1.3	µs
Delay time, $\overline{CS}$ ↓ to data out	t_{PHZ}, t_{PLZ}	See figure 5, V_{CC} = 5.0 V	9,10,11	02		150	ns
Rise time	t_R (EOC)	See figure 5, V_{CC} = 5.0 V	9,10,11	02		300	ns

See footnotes at end of table.

TABLE I. Electrical performance characteristics - Continued.

Test	Symbol	Conditions 1/ $-55°C \le T_A \le +125°C$ unless otherwise specified	Group A subgroups	Device type	Limits 2/		Unit
					Min	Max	
Fall time	t_F (EOC)	See figure 5, V_{CC} = 5.0 V	9,10,11	02		300	ns
Data bus rise time 7/	$t_{R\ BUS}$	See figure 5, V_{CC} = 5.0 V	9,10,11	All		300	ns
Data bus fall time 7/	$t_{F\ BUS}$	See figure 5, V_{CC} = 5.0 V	9,10,11	All		300	ns
Delay time, 10 th I/O CLK out to CS out to abort conversion	t_D I/O-CS	See figure 5, V_{CC} = 5.0 V	9,10,11	02		9	µs

1/ Unless otherwise specified, $V_{CC} = V_{REF+}$ = 4.75 V to 5.5 V. For device type 01, $f_{CLK(I/O)}$ = 1.1 MHz and $f_{CLK(SYS)}$ = 2.1 MHz. For device type 02, $f_{CLK(I/O)}$ = 2.1 MHz. See figure 3 for load circuits.

2/ The limiting terms "min" (minimum) and "max" (maximum) shall be considered to apply to magnitudes only. Negative current shall be defined as conventional current flow out of a device terminal.

3/ Linearity error is the maximum deviation from the best straight line through the A/D transfer characteristics.

4/ Analog input voltages greater than that applied to REF+ convert as all "1"s (1111111111), while input voltages less than that applied to REF- convert as all "0"s (0000000000). For proper operation, REF+ voltage must be at least 1 V higher than REF- voltage. Also, the total unadjusted error may increase as this differential reference voltage falls below 4.75 V.

5/ Zero error is the difference between 0000000000 and the converted output for zero input voltage; full-scale error is the difference between 1111111111 and the converted output for full-scale input voltage.

6/ Total unadjusted error comprises linearity, zero, and full scale errors.

7/ If not tested, shall be guaranteed to the limits specified in table I herein.

Device types	01	02
Case outlines	R and 2	R and 2
Terminal number	Terminal symbol	
1	INPUT A0	INPUT A0
2	INPUT A1	INPUT A1
3	INPUT A2	INPUT A2
4	INPUT A3	INPUT A3
5	INPUT A4	INPUT A4
6	INPUT A5	INPUT A5
7	INPUT A6	INPUT A6
8	INPUT A7	INPUT A7
9	INPUT A8	INPUT A8
10	GND	GND
11	INPUT A9	INPUT A9
12	INPUT A10	INPUT A10
13	REF-	REF-
14	REF+	REF+
15	$\overline{CS}$	$\overline{CS}$
16	DATA OUT	DATA OUT
17	ADDRESS INPUT	ADDRESS INPUT
18	I/O CLOCK	I/O CLOCK
19	SYSTEM CLOCK	$\overline{EOC}$
20	V_{CC}	V_{CC}

FIGURE 1. Terminal connections.

Device type 01

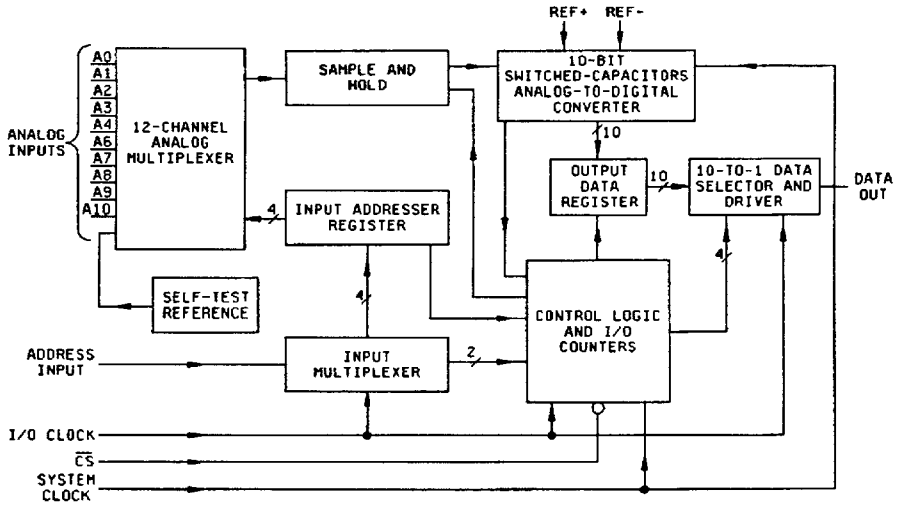


FIGURE 2. Block diagram.

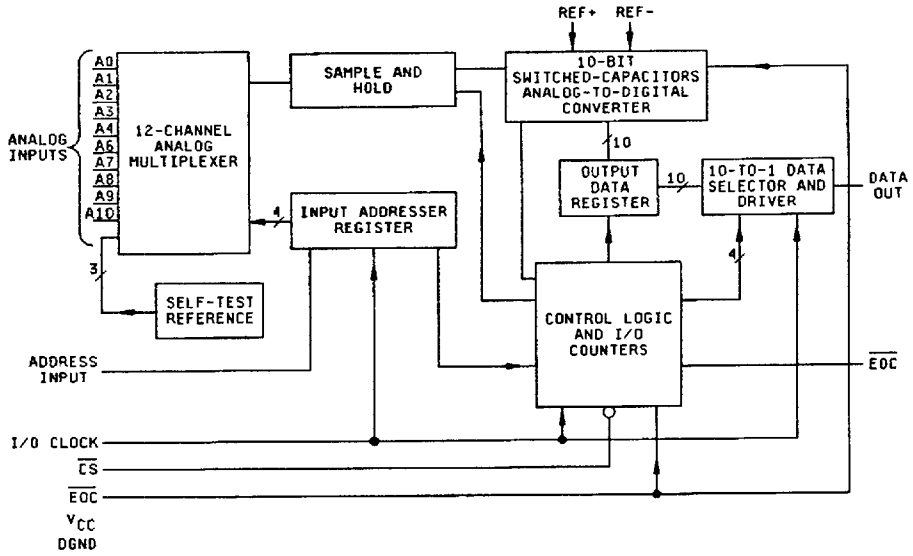
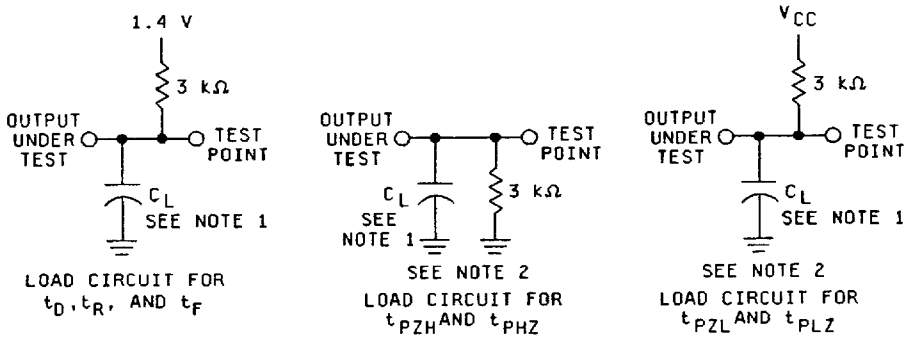
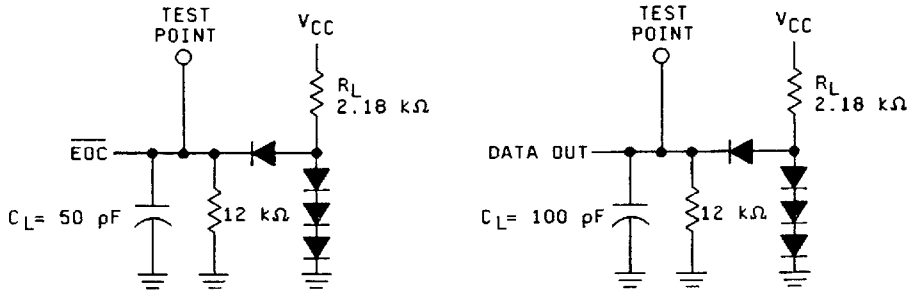


FIGURE 2. Block diagram - Continued.

Device type 01



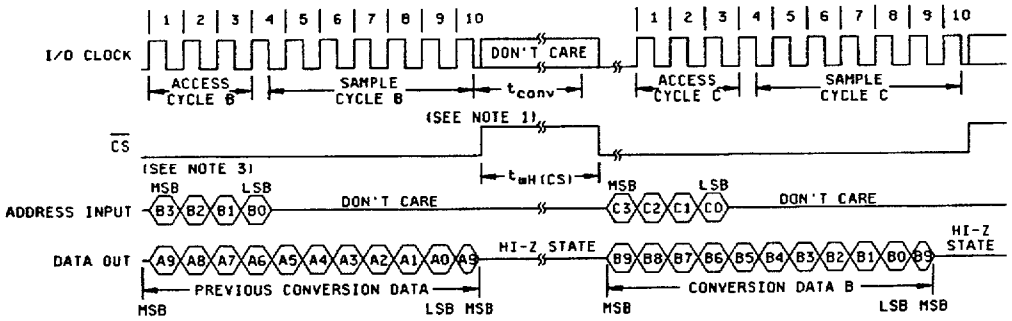
Device type 02



NOTES: 1. C_L = 50 pF.

2. $t_{EN} = t_{PZH}$ or t_{PZL}, $t_{DIS} = t_{PHZ}$ or t_{PLZ}.

FIGURE 3. Load circuits.

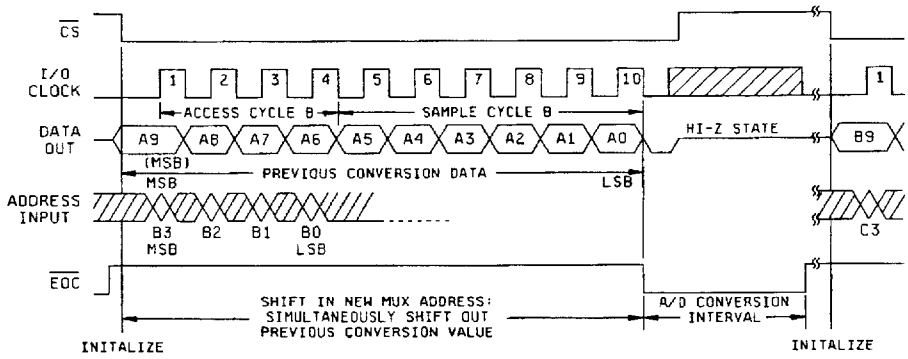


NOTES:

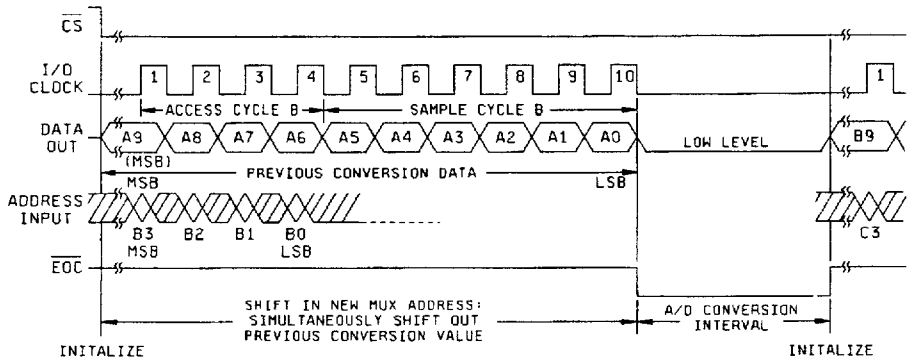
1. The conversion cycle, which requires 44 system clock periods, is initiated on the 10th falling edge after $\overline{CS}$ goes low for the channel whose address exists in memory at this time. If $\overline{CS}$ is kept low during conversion, the I/O clock must remain low for at least 44 systems clock cycles to allow conversion to be completed.
2. The most significant bit (MSB) will automatically be placed on the DATA OUT bus after $\overline{CS}$ is brought low. The remaining nine bits (A8-A0) will be clocked out on the first nine I/O clock falling edges.
3. To minimize errors caused by noise at the $\overline{CS}$ input, the internal circuitry waits for three system clock cycles (or less) after a chip select falling edge is detected before responding to control input signals. Therefore, no attempt should be made to clock in address data until the minimum chip select setup time has elapsed.

FIGURE 4. Timing diagrams.

Device type 02



Timing fo 10-clock transfer using $\overline{CS}$.

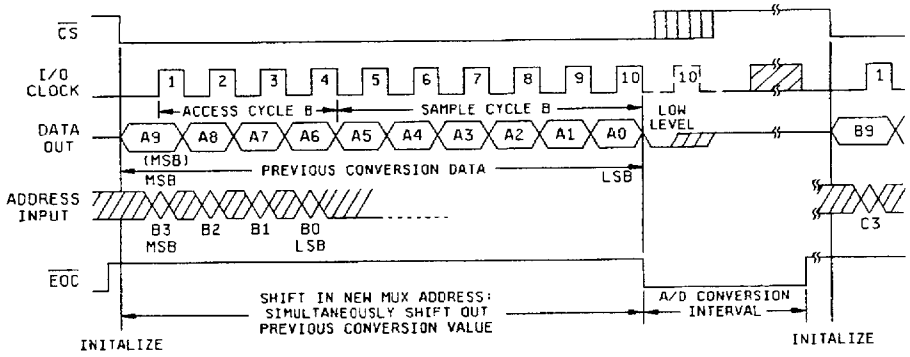


Timing for 10-clock transfer not using $\overline{CS}$.

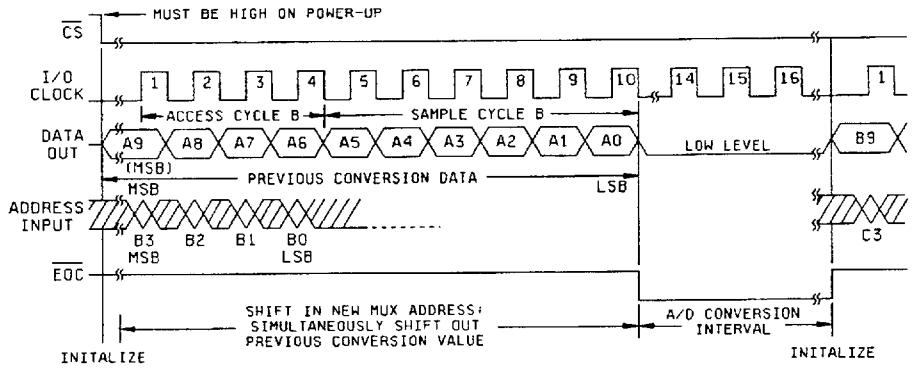
NOTE: To minimize errors caused by noise in the chip select input, the internal circuitry waits for two rising edges and one falling edge of the internal system clock after $\overline{CS}$ ↓ before responding to control input signals. Therefore, no attempt should be made to clock in an address until the minimum chip select setup time has elapsed.

FIGURE 4. Timing diagrams - Continued.

Device type 02



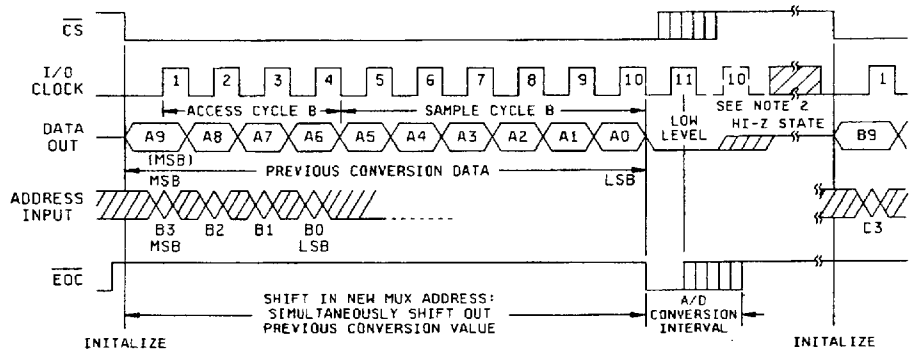
MODE 1. Timing for 11 to 16 clock transfer using $\overline{CS}$ (serial transfer interval shorter than conversion).



MODE 2. Timing for 16 clock transfer not using $\overline{CS}$ (serial transfer interval shorter than conversion).

NOTE: To minimize errors caused by noise in the chip select input, the internal circuitry waits for two rising edges and one falling edge of the internal system clock after $\overline{CS}$ ↓ before responding to control input signals. Therefore , no attempt should be made to clock in an address until the minimum chip select setup time has elapsed.

FIGURE 4. Timing diagrams - Continued.

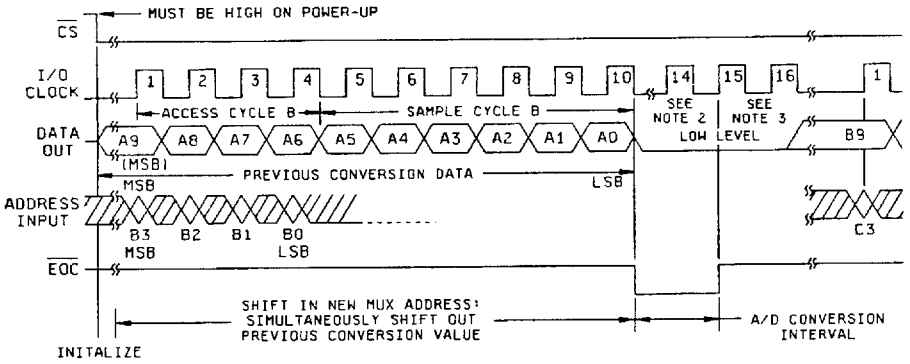


MODE 3. Timing for 11 to 16 clock transfer using $\overline{CS}$ (serial transfer interval longer than conversion).

NOTES: 1. To minimize errors caused by noise at the chip select input, the internal circuitry waits for two rising edges and one falling edge the internal system clock after $\overline{CS}$ ↓ before responding to control input signals. Therefore, no attempt should be made to clock address until the minimum chip select setup time has elapsed.

2. The 11th rising edge of the I/O clock sequence must occur before the conversion is complete to prevent losing SPI synchronized.

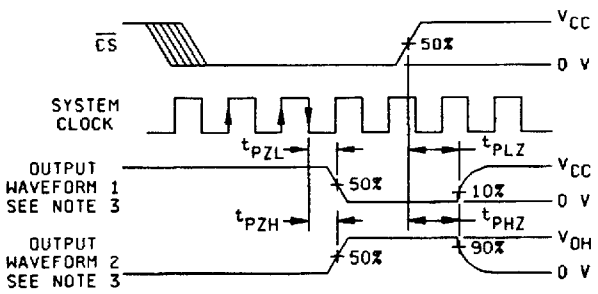
FIGURE 4. Timing diagrams - Continued.



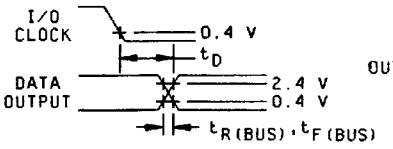
MODE 4. Timing for 11 to 16 clock transfer using not $\overline{CS}$ (serial transfer interval longer than conversion).

NOTES:
1. To minimize errors caused by noise at the chip select input, the internal circuitry waits for two rising edges and one falling edge the internal system clock after $\overline{CS}$ ↓ before responding to control input signals. Therefore, no attempt should be made to clock in address until the minimum chip select setup time has elapsed.
2. The 11th rising edge of the I/O clock sequence must occur before the conversion is complete to prevent losing SPI synchronized.
3. The I/O clock sequence is exactly 16 clock pulses long.

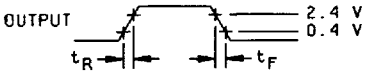
FIGURE 4. Timing diagrams - Continued.



VOLTAGE WAVEFORMS FOR ENABLE AND DISABLE TIMES



VOLTAGE WAVEFORMS FOR DELAY TIME



VOLTAGE WAVEFORMS FOR RISE AND FALL TIMES

NOTES: 1. C_L = 50 pF.

2. $t_{EN} = t_{PZH}$ or t_{PZL}, $t_{DIS} = t_{PHZ}$ or t_{PLZ}.

3. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control.
Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.

FIGURE 5. Timing waveforms.

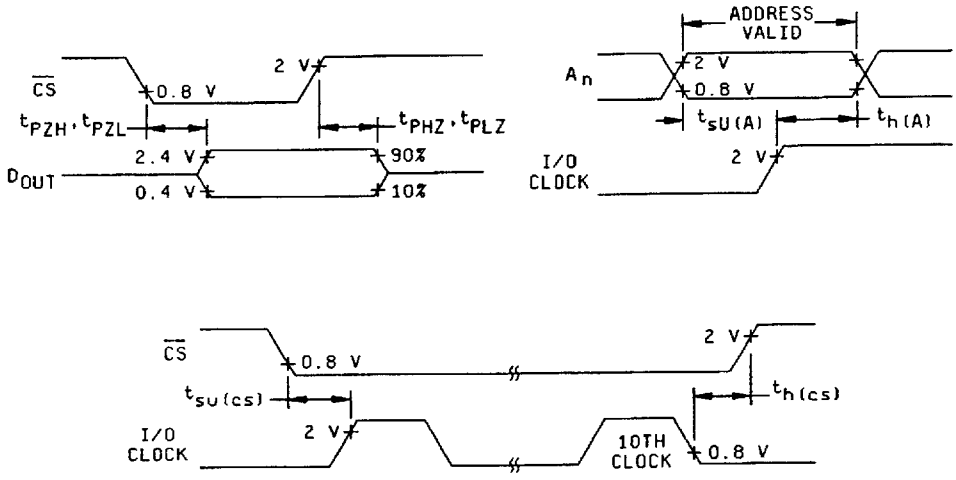


FIGURE 5. Timing waveforms - Continued.

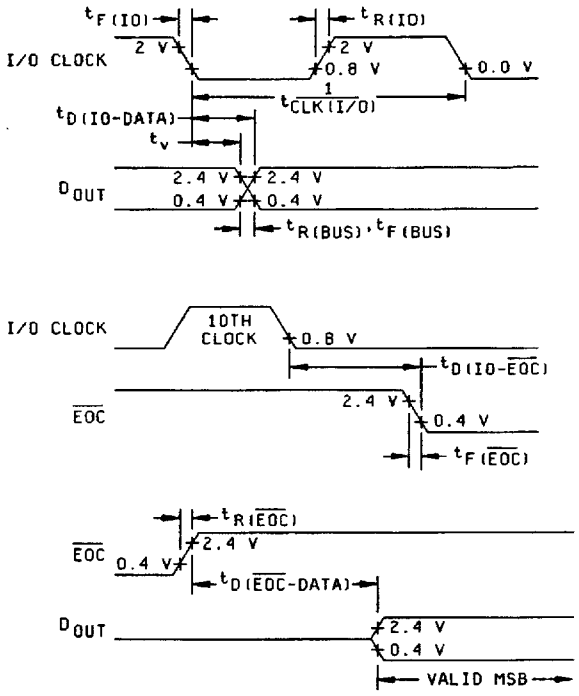


FIGURE 5. Timing waveforms - Continued.

4.2 Screening. For device class M, screening shall be in accordance with method 5004 of MIL-STD-883, and shall be conducted on all devices prior to quality conformance inspection. For device classes Q and V, screening shall be in accordance with MIL-I-38535, and shall be conducted on all devices prior to qualification and technology conformance inspection.

4.2.1 Additional criteria for device class M.

a. Burn-in test, method 1015 of MIL-STD-883.

(1) Test condition B or D. The test circuit shall be maintained by the manufacturer under document revision level control and shall be made available to the preparing or acquiring activity upon request. The test circuit shall specify the inputs, outputs, biases, and power dissipation, as applicable, in accordance with the intent specified in test method 1015.

(2) T_A = +125°C, minimum.

b. Interim and final electrical test parameters shall be as specified in table II herein.

4.2.2 Additional criteria for device classes Q and V.

a. The burn-in test duration, test condition and test temperature, or approved alternatives shall be as specified in the device manufacturer's QM plan in accordance with MIL-I-38535. The burn-in test circuit shall be maintained under document revision level control of the device manufacturer's Technology Review Board (TRB) in accordance with MIL-I-38535 and shall be made available to the acquiring or preparing activity upon request. The test circuit shall specify the inputs, outputs, biases, and power dissipation, as applicable, in accordance with the intent specified in test method 1015.

b. Interim and final electrical test parameters shall be as specified in table II herein.

c. Additional screening for device class V beyond the requirements of device class Q shall be as specified in appendix B of MIL-I-38535.

4.3 Qualification inspection for device classes Q and V. Qualification inspection for device classes Q and V shall be in accordance with MIL-I-38535. Inspections to be performed shall be those specified in MIL-I-38535 and herein for groups A, B, C, D, and E inspections (see 4.4.1 through 4.4.4).

4.4 Conformance inspection. Quality conformance inspection for device class M shall be in accordance with MIL-STD-883 (see 3.1 herein) and as specified herein. Inspections to be performed for device class M shall be those specified in method 5005 of MIL-STD-883 and herein for groups A, B, C, D, and E inspections (see 4.4.1 through 4.4.4). Technology conformance inspection for classes Q and V shall be in accordance with MIL-I-38535 including groups A, B, C, D, and E inspections and as specified herein except where option 2 of MIL-I-38535 permits alternate in-line control testing.

4.4.1 Group A inspection.

a. Tests shall be as specified in table II herein.

b. Subgroups 7 and 8 in table I, method 5005 of MIL-STD-883 shall be omitted.

c. Subgroup 4 (C_{IN} measurements) shall be measured only for the initial test and after process or design changes which may affect input capacitance.

4.4.2 Group C inspection. The group C inspection end-point electrical parameters shall be as specified in table II herein.

TABLE II. Electrical test requirements.

Test requirements	Subgroups (in accordance with MIL-STD-883, TM 5005, table I)	Subgroups (in accordance with MIL-I-38535, table III)	
	Device class M	Device class Q	Device class V
Interim electrical parameters (see 4.2)	---	---	---
Final electrical parameters (see 4.2)	1,2,3,4,5, 6,9,10,11 1/	1,2,3,4,5, 6,9,10,11 1/	1,2,3,4, 5,6,9,10,11 1/
Group A test requirements (see 4.4)	1,2,3,4,5,6, 9,10,11	1,2,3,4,5,6, 9,10,11	1,2,3,4,5,6, 9,10,11
Group C end-point electrical parameters (see 4.4)	1	1	1
Group D end-point electrical parameters (see 4.4)	1	1	1
Group E end-point electrical parameters (see 4.4)	---	---	---

1/ PDA applies to subgroup 1.

4.4.2.1 Additional criteria for device class M. Steady-state life test conditions, method 1005 of MIL-STD-883:

a. Test condition B or D. The test circuit shall be maintained by the manufacturer under document revision level control and shall be made available to the preparing or acquiring activity upon request. The test circuit shall specify the inputs, outputs, biases, and power dissipation, as applicable, in accordance with the intent specified in test method 1005.

b. T_A = +125°C, minimum.

c. Test duration: 1,000 hours, except as permitted by method 1005 of MIL-STD-883.

4.4.2.2 Additional criteria for device classes Q and V. The steady-state life test duration, test condition and test temperature, or approved alternatives shall be as specified in the device manufacturer's QM plan in accordance with MIL-I-38535. The test circuit shall be maintained under document revision level control by the device manufacturer's TRB, in accordance with MIL-I-38535, and shall be made available to the acquiring or preparing activity upon request. The test circuit shall specify the inputs, outputs, biases, and power dissipation, as applicable, in accordance with the intent specified in test method 1005.

4.4.3 Group D inspection. The group D inspection end-point electrical parameters shall be as specified in table II herein.

4.4.4 Group E inspection. Group E inspection is required only for parts intended to be marked as radiation hardness assured (see 3.5 herein). RHA levels for device classes Q and V shall be M, D, R, and H and for device class M shall be M and D.

a. End-point electrical parameters shall be as specified in table II herein.

b. For device class M, the devices shall be subjected to radiation hardness assured tests as specified in MIL-I-38535, appendix A, for the RHA level being tested. For device classes Q and V, the devices or test vehicle shall be subjected to radiation hardness assured tests as specified in MIL-I-38535 for the RHA level being tested. All device classes must meet the postirradiation end-point electrical parameter limits as defined in table I at T_A = +25°C ±5°C, after exposure, to the subgroups specified in table II herein.

c. When specified in the purchase order or contract, a copy of the RHA delta limits shall be supplied.

5. PACKAGING

5.1 Packaging requirements. The requirements for packaging shall be in accordance with MIL-STD-883 (see 3.1 herein) for device class M and MIL-I-38535 for device classes Q and V.

6. NOTES

6.1 Intended use. Microcircuits conforming to this drawing are intended for use for Government microcircuit applications (original equipment), design applications, and logistics purposes.

6.1.1 Replaceability. Microcircuits covered by this drawing will replace the same generic device covered by a contractor-prepared specification or drawing.

6.1.2 Substitutability. Device class Q devices will replace device class M devices.

6.2 Configuration control of SMD's. All proposed changes to existing SMD's will be coordinated with the users of record for the individual documents. This coordination will be accomplished in accordance with MIL-STD-973 using DD Form 1692, Engineering Change Proposal.

6.3 Record of users. Military and industrial users shall inform Defense Electronics Supply Center when a system application requires configuration control and which SMD's are applicable to that system. DESC will maintain a record of users and this list will be used for coordination and distribution of changes to the drawings. Users of drawings covering microelectronic devices (FSC 5962) should contact DESC-EC, telephone (513) 296-6047.

6.4 Comments. Comments on this drawing should be directed to DESC-EC, Dayton, Ohio 45444-5270, or telephone (513) 296-5377.

6.5 Abbreviations, symbols, and definitions.

ADDRESS INPUT	Serial address input. A 4-bit serial address selects the desired analog input or test voltage that will be converted next. The address data is presented with the MSB first and is shifted in on the first four rising edges of the I/O clock. After the four address bits have been read into the address regulator, this pin is ignored for the remainder of the current conversions period.
A0 to A10	Analog signal inputs. The 11 analog inputs are applied to those terminals and are normally multiplexed.
$\overline{CS}$	Chip select. A high-to-low transition on this input resets the internal counters and controls and enable the ADDRESS INPUT, DATA OUTPUT, and I/O CLK inputs. Within the specified time consisted, high-to-low transitions CS during an ongoing conversion aborts the conversion.
DATA OUT	The three-state serial output for the A/D conversion result. This output is in the high impedance state when CS is high and active when CS is low. With a valid chip select, DATA OUT is removed from the high impedance state and is driven to the logic level corresponding to the MSB value of the previous conversion result. The next falling edge of the I/O clock drives the output to the logic level corresponding to the next most significant bit, and the remaining bits are shifted out in order, with the LSB appearing on the ninth falling edge of the I/O clock. On the tenth falling edge of the I/O clock, DATA OUT is driven to a l;ow logic level so that SPI data transfer of more than 10 clocks produce zeroes as the unused LSBs.

$\overline{EOC}$	End of conversion. This output goes from a high to a low logic level on the trailing edge of the tenth I/O clock and remains low until the conversion is completed and data are ready for transfer.
SYSTEM CLOCK	Once a clock signal is applied to the system clock input, the control hardware and software need only be concerned with addressing the desired analog channel, reading the previous conversion result, and starting the conversion by using the I/O clock. The system clock will drive the "conversion crunching" circuitry so that the control hardware and software need not be concerned with this task.
GND	The ground return pin for the internal circuitry. Unless otherwise noted all voltage measurements are with respect to this terminal.
I/O CLK	Input/Output clock. This terminal receives the serial I/O clock input and performs the following four functions: 1) It clocks the four input address bits into the address register on the list four rising edges of the I/O clock, with the MUX address available on the fourth rising edge. 2) On the fourth falling edge of the I/O clock, the analog input voltage on the selected MUX input begins charging the RC DAC and continues to do so until the tenth falling edge of the I/O clock. 3) It shifts the nine remaining bits of the previous conversions data out on the DATA OUT output. 4) It transfer control of the conversion to the internal state controller on the falling edge of the tenth clock.
REF+	The upper reference voltage value (nominally V_{CC}) is applied to this terminal. The maximum input voltage range is determined by the difference between the voltage applied to this terminal and the voltage applied to the REF- terminal.
REF-	The lower reference voltage value (nominally ground) is applied to this terminal.
V_{CC}	The positive supply voltage pin.

6.6 One part - one part number system. The one part - one part number system described below has been developed to allow for transitions between identical generic devices covered by the three major microcircuit requirements documents (MIL-H-38534, MIL-I-38535, and 1.2.1 of MIL-STD-883) without the necessity for the generation of unique PIN's. The three military requirements documents represent different class levels, and previously when a device manufacturer upgraded military product from one class level to another, the benefits of the upgraded product were unavailable to the Original Equipment Manufacturer (OEM), that was contractually locked into the original unique PIN. By establishing a one part number system covering all three documents, the OEM can acquire to the highest class level available for a given generic device to meet system needs without modifying the original contract parts selection criteria.

Military documentation format	Example PIN under new system	Manufacturing source listing	Document listing
New MIL-H-38534 Standardized Military Drawings	5962-XXXXXZZ(H or K)YY	QML-38534	MIL-BUL-103
New MIL-I-38535 Standardized Military Drawings	5962-XXXXXZZ(Q or V)YY	QML-38535	MIL-BUL-103
New 1.2.1 of MIL-STD-883 Standardized Military Drawings	5962-XXXXXZZ(M)YY	MIL-BUL-103	MIL-BUL-103

6.7 Sources of supply.

6.7.1 Sources of supply for device classes Q and V. Sources of supply for device classes Q and V are listed in QML-38535. The vendors listed in QML-38535 have submitted a certificate of compliance (see 3.6 herein) to DESC-EC and have agreed to this drawing.

6.7.2 Approved sources of supply for device class M. Approved sources of supply for class M are listed in MIL-BUL-103. The vendors listed in MIL-BUL-103 have agreed to this drawing and a certificate of compliance (see 3.6 herein) has been submitted to and accepted by DESC-EC.