REVISIONS			
LTR	DESCRIPTION	DATE (YR-MO-DA)	APPROVED

REV																			
SHEET																			
REV																			
SHEET	35	36	37	38	39	40	41												
REV																			
SHEET	15	16	17	18	19	20	21	22	23	24	25	26	27	28	29	30	31	32	33	34

REV STATUS OF SHEETS	REV															
	SHEET	1	2	3	4	5	6	7	8	9	10	11	12	13	14	

PMIC N/A

STANDARDIZED MILITARY DRAWING

THIS DRAWING IS AVAILABLE FOR USE BY ALL DEPARTMENTS AND AGENCIES OF THE DEPARTMENT OF DEFENSE

AMSC N/A

PREPARED BY Thomas M. Hess

CHECKED BY Thomas M. Hess

APPROVED BY Monica L. Poelking

DRAWING APPROVAL DATE
93-05-19

REVISION LEVEL

DEFENSE ELECTRONICS SUPPLY CENTER
DAYTON, OHIO 45444

MICROCIRCUIT, DIGITAL, CMOS, UNIVERSAL SERIAL CONTROLLER, MONOLITHIC SILICON

SIZE	CAGE CODE	5962-90657
A	67268	

SHEET 1 OF 41

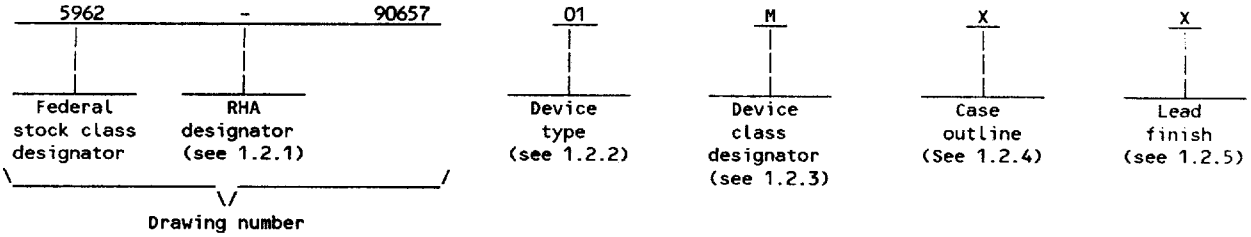
DESC FORM 193
JUL 91

5962-E156-93

1. SCOPE

1.1 Scope. This drawing forms a part of a one part - one part number documentation system (see 6.6 herein). Two product assurance classes consisting of military high reliability (device classes B, Q, and M) and space application (device classes S and V), and a choice of case outlines and lead finishes are available and are reflected in the Part or Identifying Number (PIN). Device class M microcircuits represent non-JAN class B microcircuits in accordance with 1.2.1 of MIL-STD-883, "Provisions for the use of MIL-STD-883 in conjunction with compliant non-JAN devices". When available, a choice of Radiation Hardness Assurance (RHA) levels are reflected in the PIN.

1.2 PIN. The PIN shall be as shown in the following example:



1.2.1 RHA designator. Device classes M, B, and S RHA marked devices shall meet the MIL-M-38510 specified RHA levels and shall be marked with the appropriate RHA designator. Device classes Q and V RHA marked devices shall meet the MIL-I-38535 specified RHA levels and shall be marked with the appropriate RHA designator. A dash (-) indicates a non-RHA device.

1.2.2 Device type(s). The device type(s) shall identify the circuit function as follows:

Device type	Generic number	Circuit function
01	16C30	Universal serial controller

1.2.3 Device class designator. The device class designator shall be a single letter identifying the product assurance level as follows:

Device class	Device requirements documentation
M	Vendor self-certification to the requirements for non-JAN class B microcircuits in accordance with 1.2.1 of MIL-STD-883
B or S	Certification and qualification to MIL-M-38510
Q or V	Certification and qualification to MIL-I-38535

1.2.4 Case outline(s). The case outline(s) shall be as designated in MIL-STD-1835 and as follows:

Outline letter	Descriptive designator	Terminals	Package style
X	CMGA3-P68	68	pin grid array

1.2.5 Lead finish. The lead finish shall be as specified in MIL-M-38510 for classes M, B, and S or MIL-I-38535 for classes Q and V. Finish letter "X" shall not be marked on the microcircuit or its packaging. The "X" designation is for use in specifications when lead finishes A, B, and C are considered acceptable and interchangeable without preference.

1.3 Absolute maximum ratings. 1/

Supply voltage range	-0.3 V dc to +7.0 V dc
Voltages on all pins with respect to V_{SS} (except V_{CC})	-0.3 V dc to V_{CC} + 0.3 V dc
Power dissipation (P_D)	350 mW
Lead temperature (soldering, 10 seconds)	+270°C
Thermal resistance, junction-to-case (Θ_{JC})	See MIL-STD-1835
Junction temperature (T_J)	+145°C
Storage temperature	-65°C to +150°C

1.4 Recommended operating conditions.

Ambient operating temperature range (T_A)	-55°C to +125°C
Supply voltage (V_{CC})	4.5 V dc to 5.5 V dc

1.5 Digital logic testing for device classes Q and V.

Fault coverage measurement of manufacturing logic tests (MIL-STD-883, test method 5012)	XX percent 2/

2. APPLICABLE DOCUMENTS

2.1 Government specifications, standards, bulletin, and handbook. Unless otherwise specified, the following specifications, standards, bulletin, and handbook of the issue listed in that issue of the Department of Defense Index of Specifications and Standards specified in the solicitation, form a part of this drawing to the extent specified herein.

SPECIFICATIONS

MILITARY

MIL-M-38510 - Microcircuits, General Specification for.
MIL-I-38535 - Integrated Circuits, Manufacturing, General Specification for.

STANDARDS

MILITARY

MIL-STD-480 - Configuration Control-Engineering Changes, Deviations and Waivers.
MIL-STD-883 - Test Methods and Procedures for Microelectronics.
MIL-STD-1835 - Microcircuit Case Outlines.

BULLETIN

MILITARY

MIL-BUL-103 - List of Standardized Military Drawings (SMD's).

HANDBOOK

MILITARY

MIL-HDBK-780 - Standardized Military Drawings.

(Copies of the specifications, standards, bulletin, and handbook required by manufacturers in connection with specific acquisition functions should be obtained from the contracting activity or as directed by the contracting activity.)

1/ Stresses above the absolute maximum rating may cause permanent damage to the device. Extended operation at the maximum levels may degrade performance and affect reliability.
2/ Values will be added when they become available.

2.2 Order of precedence. In the event of a conflict between the text of this drawing and the references cited herein, the text of this drawing shall take precedence.

3. REQUIREMENTS

3.1 Item requirements. The individual item requirements for device class M shall be in accordance with 1.2.1 of MIL-STD-883, "Provisions for the use of MIL-STD-883 in conjunction with compliant non-JAN devices" and as specified herein. The individual item requirements for device classes B and S shall be in accordance with MIL-M-38510 and as specified herein. For device classes B and S, a full electrical characterization table for each device type shall be included in this SMD. The individual item requirements for device classes Q and V shall be in accordance with MIL-I-38535, the device manufacturer's Quality Management (QM) plan, and as specified herein.

3.2 Design, construction, and physical dimensions. The design, construction, and physical dimensions shall be as specified in MIL-M-38510 for device classes M, B, and S and MIL-I-38535 for device classes Q and V and herein.

3.2.1 Case outline(s). The case outline(s) shall be in accordance with 1.2.4 herein.

3.2.2 Terminal connections. The terminal connections shall be as specified on figure 1.

3.2.3 Block diagram. The block diagram shall be as specified on figure 2.

3.3 Electrical performance characteristics and postirradiation parameter limits. Unless otherwise specified herein, the electrical performance characteristics and postirradiation parameter limits are as specified in table I and shall apply over the full ambient operating temperature range.

3.4 Electrical test requirements. The electrical test requirements shall be the subgroups specified in table II. The electrical tests for each subgroup are defined in table I.

3.5 Marking. The part shall be marked with the PIN listed in 1.2 herein. Marking for device class M shall be in accordance with MIL-STD-883 (see 3.1 herein). In addition, the manufacturer's PIN may also be marked as listed in MIL-BUL-103. Marking for device classes B and S shall be in accordance with MIL-M-38510. Marking for device classes Q and V shall be in accordance with MIL-I-38535.

3.5.1 Certification/compliance mark. The compliance mark for device class M shall be a "C" as required in MIL-STD-883 (see 3.1 herein). The certification mark for device classes B and S shall be a "J" or "JAN" as required in MIL-M-38510. The certification mark for device classes Q and V shall be a "QML" as required in MIL-I-38535.

3.6 Certificate of compliance. For device class M, a certificate of compliance shall be required from a manufacturer in order to be listed as an approved source of supply in MIL-BUL-103 (see 6.7.3 herein). For device classes Q and V, a certificate of compliance shall be required from a QML-38535 listed manufacturer in order to supply to the requirements of this drawing (see 6.7.2 herein). The certificate of compliance submitted to DESC-EC prior to listing as an approved source of supply for this drawing shall affirm that the manufacturer's product meets, for device class M, the requirements of MIL-STD-883 (see 3.1 herein), or for device classes Q and V, the requirements of MIL-I-38535 and the requirements herein.

3.7 Certificate of conformance. A certificate of conformance as required for device class M in MIL-STD-883 (see 3.1 herein) or device classes B and S in MIL-M-38510 or for device classes Q and V in MIL-I-38535 shall be provided with each lot of microcircuits delivered to this drawing.

3.8 Notification of change for device class M. For device class M, notification to DESC-EC of change of product (see 6.2 herein) involving devices acquired to this drawing is required for any change as defined in MIL-STD-480.

3.9 Verification and review for device class M. For device class M, DESC, DESC's agent, and the acquiring activity retain the option to review the manufacturer's facility and applicable required documentation. Offshore documentation shall be made available onshore at the option of the reviewer.

3.10 Microcircuit group assignment for device classes M, B, and S. Device classes M, B, and S devices covered by this drawing shall be in microcircuit group number 105 (see MIL-M-38510, appendix E).

3.11 Serialization for device class S. All device class S devices shall be serialized in accordance with MIL-M-38510.

TABLE I. Electrical performance characteristics.

Test	Symbol	Conditions $-55°C \le T_A \le +125°C$ unless otherwise specified 1/	Group A subgroups	Device type	Limits		Unit
					Min	Max	
Input high voltage	V_{IH}		1, 2, 3	01	2.2	V_{CC}+0.3	V
Input low voltage	V_{IL}		1, 2, 3	01	-0.3	0.8	V
Output high voltage	V_{OH1}	I_{OH} = -1.6 mA, V_{CC} = 4.5 V	1, 2, 3	01	2.4		V
Output high voltage	V_{OH2}	I_{OH} = -250 µA, V_{CC} = 4.5 V	1, 2, 3	01	V_{CC} -0.8		V
Output low voltage	V_{OL}	I_{OL} = +2.0 mA, V_{CC} = 4.5 V	1, 2, 3	01		0.4	V
Input leakage	I_{IL}	0.4 V < V_{IN} < +2.4 V V_{CC} = 5.5 V	1, 2, 3	01		10	µA
Output leakage	I_{OL}	0.4 V < V_{OUT} < +2.4 V V_{CC} = 5.5 V	1, 2, 3	01		10	µA
V_{CC} supply current	I_{CCI}	V_{CC} = 5.0 V, V_{IH} = 4.8 V V_{IL} = -0.2 V	1, 2, 3	01		50	mA
Input capacitance	C_{IN}	See 4.4.1.c	4	01		10	pf
Output capacitance	C_{OUT}	See 4.4.1.c	4	01		15	pf
Bidirectional capacitance	$C_{I/O}$	See 4.4.1.c	4	01		20	pf
Functional testing		See 4.4.1.b	7,8	01			
Bus cycle time	1	V_{CC} = 4.5 V See figure 3	9, 10, 11	01	160		ns

See footnotes at end of table.

TABLE I. Electrical performance characteristics - Continued.

Test	Symbol	Conditions $-55°C \le T_A \le +125°C$ unless otherwise specified 1/	Group A subgroups	Device type	Limits		Unit
					Min	Max	
/AS low width	2	V_{CC} = 4.5 V See figure 3	9, 10, 11	01	40		ns
/AS high width	3				90		
/DS low width	4				70		
/DS high width	5				60		
/AS↑ to /DS↓ delay time	6				5		
/DS↑ to /AS↓ delay time	7				5		
/DS↓ to data active delay	8				0		
/DS↓ to data valid delay	9					85	
/DS↑ to data not valid delay	10				0		
/DS↑ to data float delay	11					20	
/CS to /AS↓ setup time	12				15		
/CS to /AS↓ hold time	13				0		
Direct address to /AS↓ setup time 2/	14				15		
Direct address to /AS↓ hold time 2/	15				5		
/SITACK to /AS↓ setup time	16				15		
/SITACK to /AS↓ hold time	17				5		
Address to /AS↓ setup time	18				15		

See footnotes at end of table.

TABLE I. Electrical performance characteristics - Continued.

Test	Symbol	Conditions $-55°C \le T_A \le +125°C$ unless otherwise specified 1/	Group A subgroups	Device type	Limits		Unit
					Min	Max	
Address to /AS↓ hold time	19	V_{CC} = 4.5 V See figure 3	9, 10, 11	01	5		ns
R/$\overline{W}$ to /DS↓ setup time	20				0		
R/$\overline{W}$ to /DS↓ hold time	21				25		
/DS↓ to /RxREQ inactive delay 3/	22					60	
/DS↓ to /RxREQ active delay	23				0		
Write data to /DS↓ setup time	24				30		
Write data to /DS↓ hold time	25				0		
/DS↓ to /TxREQ inactive delay 4/	26					70	
/DS↓ to /TxREQ active delay	27				0		
/RD low width	28				70		
/RD high width	29				60		
/AS↓ to /RD↓ delay time	30				5		
/RD↑ to /AS↓ delay time	31				5		
/RD↓ to data active delay	32				0		
/RD↓ to data valid delay	33					85	
/RD↑ to data non valid delay	34				0		
/RD↑ to data float delay	35					20	

See footnotes at end of table.

TABLE I. Electrical performance characteristics - Continued.

Test	Symbol	Conditions $-55°C \le T_A \le +125°C$ unless otherwise specified 1/	Group A subgroups	Device type	Limits		Unit
					Min	Max	
/RD↓ to /RxREQ inactive delay 3/	36	V_{CC} = 4.5 V See figure 3	9, 10, 11	01		60	ns
/RD↓ to /RxREQ active delay	37				0		
/WR low width	38				70		
/WR high width	39				60		
/AS↓ to /WR↓ delay time	40				5		
/WR↑ to /AS↓ delay time	41				5		
Write data to /WR↑ setup time	42				30		
Write data to /WR↑ hold time	43				0		
/WR↑ to /TxREQ inactive delay 4/	44					70	
/WR↑ to /TxREQ active delay	45				0		
/CS to /DS↓ setup time 5/	46				0		
/CS to /DS↓ hold time 5/	47				25		
Direct address to /DS↓ setup time 2/, 5/	48				5		
Direct address to /DS↓ hold time 2/, 5/	49				25		
/SITACK to /DS↓ setup time 5/	50				5		
/SITACK to /DS↓ hold time 5/	51				25		
/CS to /RD↓ setup time 5/	52				0		

See footnotes at end of table.

TABLE I. Electrical performance characteristics - Continued.

Test	Symbol	Conditions $-55°C \le T_A \le +125°C$ unless otherwise specified 1/	Group A subgroups	Device type	Limits		Unit
					Min	Max	
/CS to /RD↓ hold time 5/	53	V_{CC} = 4.5 V See figure 3	9, 10, 11	01	25		ns
Direct address to /RD↓ setup time 2/, 5/	54				5		
Direct address to /RD↓ hold time 2/, 5/	55				25		
/SITACK to /RD↓ setup time 5/	56				5		
/SITACK to /RD↓ hold time 5/	57				25		
/CS to /WR↓ setup time 5/	58				0		
/CS to /WR↓ hold time 5/	59				25		
Direct address to /WR↓ setup time 2/, 5/	60				5		
Direct address to /WR↓ hold time 2/, 5/	61				25		
/SITACK to /WR↓ setup time 5/	62				5		
/SITACK to /WR↓ hold time 5/	63				25		
/RxACK low width 5/	64				70		
/RxACK high width	65				60		
/RxACK↓ to data active delay	66				0		
/RxACK↓ to data valid delay	67					85	
/RxACK↑ to data not valid delay	68				0		
/RxACK↑ to data float delay	69					20	

See footnotes at end of table.

TABLE I. Electrical performance characteristics - Continued.

Test	Symbol	Conditions $-55°C \le T_A \le +125°C$ unless otherwise specified 1/	Group A subgroups	Device type	Limits		Unit
					Min	Max	
/RxACK↓ to /RxREQ inactive delay 3/	70	V_{CC} = 4.5 V See figure 3	9, 10, 11	01		60	ns
/RxACK↑ to /RxREQ active delay	71				0		
/TxACK low width	72				70		
/TxACK high width	73				60		
Write data to /TxACK↓ setup time	74				30		
Write data to /TxACK↓ hold time	75				0		
/TxACK↑ to /TxREQ inactive delay 4/	76					60	
TxACK↑ to /TxREQ active delay	77				0		
/DS↓ (intack) to /READY↓ delay	78					200	
/READY↑ to data valid delay	79					40	
/D↓ to /READY↑ delay	80					40	
IEI to /DS↓ (intack) setup time	81				60		
IEI to /DS↓ (intack) hold time	82				0		
IEI to IEO delay	83					60	
/AS↓ (intack) to IEO delay	84					60	
/DS↓ (intack) to /INT inactive delay	85					200	
/DS↓ (intack) to /WAIT↓ delay	86					40	

See footnotes at end of table.

TABLE I. Electrical performance characteristics - Continued.

Test	Symbol	Conditions $-55°C \le T_A \le +125°C$ unless otherwise specified 1/	Group A subgroups	Device type	Limits		Unit
					Min	Max	
/DS↓ (intack) to /WAIT↓ delay	87	V_{CC} = 4.5 V See figure 3	9, 10, 11	01		200	ns
/WAIT↑ to data valid delay	88					40	
/RD↓ (intack) to /READY↑ delay	89					200	
/RD↑ to /READY↑ delay	90					40	
IEI to /RD↓ (intack) setup time	91				60		
IEI to /RD↓ (intack) hold time	92				0		
/RD↓ (intack) to /INT inactive delay	93					200	
/RD↓ (intack) to /WAIT↑ delay	94					40	
/RD↓ (intack) to /WAIT↑ delay	95					200	
/PITACK low width	96				70		
/PITACK high width	97				60		
/AS↓ to /PITACK↓ delay time	98				5		
/PITACK↑ to /AS↓ delay time	99				5		
/PITACK↓ to data active delay	100				0		
/PITACK↑ to data not valid delay	101				0		
/PITACK↑ to data float delay	102					20	
IEI to /PITACK↓ setup time	103				60		

See footnotes at end of table.

TABLE I. Electrical performance characteristics - Continued.

Test	Symbol	Conditions $-55°C \le T_A \le +125°C$ unless otherwise specified 1/	Group A subgroups	Device type	Limits		Unit
					Min	Max	
IEI to /PITACK↓ hold time	104	V_{CC} = 4.5 V See figure 3	9, 10, 11	01	0		ns
/PITACK↓ to IEO delay	105					60	
/PITACK↓ to /INT inactive delay	106					200	
/PITACK↓ to /READY↓ delay	107					200	
/PITACK↓ to /READY↑ delay	108					40	
/PITACK↓ to /WAIT↓ delay	109					40	
/PITACK↓ to /WAIT↑ delay	110					200	
/SITACK↓ to IEO inactive delay 5/	111					200	
/Strobe high width 6/	112				60		
/Reset low width	113				170		
/Reset high width	114				60		
/Reset↓ to /Strobe↓ 6/	115				60		
/DS↓ to /READY↑ delay	116					50	
/WR↓ to /READY↓ delay	117					50	
/WR↓ to /READY↑ delay	118					40	
/RD↓ to /READY↓ delay	119					50	
/RxACK↓ to /READY↓ delay	120					50	

See footnotes at end of table.

TABLE I. Electrical performance characteristics - Continued.

Test	Symbol	Conditions $-55°C \le T_A \le +125°C$ unless otherwise specified 1/	Group A subgroups	Device type	Limits		Unit
					Min	Max	
/RxACK↑ to /READY↑ delay	121	V_{CC} = 4.5 V See figure 3	9, 10, 11	01		40	ns
/TxACK↑ to /READY↑ delay	122					50	
TxACK↑ to /READY↑ delay	123					40	

1/ All testing to be performed at worst-case test conditions unless otherwise specified.
2/ Direct address is any of A//B, D//C or AD15-AD8 used as an address bus.
3/ Parameter applies only if read empties the receive FIFO.
4/ Parameter applies only if write fills the transmit FIFO.
5/ The parameter applies only when /AS is not present.
6/ Strobe is any of /DS, /RD, /WR, /PITACK, /RxACK or /TxACK.

Case X

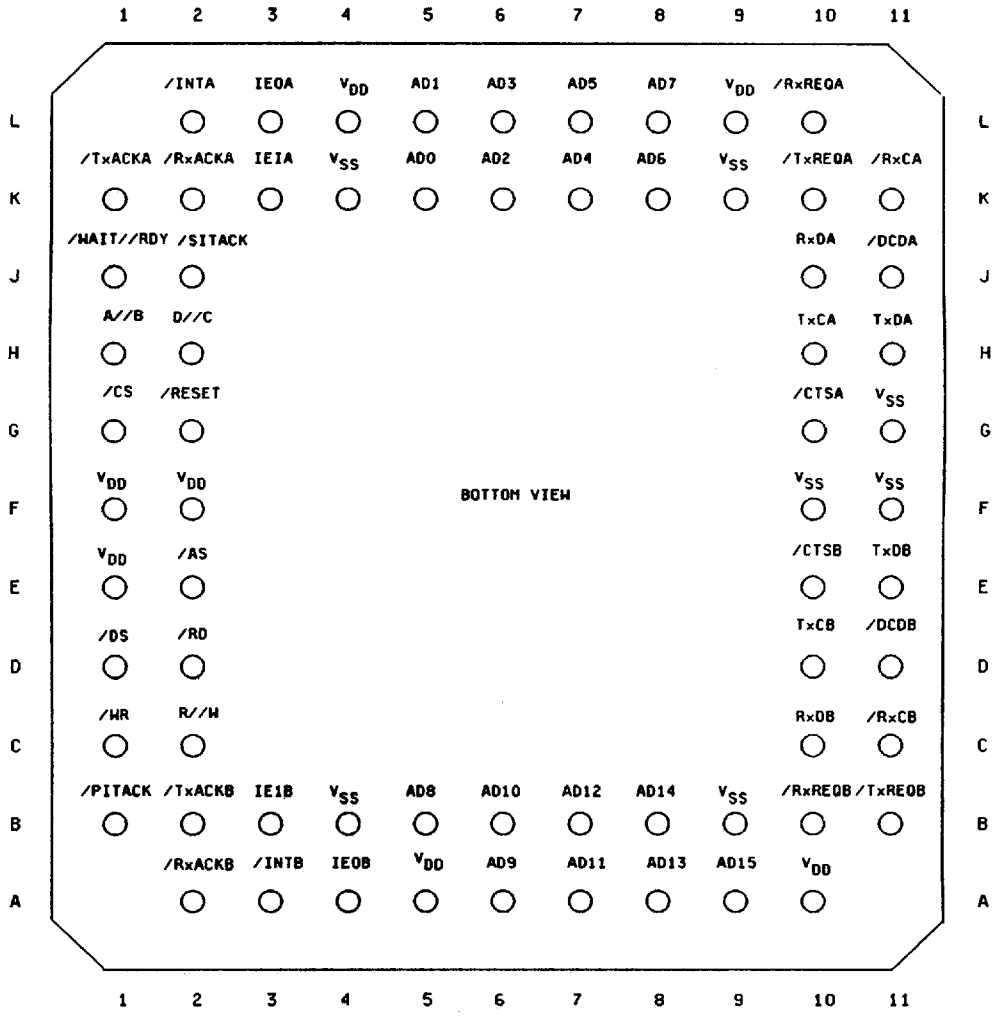


FIGURE 1. Terminal connections.

STANDARDIZED MILITARY DRAWING DEFENSE ELECTRONICS SUPPLY CENTER DAYTON, OHIO 45444	SIZE A		5962-90657
		REVISION LEVEL	SHEET 14

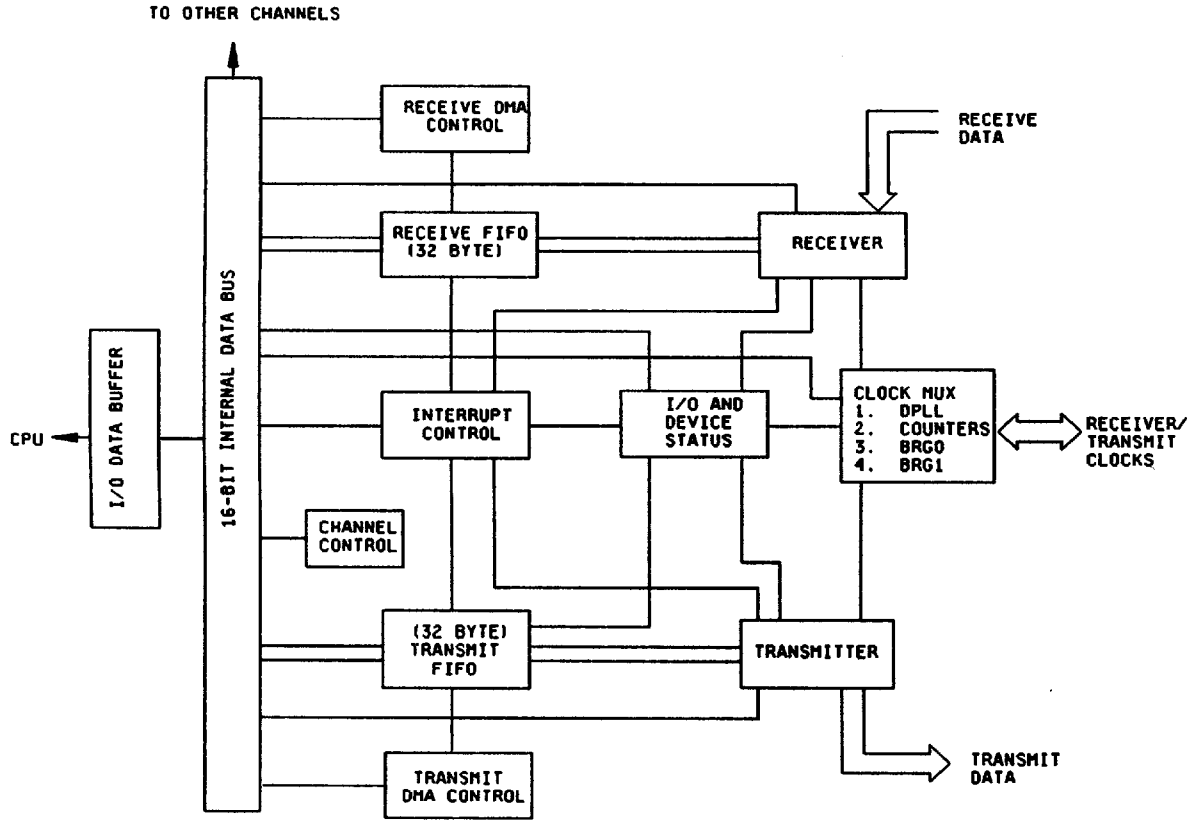
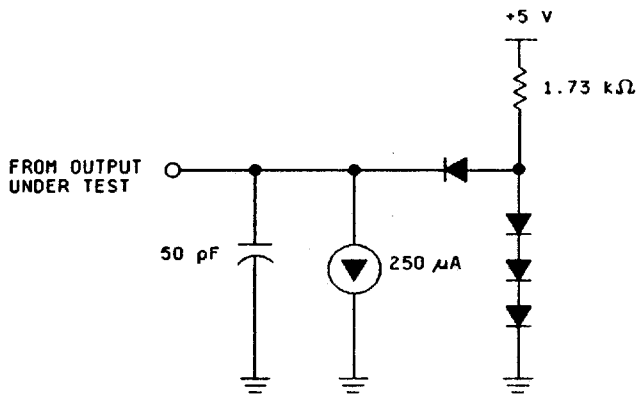
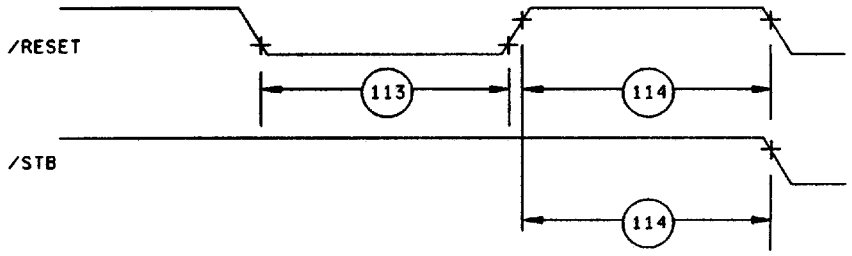


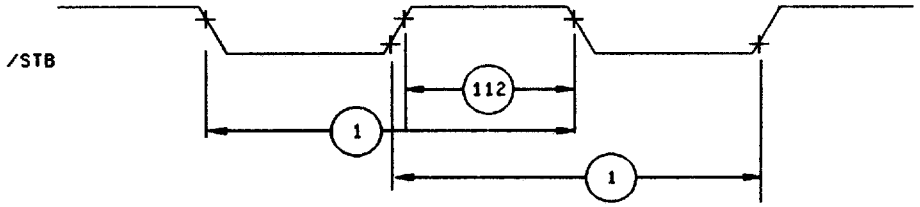
FIGURE 2. Block diagram.



Standard test load

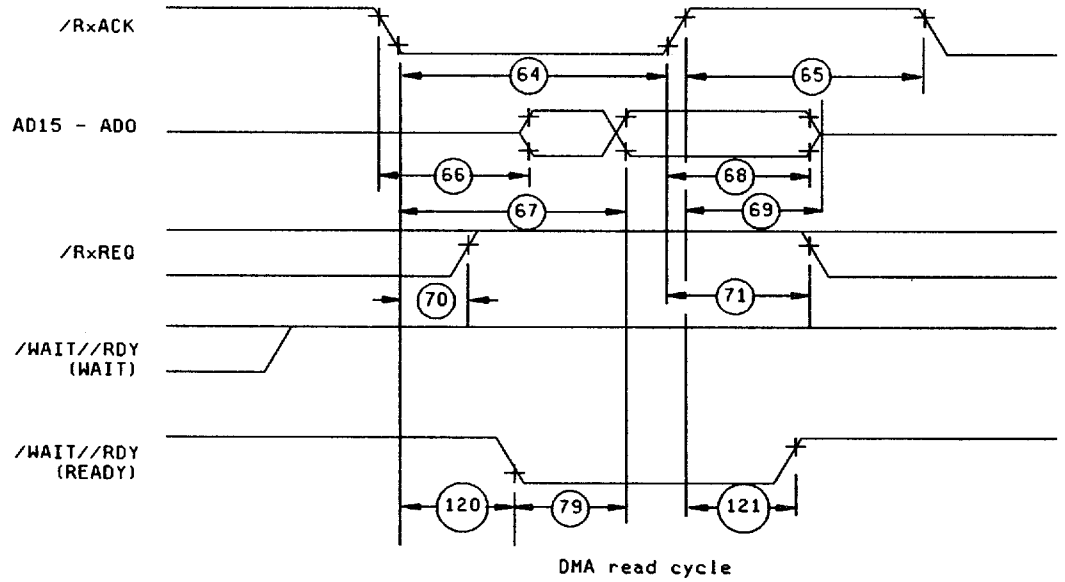


Reset timing

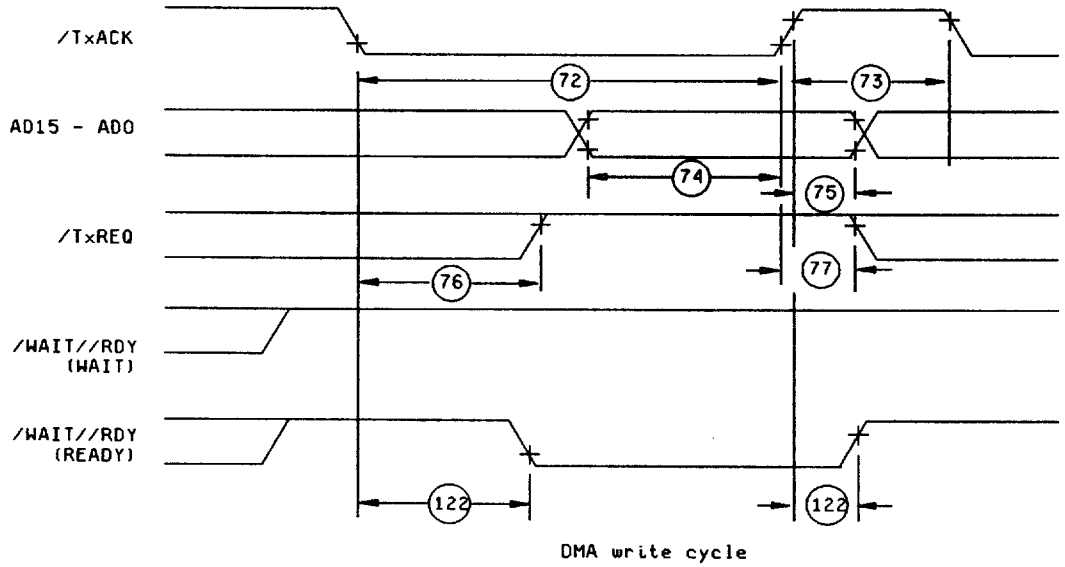


Bus cycle timing

FIGURE 3. Timing waveforms.

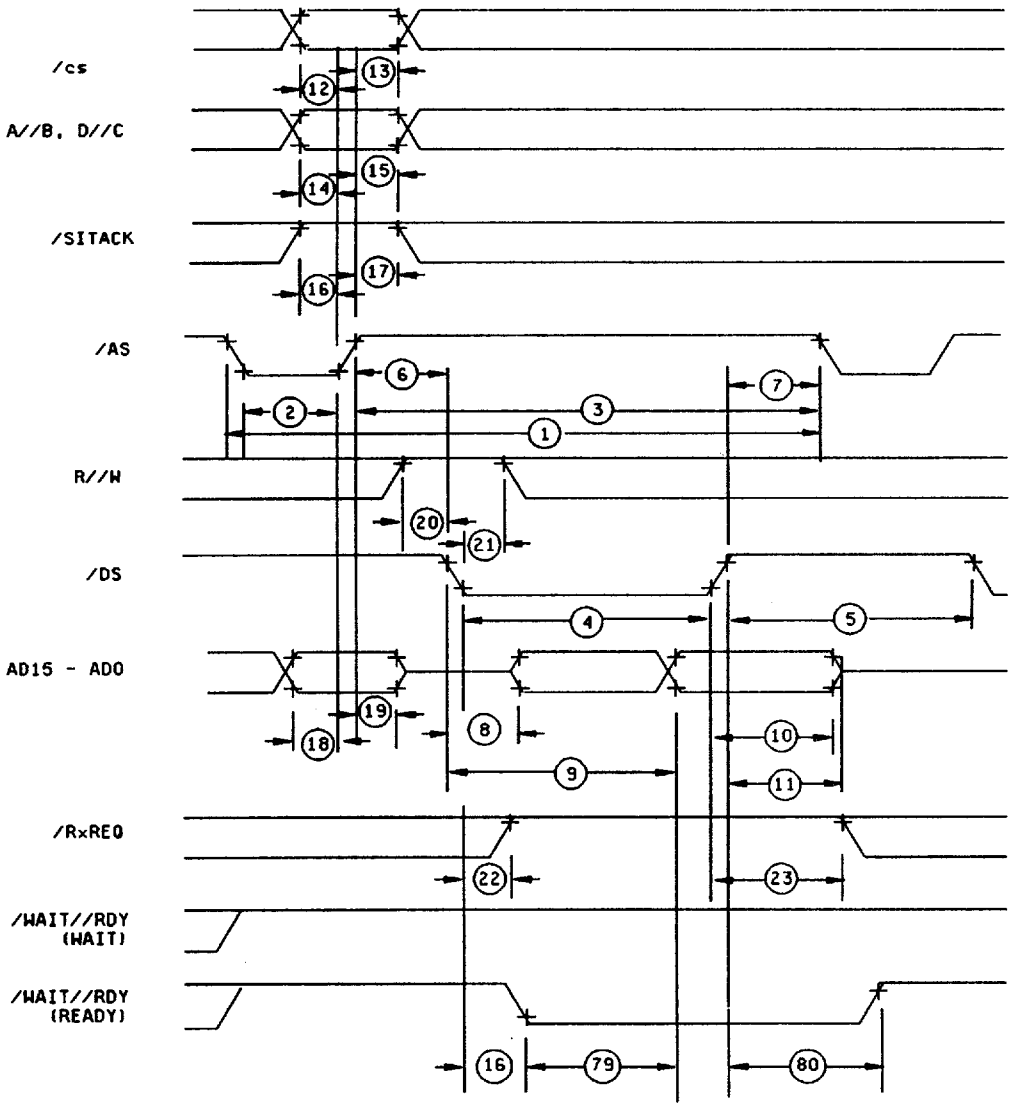


DMA read cycle



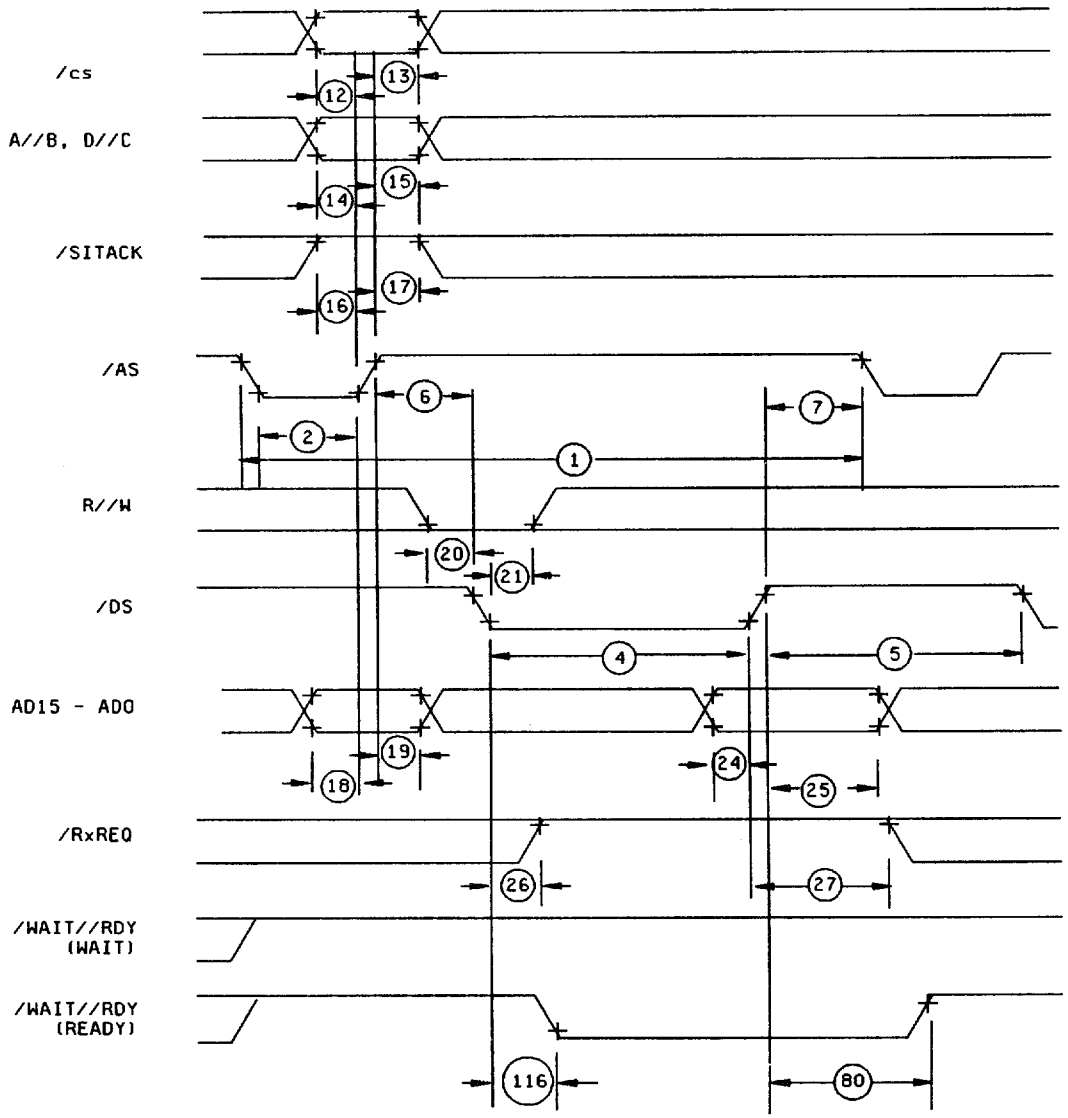
DMA write cycle

FIGURE 3. Timing waveforms - Continued.



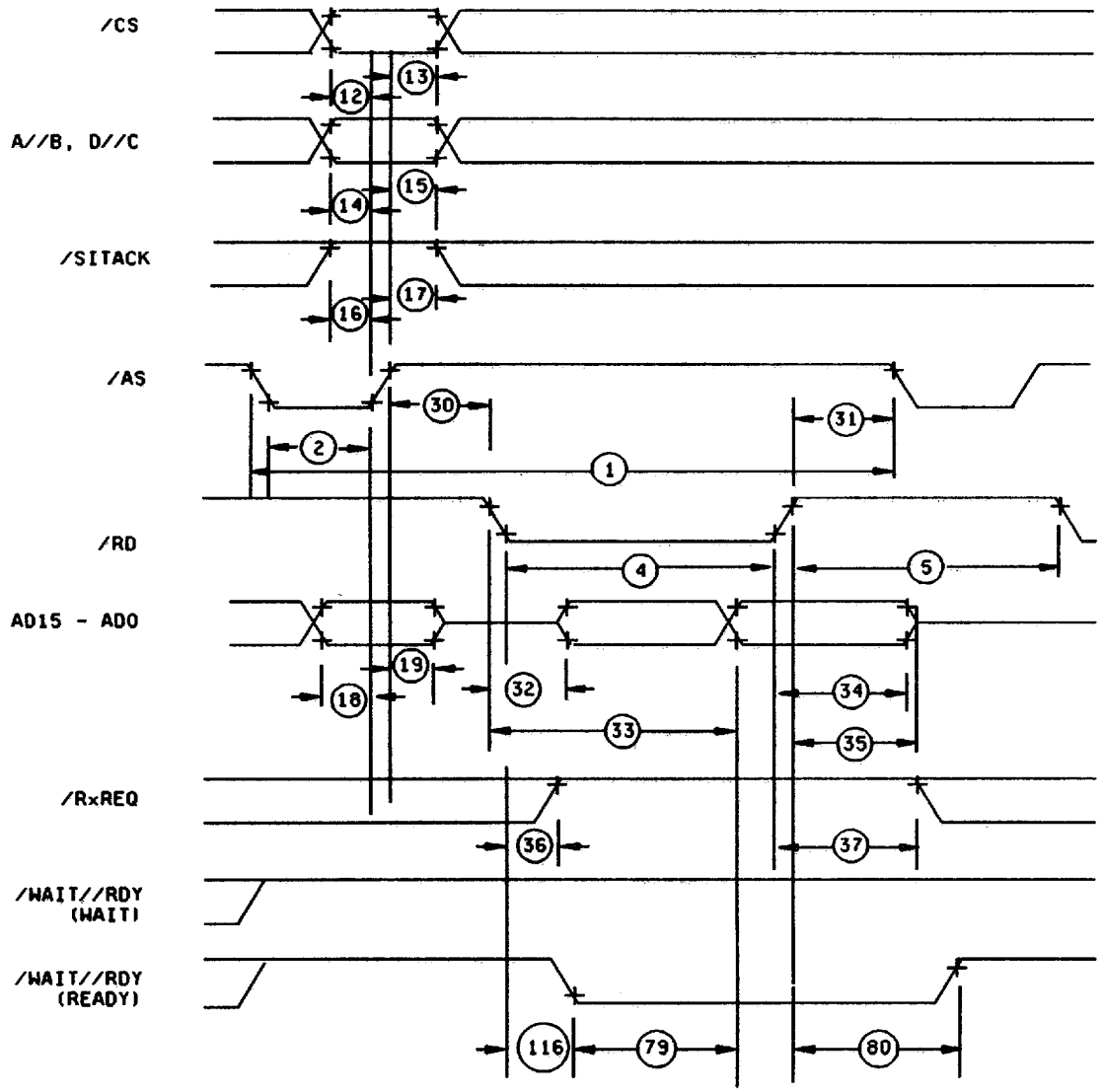
Multiplexed/DS read cycle

FIGURE 3. Timing waveforms - Continued.



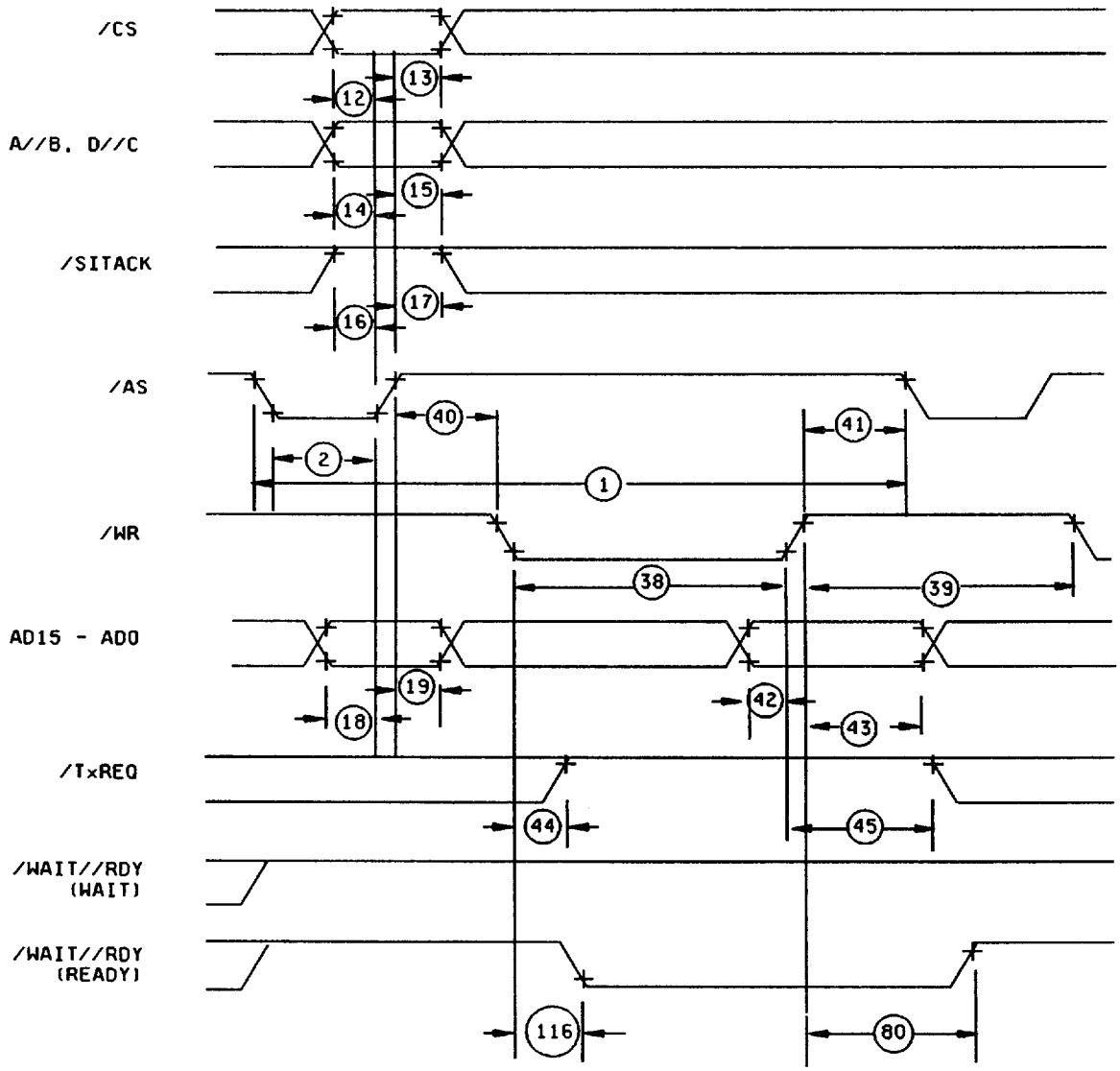
Multiplexed/DS write cycle

FIGURE 3. Timing waveforms - Continued.



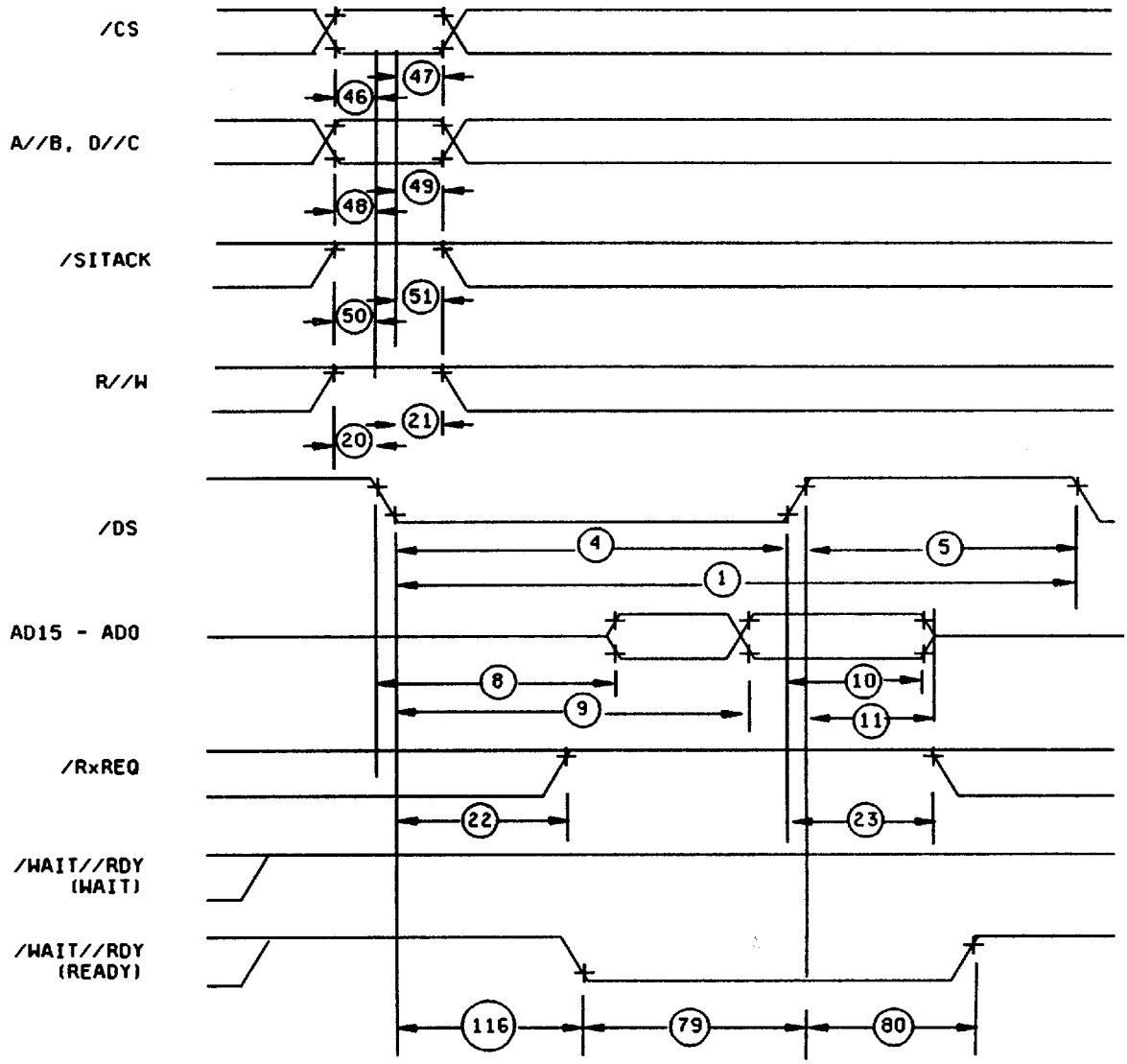
Multiplexed/RD read cycle

FIGURE 3. Timing waveforms - Continued.



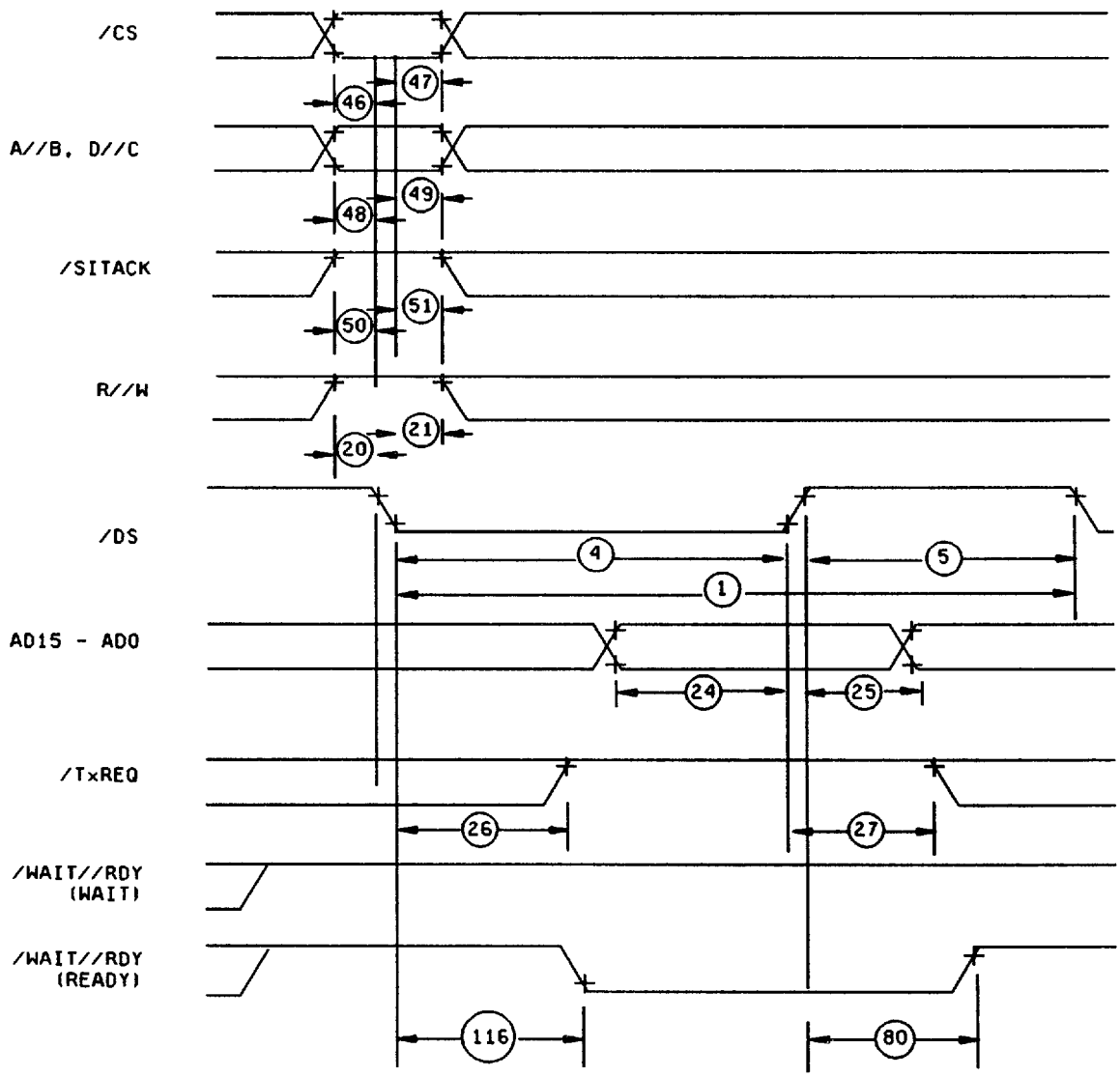
Multiplexed/WR write cycle

FIGURE 3. Timing waveforms - Continued.



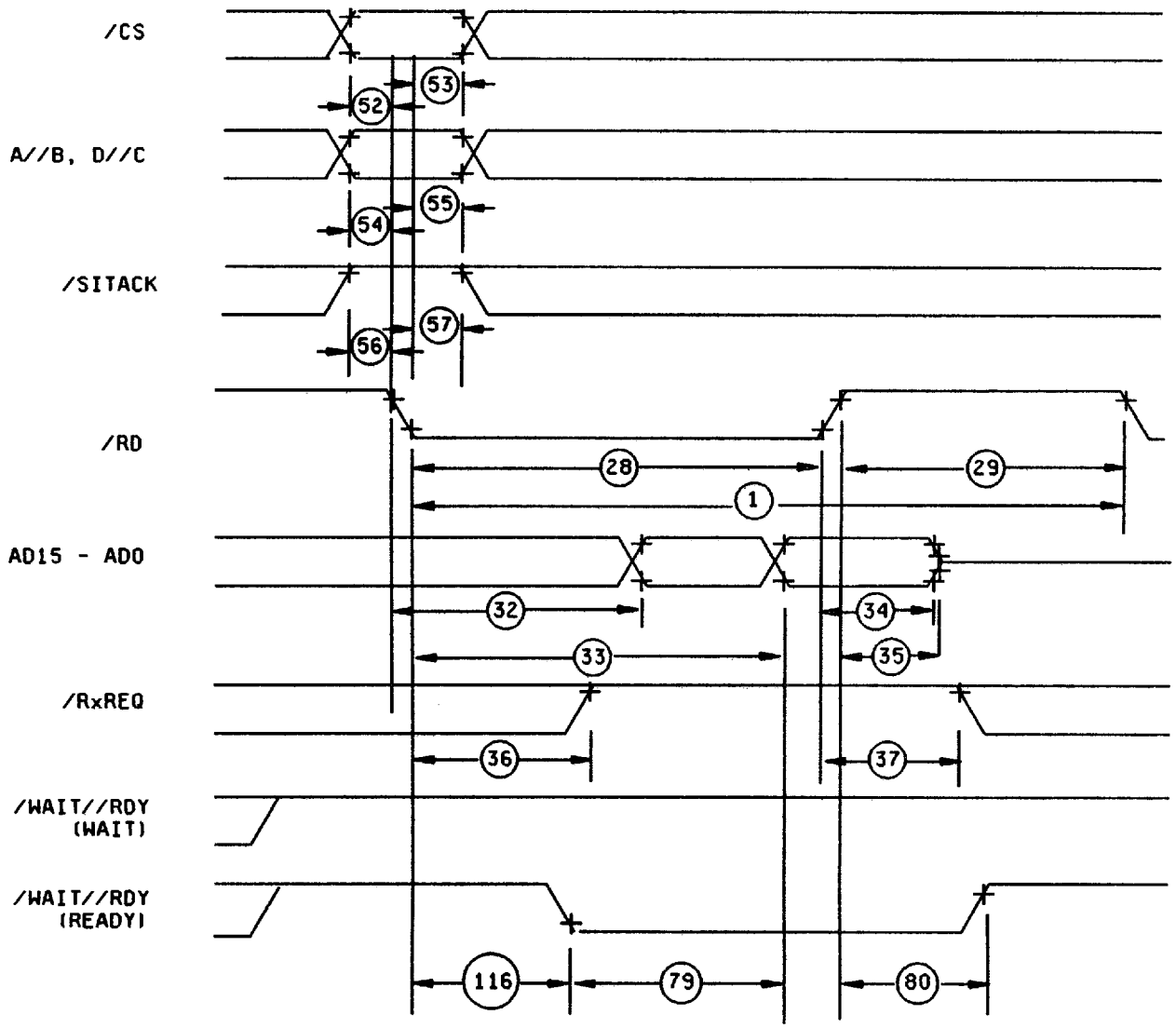
Non-multiplexed/DS read cycle

FIGURE 3. Timing waveforms - Continued.



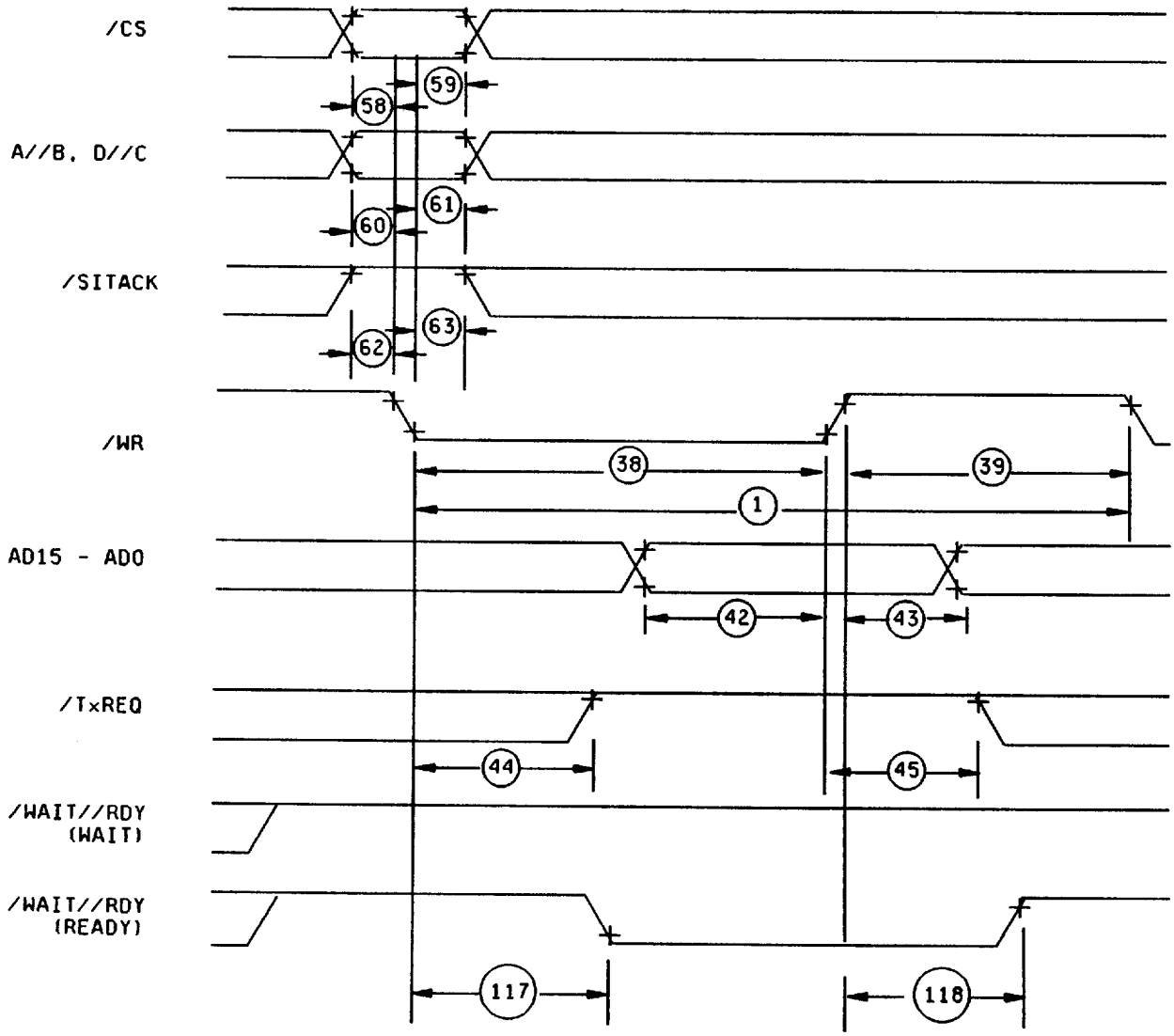
Non-multiplexed/DS write cycle

FIGURE 3. Timing waveforms - Continued.



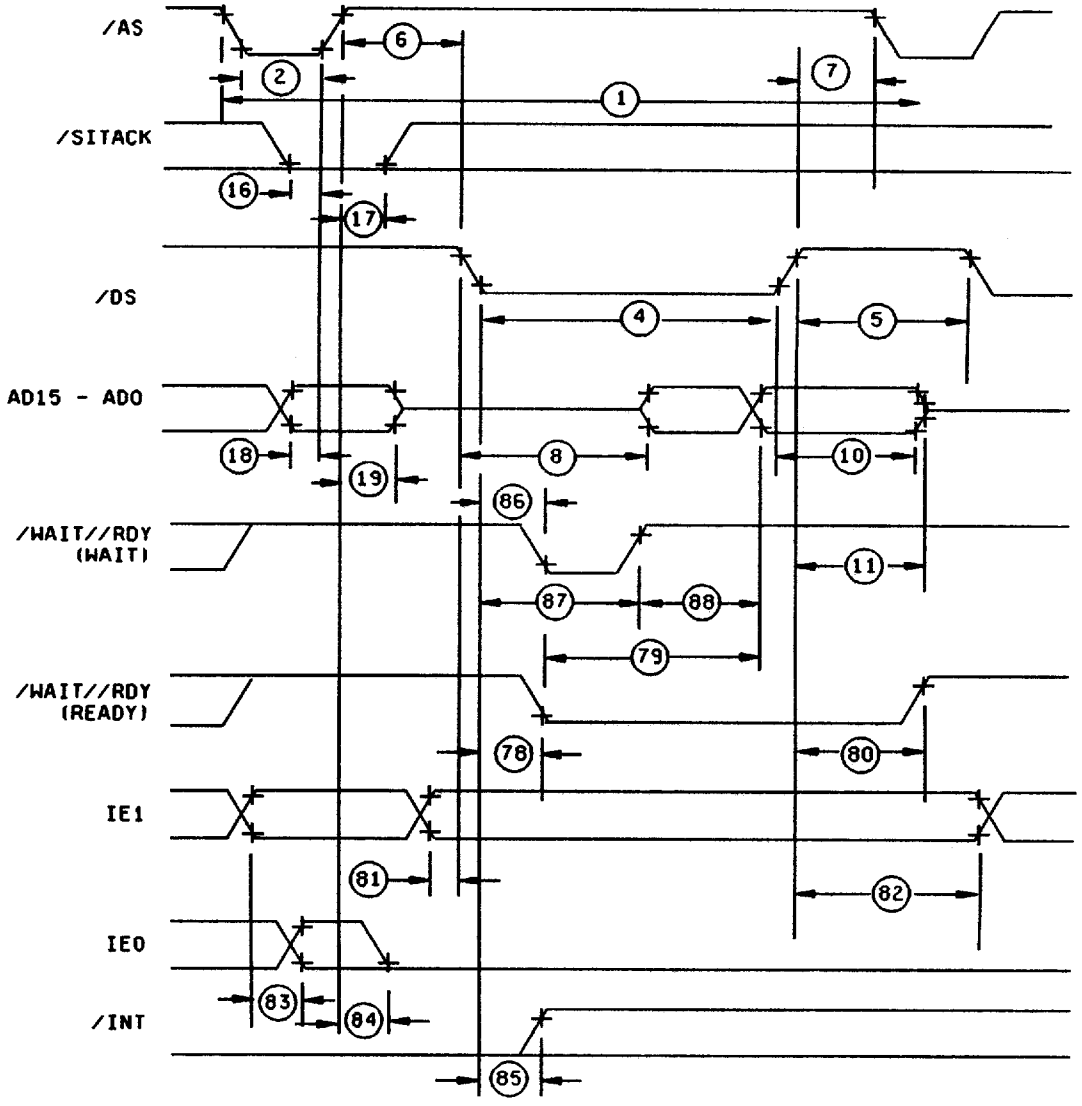
Non-multiplexed/RD read cycle

FIGURE 3. Timing waveforms - Continued.



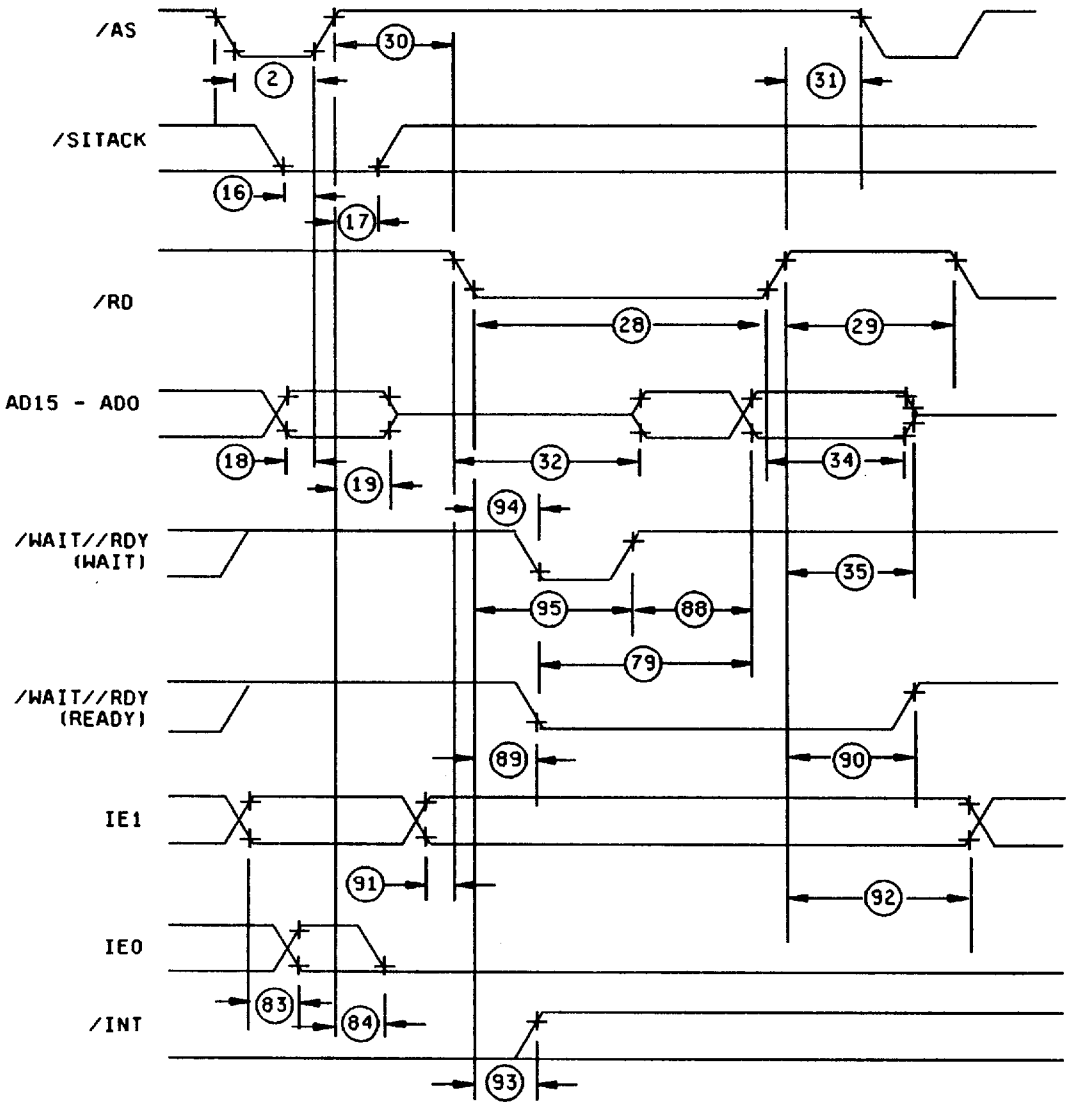
Non-multiplexed/WR write cycle

FIGURE 3. Timing waveforms - Continued.



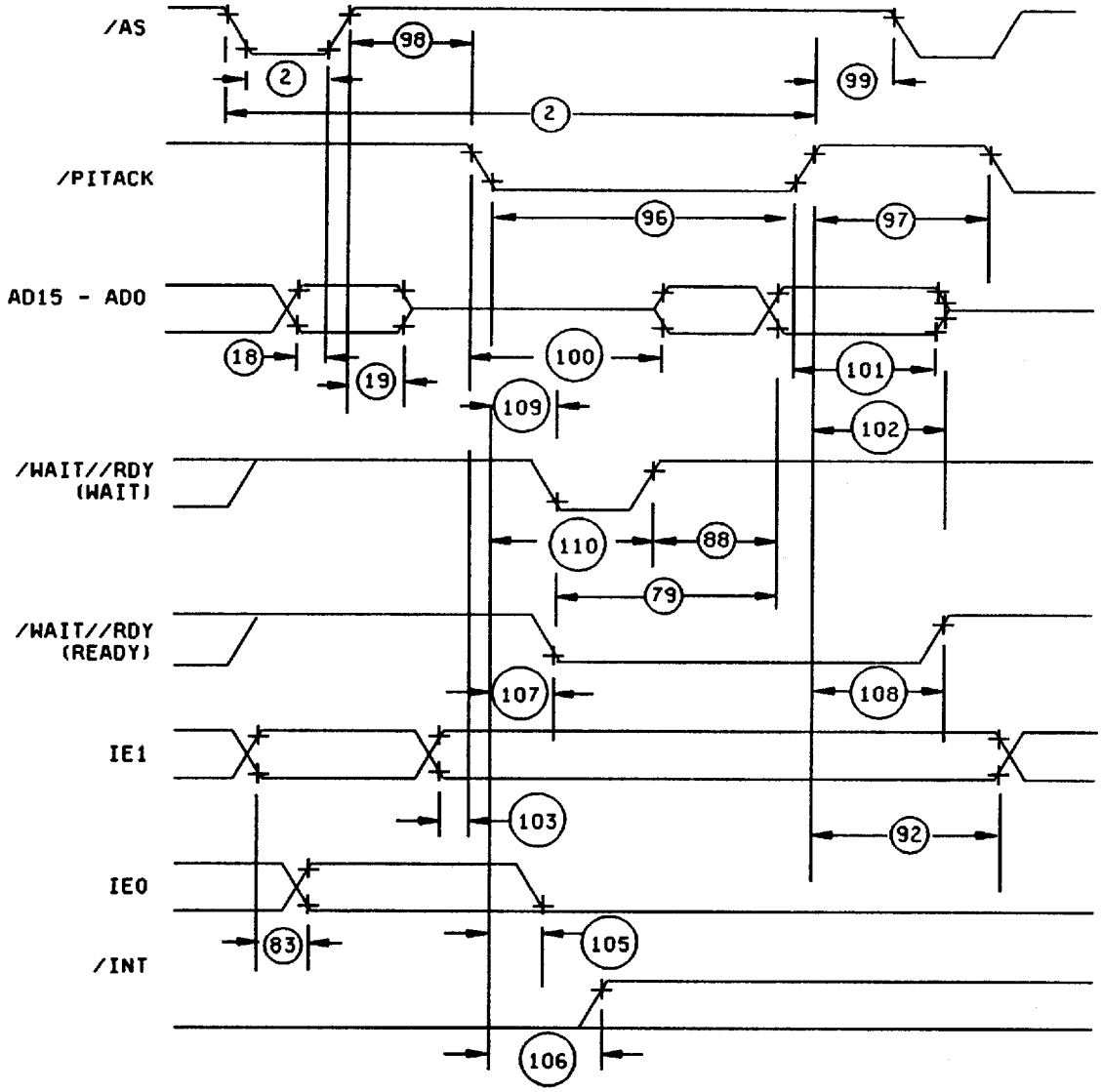
Multiplexed/DS interrupt acknowledge cycle

FIGURE 3. Timing waveforms - Continued.



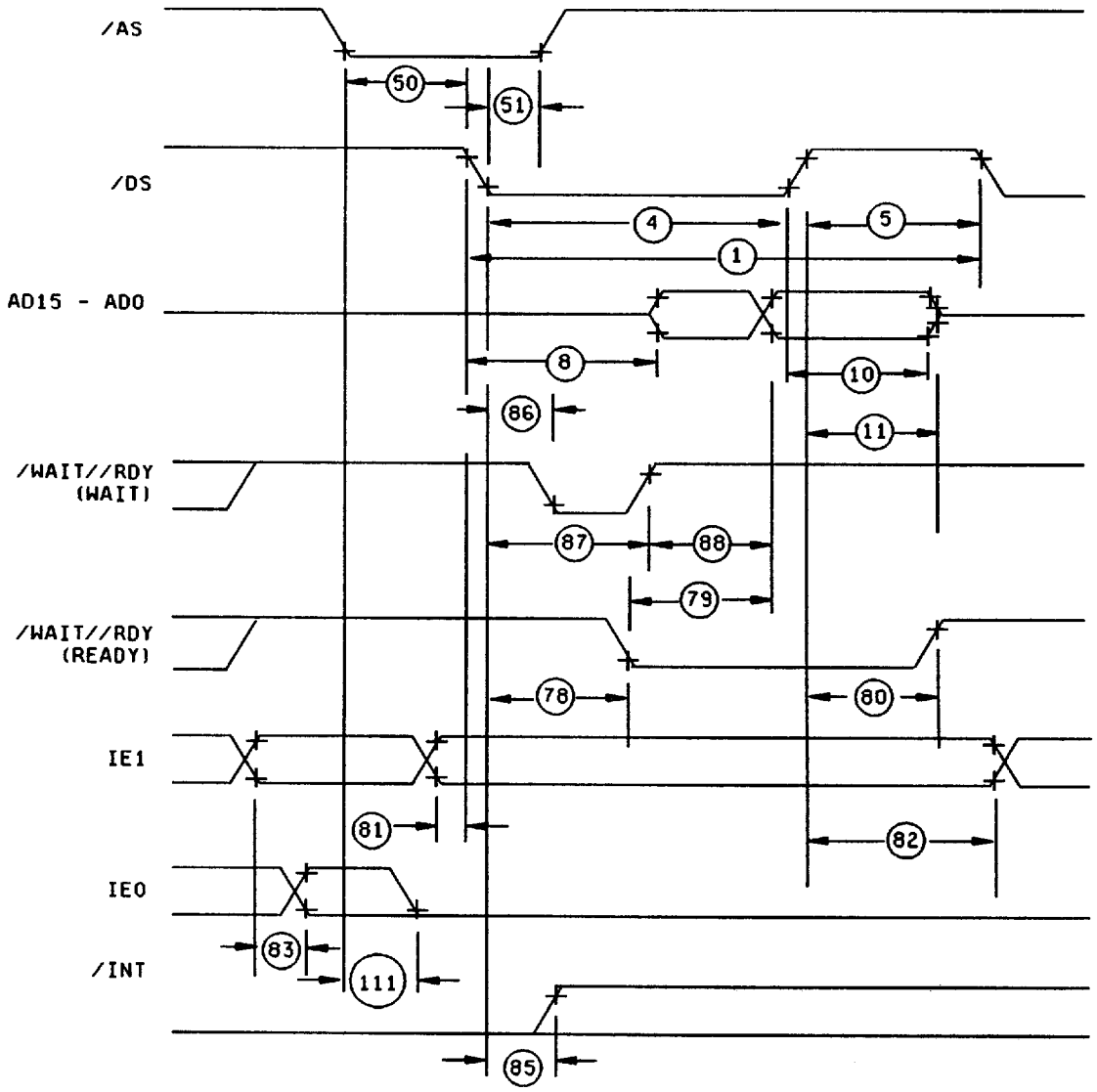
Multiplexed/rd interrupt acknowledge cycle

FIGURE 3. Timing waveforms - Continued.



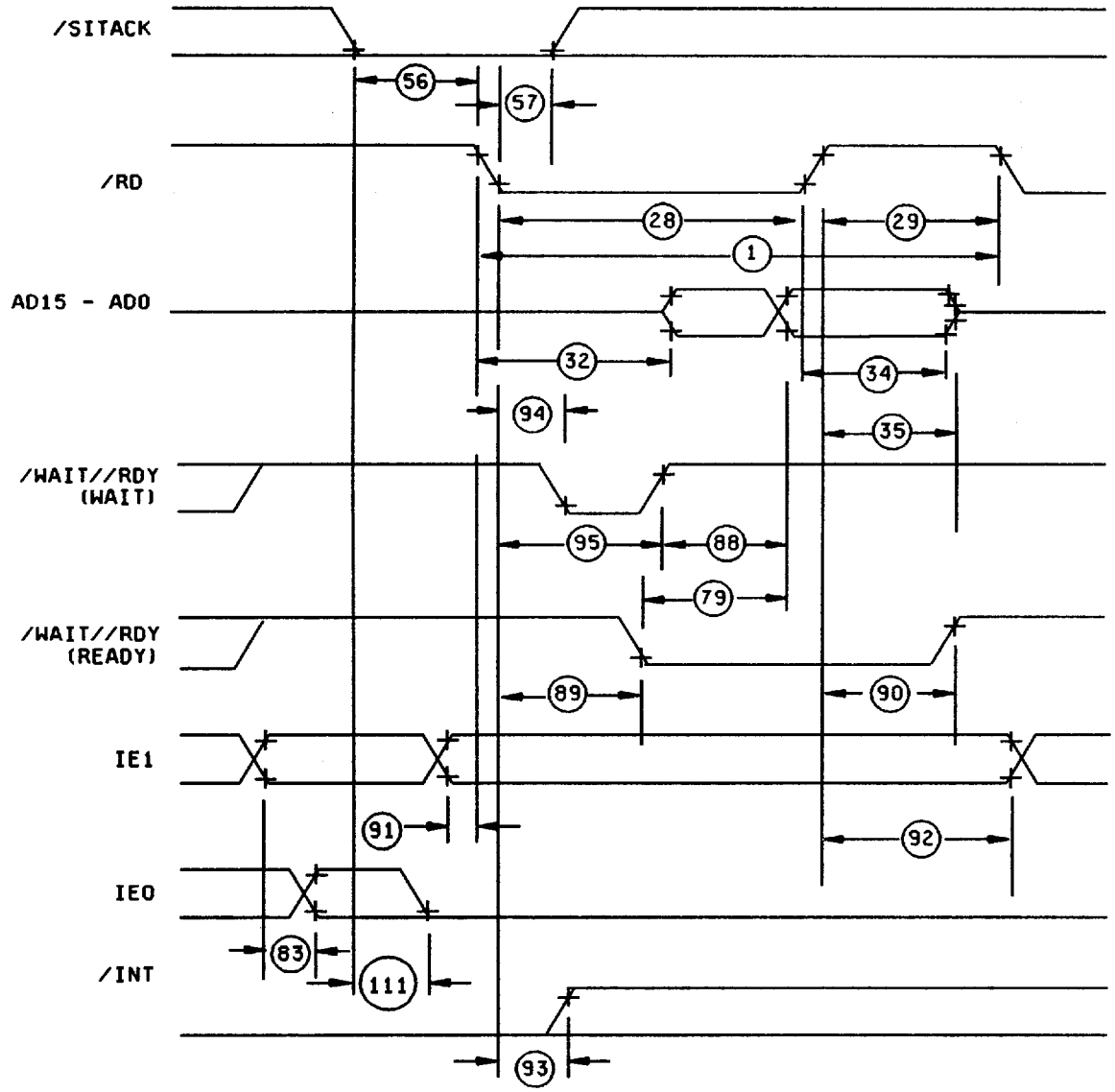
Multiplexed pulsed interrupt acknowledge cycle

FIGURE 3. Timing waveforms - Continued.



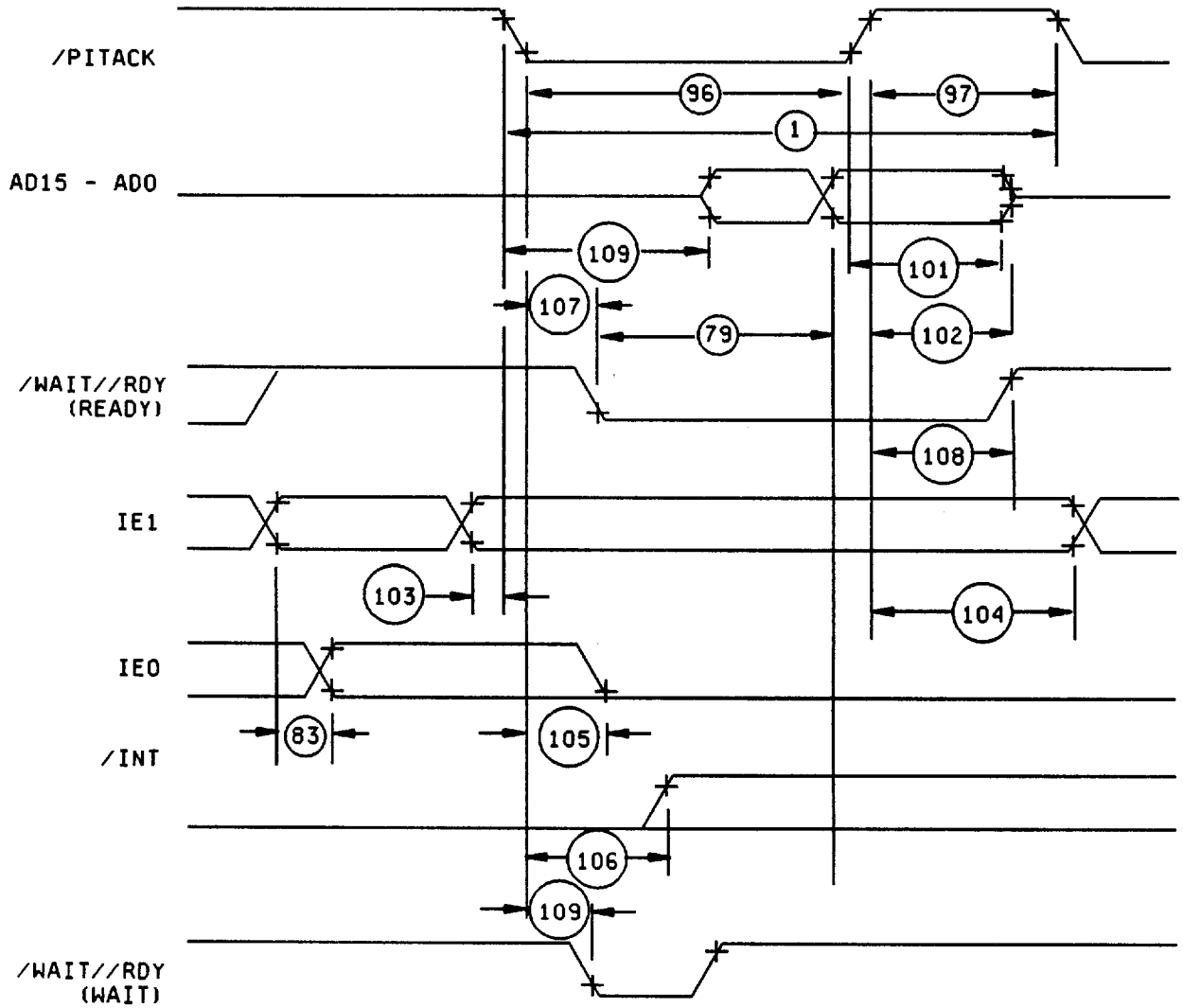
Non-MUX/DS interrupt acknowledge cycle

FIGURE 3. Timing waveforms - Continued.



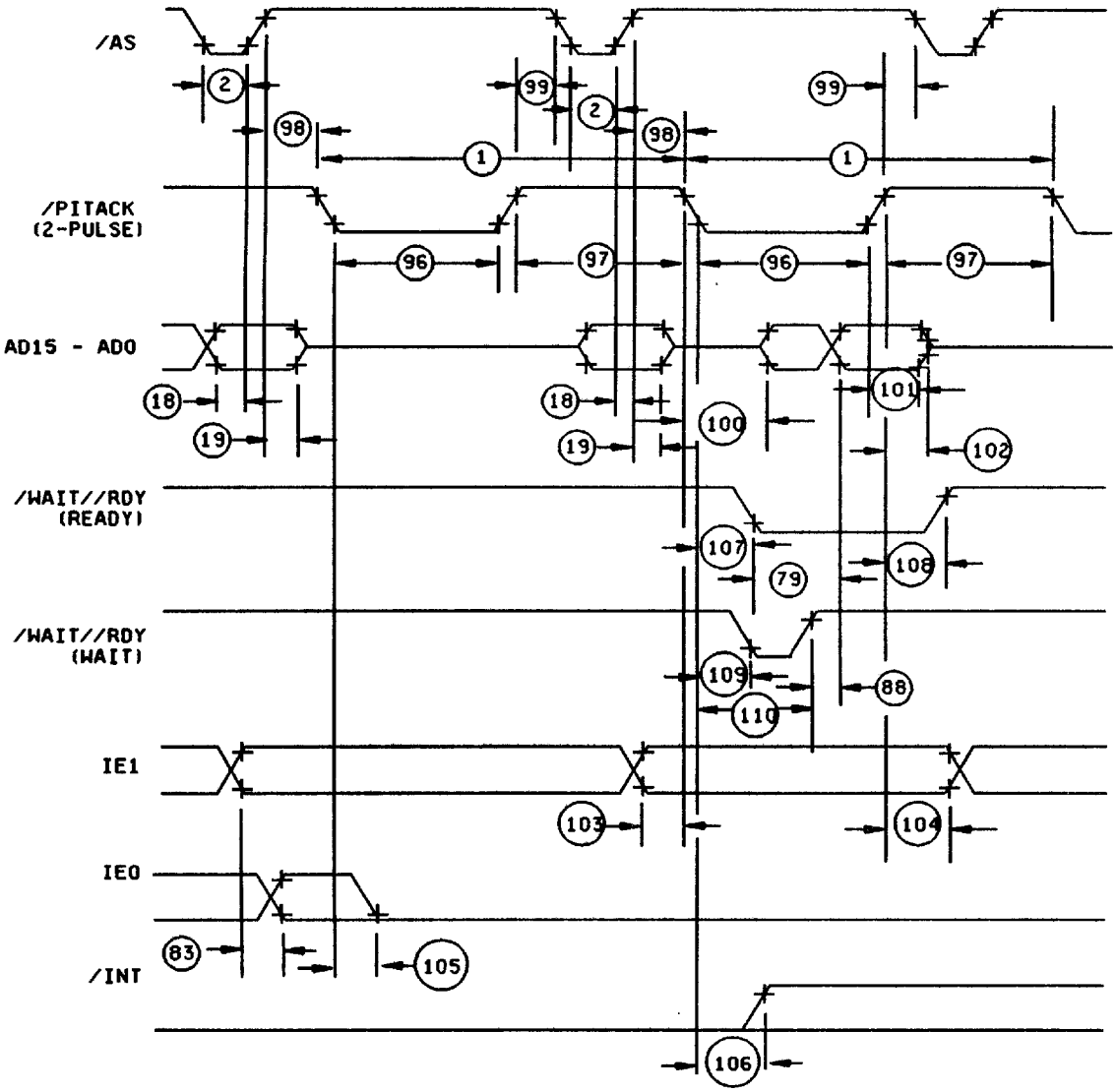
Non-MUX pulsed interrupt acknowledge cycle

FIGURE 3. Timing waveforms - Continued.



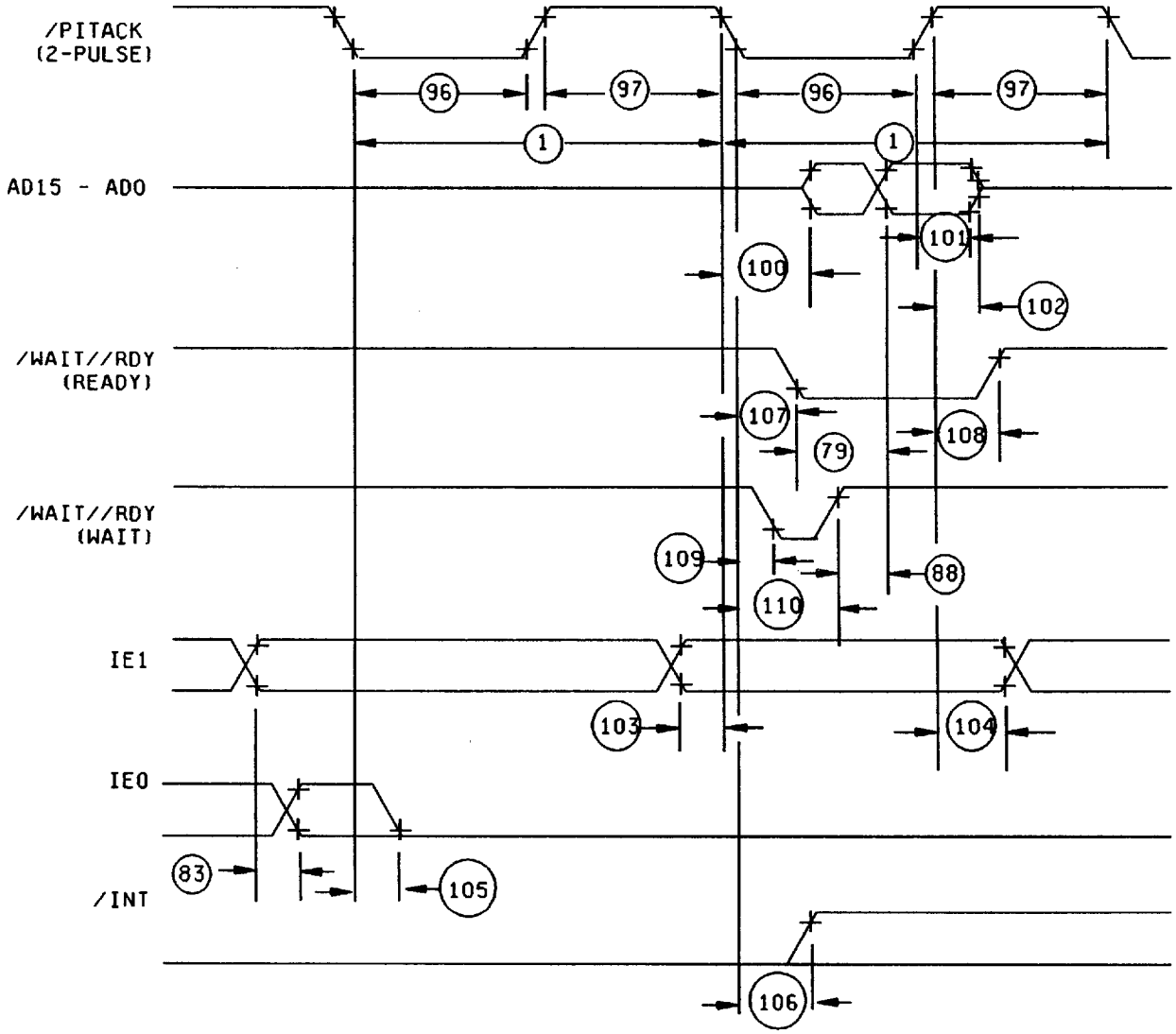
Non-MUX/RD interrupt acknowledge cycle

FIGURE 3. Timing waveforms - Continued.



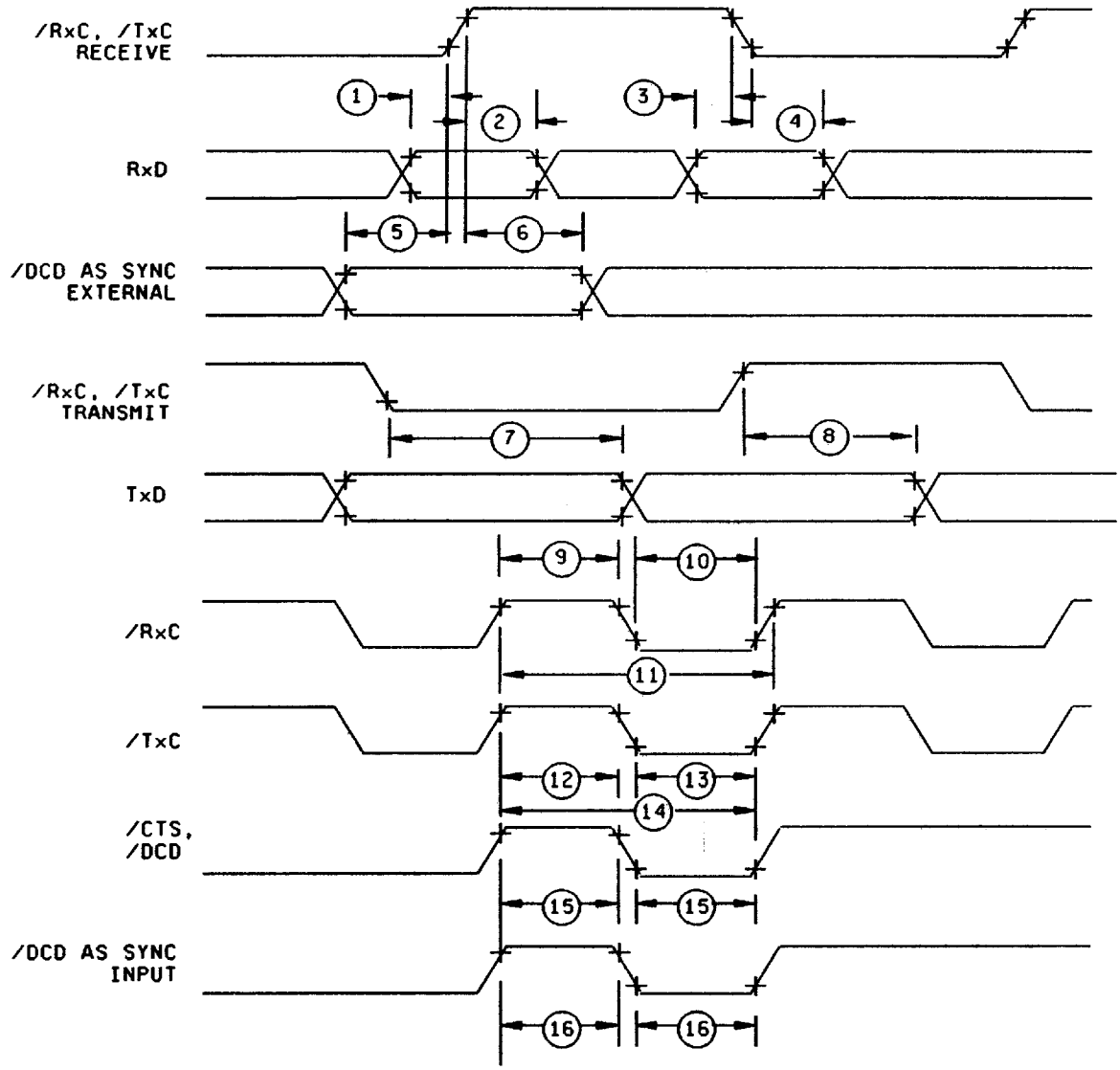
Multiplexed double-pulse intack cycle

FIGURE 3. Timing waveforms - Continued.



Non-multiplexed double-pulse intack cycle

FIGURE 3. Timing waveforms - Continued.



General timing

FIGURE 3. Timing waveforms - Continued.

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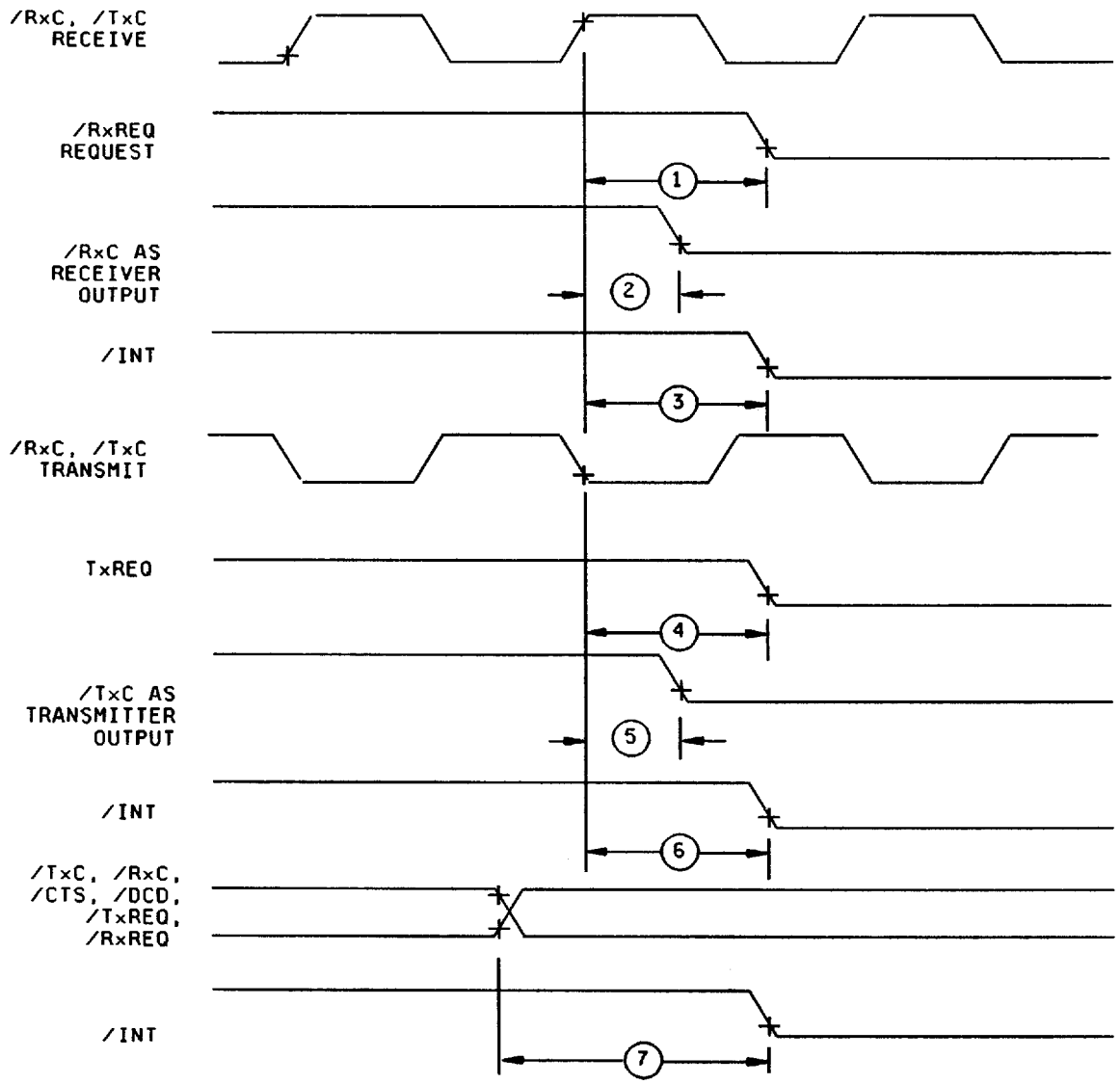

System timing

FIGURE 3. Timing waveforms - Continued.

4. QUALITY ASSURANCE PROVISIONS

4.1 Sampling and inspection. For device class M, sampling and inspection procedures shall be in accordance with section 4 of MIL-M-38510 to the extent specified in MIL-STD-883 (see 3.1 herein). For device classes B and S, sampling and inspection procedures shall be in accordance with MIL-M-38510 and method 5005 of MIL-STD-883, except as modified herein. For device classes Q and V, sampling and inspection procedures shall be in accordance with MIL-I-38535 and the device manufacturer's QM plan.

4.2 Screening. For device class M, screening shall be in accordance with method 5004 of MIL-STD-883, and shall be conducted on all devices prior to quality conformance inspection. For device classes B and S, screening shall be in accordance with method 5004 of MIL-STD-883, and shall be conducted on all devices prior to qualification and quality conformance inspection. For device classes Q and V, screening shall be in accordance with MIL-I-38535, and shall be conducted on all devices prior to qualification and technology conformance inspection.

4.2.1 Additional criteria for device classes M, B, and S.

a. Burn-in test, method 1015 of MIL-STD-883.

(1) Test condition A or D. For device class M, the test circuit shall be maintained by the manufacturer under document revision level control and shall be made available to the preparing or acquiring activity upon request. For device classes B and S, the test circuit shall be submitted to the qualifying activity. For device classes M, B, and S, the test circuit shall specify the inputs, outputs, biases, and power dissipation, as applicable, in accordance with the intent specified in test method 1015.

(2) T_A = +125°C, minimum.

b. Interim and final electrical test parameters shall be as specified in table II herein.

4.2.2 Additional criteria for device classes Q and V.

a. The burn-in test duration, test condition and test temperature, or approved alternatives shall be as specified in the device manufacturer's QM plan in accordance with MIL-I-38535. The burn-in test circuit shall be maintained under document revision level control of the device manufacturer's Technology Review Board (TRB) in accordance with MIL-I-38535 and shall be made available to the acquiring or preparing activity upon request. The test circuit shall specify the inputs, outputs, biases, and power dissipation, as applicable, in accordance with the intent specified in test method 1015.

b. Interim and final electrical test parameters shall be as specified in table II herein.

c. Additional screening for device class V beyond the requirements of device class Q shall be as specified in appendix B of MIL-I-38535.

4.3 Qualification inspection.

4.3.1 Qualification inspection for device classes B and S. Qualification inspection for device classes B and S shall be in accordance with MIL-M-38510. Inspections to be performed shall be those specified in method 5005 of MIL-STD-883 and herein for groups A, B, C, D, and E inspections (see 4.4.1 through 4.4.5).

4.3.2 Qualification inspection for device classes Q and V. Qualification inspection for device classes Q and V shall be in accordance with MIL-I-38535. Inspections to be performed shall be those specified in MIL-I-38535 and herein for groups A, B, C, D, and E inspections (see 4.4.1 through 4.4.5).

4.4 Conformance inspection. Quality conformance inspection for device class M shall be in accordance with MIL-STD-883 (see 3.1 herein) and as specified herein. Quality conformance inspection for device classes B and S shall be in accordance with MIL-M-38510 and as specified herein. Inspections to be performed for device classes M, B, and S shall be those specified in method 5005 of MIL-STD-883 and herein for groups A, B, C, D, and E inspections (see 4.4.1 through 4.4.5). Technology conformance inspection for classes Q and V shall be in accordance with MIL-I-38535 including groups A, B, C, D, and E inspections and as specified herein except where option 2 of MIL-I-38535 permits alternate in-line control testing.

4.4.1 Group A inspection.

a. Tests shall be as specified in table II herein.

b. For device class M, subgroups 7 and 8 tests shall be sufficient to verify the functionality. For device classes B and S, subgroups 7 and 8 tests shall be sufficient to verify the truth table as approved by the qualifying activity. For device classes Q and V, subgroups 7 and 8 shall include verifying the functionality of the device; these tests shall have been fault graded in accordance with MIL-STD-883, test method 5012 (see 1.5 herein).

c. Subgroup 4 (C_{IN}, C_{OUT}, and $C_{I/O}$ measurement) shall be measured only for the initial test and after process or design changes which may affect input capacitance. A minimum of five devices with zero rejects shall be required.

TABLE II. Electrical test requirements.

Test requirements	Subgroups (in accordance with MIL-STD-883, method 5005, table I)			Subgroups (in accordance with MIL-I-38535, table III)	
	Device class M	Device class B	Device class S	Device class Q	Device class V
Interim electrical parameters (see 4.2)			1, 7, 9		1, 7, 9
Final electrical parameters (see 4.2)	1, 2, 3, 7, 8, 9 10, 11 1/	1, 2, 3, 7, 8, 9 10, 11 1/	1, 2, 3, 7, 8, 9 10, 11 2/	1, 2, 3, 7, 8, 9 10, 11 1/	1, 2, 3, 7, 8, 9 10, 11 2/
Group A test requirements (see 4.4)	1, 2, 3, 4 7, 8, 9 10, 11	1, 2, 3, 4 7, 8, 9 10, 11	1, 2, 3, 4 7, 8, 9 10, 11	1, 2, 3, 4 7, 8, 9 10, 11	1, 2, 3, 4 7, 8, 9 10, 11
Group B end-point electrical parameters (see 4.4)			1, 7, 9		
Group C end-point electrical parameters (see 4.4)	1, 7, 9	1, 7, 9	1, 7, 9	1, 7, 9	1, 7, 9
Group D end-point electrical parameters (see 4.4)	1, 7, 9	1, 7, 9	1, 7, 9	1, 7, 9	1, 7, 9
Group E end-point electrical parameters (see 4.4)	----	----	----	----	----

1/ PDA applies to subgroup 1.
2/ PDA applies to subgroups 1 and 7.

4.4.2 Group B inspection. The group B inspection end-point electrical parameters shall be as specified in table II herein. For device class S steady-state life tests, the test circuit shall be submitted to the qualifying activity.

4.4.3 Group C inspection. The group C inspection end-point electrical parameters shall be as specified in table II herein.

4.4.3.1 Additional criteria for device classes M and B. Steady-state life test conditions, method 1005 of MIL-STD-883:

a. Test condition A or D. For device class M, the test circuit shall be maintained by the manufacturer under document revision level control and shall be made available to the preparing or acquiring activity upon request. For device class B, the test circuit shall be submitted to the qualifying activity. For device classes M and B, the test circuit shall specify the inputs, outputs, biases, and power dissipation, as applicable, in accordance with the intent specified in test method 1005.

b. T_A = +125°C, minimum.

c. Test duration: 1,000 hours, except as permitted by method 1005 of MIL-STD-883.

4.4.3.2 Additional criteria for device classes Q and V. The steady-state life test duration, test condition and test temperature, or approved alternatives shall be as specified in the device manufacturer's QM plan in accordance with MIL-I-38535. The test circuit shall be maintained under document revision level control by the device manufacturer's TRB in accordance with MIL-I-38535 and shall be made available to the acquiring or preparing activity upon request. The test circuit shall specify the inputs, outputs, biases, and power dissipation, as applicable, in accordance with the intent specified in test method 1005.

4.4.4 Group D inspection. The group D inspection end-point electrical parameters shall be as specified in table II herein.

4.4.5 Group E inspection. Group E inspection is required only for parts intended to be marked as radiation hardness assured (see 3.5 herein). RHA levels for device classes B, S, Q, and V shall be M, D, R, and H and for device class M shall be M and D.

a. End-point electrical parameters shall be as specified in table II herein.

b. For device classes M, B, and S, the devices shall be subjected to radiation hardness assured tests as specified in MIL-M-38510 for the RHA level being tested. For device classes Q and V, the devices or test vehicle shall be subjected to radiation hardness assured tests as specified in MIL-I-38535 for the RHA level being tested. All device classes must meet the postirradiation end-point electrical parameter limits as defined in table I at T_A = +25°C ±5°C, after exposure, to the subgroups specified in table II herein.

c. When specified in the purchase order or contract, a copy of the RHA delta limits shall be supplied.

5. PACKAGING

5.1 Packaging requirements. The requirements for packaging shall be in accordance with MIL-M-38510 for device classes M, B, and S and MIL-I-38535 for device classes Q and V.

6. NOTES

6.1 Intended use. Microcircuits conforming to this drawing are intended for use for Government microcircuit applications (original equipment), design applications, and logistics purposes.

6.1.1 Replaceability. Microcircuits covered by this drawing will replace the same generic device covered by a contractor-prepared specification or drawing.

6.1.2 Substitutability. Device classes B and Q devices will replace device class M devices.

6.2 Configuration control of SMD's. All proposed changes to existing SMD's will be coordinated with the users of record for the individual documents. This coordination will be accomplished in accordance with MIL-STD-481 using DD Form 1693, Engineering Change Proposal (Short Form).

6.3 Record of users. Military and industrial users shall inform Defense Electronics Supply Center when a system application requires configuration control and which SMD's are applicable to that system. DESC will maintain a record of users and this list will be used for coordination and distribution of changes to the drawings. Users of drawings covering microelectronic devices (FSC 5962) should contact DESC-EC, telephone (513) 296-6047.

6.4 Comments. Comments on this drawing should be directed to DESC-EC, Dayton, Ohio 45444, or telephone (513) 296-5377.

6.5 Abbreviations, symbols, and definitions. The abbreviations, symbols, and definitions used herein are defined in MIL-M-38510 and MIL-STD-1331 and as follows in table III.

TABLE III. Pin description.

Symbol	Function
/RESET	Reset (input, active low). This signal resets the device to a known state. The first write to the USC after a reset accesses the BCR to select additional bus options for the device.
/AS	Address Strobe (input, active low). This signal is used in the multiplexed bus modes to latch the address on the AD lines. The AS signal is not used in the non-multiplexed bus modes and should be tied to V_{DD} in these cases.
/DS	Data Strobe (input, active low). This signal strobes data out of the device during a read and may strobe an interrupt vector out of the device during an interrupt acknowledge cycle. DS also strobes data into the device during the active state of R/W.
/RD	Read strobe (input, active low). This signal strobes data out of the device during a read and may strobe an interrupt vector out of the device during an interrupt acknowledge cycle.
/WR	Write strobe (input, active low). This signal strobes data into the device during a write.
R//W	Read/Write (input). This signal determines the direction of data transfer for a read or write cycle in conjunction with DS.
/CS	Chip select (input, active low). This signal selects the device for access and must be asserted for read and write cycles, but is ignored during interrupt acknowledge and fly-by DMA transfers. In the case of a multiplexed bus interface, CS is latched by the rising edge of AS.
A//B	Channel A/Channel B select (input). This signal selects between the two channels in the device. High selects channel A and low selects channel B. This signal is sampled and the result is latched during the BCR (Bus Configuration Register) write. It programs the sense of the /WAIT//RDY signal appropriate for different bus interfaces. (See /WAIT//RDY below.)
D//C	Data/Control select (input). This signal, when high, provides for direct access to the RDR and TDR. In the case of a multiplexed bus interface, D//C high overrides the address provided to the device.
/SITACK	Status interrupt acknowledge (input, active low). This signal is a status signal that indicates that an interrupt acknowledge cycle is in progress. The device is capable of returning an interrupt vector that may be encoded with the type of interrupt pending during this acknowledge cycle. This signal is compatible with 680x0 family microprocessors.
/PITACK	Pulsed interrupt acknowledge (input, active low). This is a strobe signal that indicates that an interrupt acknowledge cycle is in progress. The device is capable of returning an interrupt vector that may be encoded with the type of interrupt pending during this acknowledge cycle. PITACK may be programmed to accept a single pulse or double pulse acknowledge type. This programming is done in the BCR. With the double pulse type selected, the first PITACK is recognized but no action takes place. The interrupt vector is returned on the second pulse if the no-vector option is not selected. The double pulse type is compatible with 8x86 family microprocessors.
/WAIT//RDY	/Wait data ready (output, active low). This signal indicates when the data is available during a read cycle, when the device is ready to receive data during a write cycle, and when a valid vector is available during an interrupt acknowledge cycle. It may be programmed to function either as a Wait signal or a Ready signal using the state of the A//B pin during the BCR write. When A//B is high during the BCR write, this signal functions as a wait output and thus supports the READY function of 8x86 family microprocessors. When A//B is low during the BCR write, this signal functions as a ready output and this supports the DTACK function of 680x0 family microprocessors.

TABLE III. Pin descriptions - Continued.

Symbol	Function
AD15 - AD0	Address/Data bus (bidirectional, active high, tri-state). The AD signals carry addresses to, and data to and from, the device. When the 16-bit non-multiplexed bus is selected, AD15 - 0 carry data to and from the device. Addresses are provided using a pointer within the device that is loaded with the desired register address. When the 8-bit non-multiplexed bus is selected without separate address, only AD7 - 0 are used to transfer data. The pointer is used for addressing; AD15 - 8 are unused. When the 8-bit non-multiplexed bus is selected with separate address, AD7 - 0 are used to transfer data, while AD15 - 8 are used as an address bus. When the 16-bit multiplexed bus is selected, addresses are latched from AD7 - 0 and data transfers are sixteen bits wide. When the 8-bit multiplexed bus is selected without separate address, only AD7 - 0 are used to transfer addresses and data; AD15 - 8 are unused. When the 8-bit multiplexed bus with separate address is selected, only AD7 - 0 are used to transfer data, while AD15 - 8 are used as an address bus.
/INTA,/INTB	Interrupt request (outputs active low). These signals indicate that the channel has an interrupt condition pending and is requesting service. These outputs are NOT open-drained.
IEIA, IEIB	Interrupt enable in (inputs active high). The IEI signal for each channel is used with the accompanying IEI signal to form an interrupt daisy chain. An active IEI indicates that no device having higher priority is requesting or servicing an interrupt.
IEOA, IEOB	Interrupt enable out (outputs active high). The IEO signal for each channel is used with the accompanying IEI signal to form an interrupt daisy chain. IEO is low if IEI is low, an interrupt is under service in the channel, or an interrupt is pending during an interrupt acknowledge cycle.
/TxACKA, /TxACKB	Transmit acknowledge (inputs or outputs, active low). The primary function of these signals is to perform fly-by DMA transfers to the transmit FIFO's. Also, they can be used as bit inputs or outputs.
/RxACKA, /RxACKB	Receive acknowledge (inputs or outputs, active low). The primary function of these signals is to perform fly-by DMA transfers from the receive FIFO's. Also they can be used as bit inputs or outputs.
TxDA, TxDB	Transmit data (outputs, active high 3-state). These signals carry the serial transmit data for each channel.
RxDA, RxDB	Receive data (inputs, active high). These signals carry the serial receive data for each channel.
/TxCA, /TxCB	Transmit clock (inputs or outputs, active low). These signals are used as clock inputs for any of the functional blocks within the device. They may also be used as outputs for various transmitter signals or internal clock signals.
/RxCA, /RxCB	Receive clock (inputs or outputs, active low). These signals are used as clock inputs for any of the functional blocks within the device. They may also be used as outputs for various receiver signals or internal clock signals.
/TxREQA, /TxREQB	Transmit request (inputs or outputs, active low). The primary function of these signals is to request DMA transfers to the transmit FIFO's. They may also be used as simple inputs or outputs.
/RxREQA, /RxREQB	Receive request (inputs or outputs active low). The primary function of these signals is to request DMA transfers from the receive FIFO's. They may also be used as simple inputs or outputs.
/CTSA, /CTSB	Clear to send (inputs or outputs active low). These signals are used as enables for the respective transmitters. They may also be programmed to generate interrupts on either transition or used as simple inputs or outputs.
/DCDA, /DCDB	Data carrier detect (inputs or outputs, active low). These signals are used as enables for the respective receivers. Also, they may be programmed to generate interrupts on either transition or used as simple inputs or outputs.

6.6 One part - one part number system. The one part - one part number system described below has been developed to allow for transitions between identical generic devices covered by the four major microcircuit requirements documents (MIL-M-38510, MIL-H-38534, MIL-I-38535, and 1.2.1 of MIL-STD-883) without the necessity for the generation of unique PIN's. The four military requirements documents represent different class levels, and previously when a device manufacturer upgraded military product from one class level to another, the benefits of the upgraded product were unavailable to the Original Equipment Manufacturer (OEM), that was contractually locked into the original unique PIN. By establishing a one part number system covering all four documents, the OEM can acquire to the highest class level available for a given generic device to meet system needs without modifying the original contract parts selection criteria.

Military documentation format	Example PIN under new system	Manufacturing source listing	Document listing
New MIL-M-38510 Military Detail Specifications (in the SMD format)	5962-XXXXXZZ(B or S)YY	QPL-38510 (Part 1 or 2)	MIL-BUL-103
New MIL-H-38534 Standardized Military Drawings	5962-XXXXXZZ(H or K)YY	QML-38534	MIL-BUL-103
New MIL-I-38535 Standardized Military Drawings	5962-XXXXXZZ(Q or V)YY	QML-38535	MIL-BUL-103
New 1.2.1 of MIL-STD-883 Standardized Military Drawings	5962-XXXXXZZ(M)YY	MIL-BUL-103	MIL-BUL-103

6.7 Sources of supply.

6.7.1 Sources of supply for device classes B and S. Sources of supply for device classes B and S are listed in QPL-38510.

6.7.2 Sources of supply for device classes Q and V. Sources of supply for device classes Q and V are listed in QML-38535. The vendors listed in QML-38535 have submitted a certificate of compliance (see 3.6 herein) to DESC-EC and have agreed to this drawing.

6.7.3 Approved sources of supply for device class M. Approved sources of supply for class M are listed in MIL-BUL-103. The vendors listed in MIL-BUL-103 have agreed to this drawing and a certificate of compliance (see 3.6 herein) has been submitted to and accepted by DESC-EC.