REVISIONS			
LTR	DESCRIPTION	DATE (YR-MO-DA)	APPROVED
A	Changes in accordance with NOR 5962-R031-93.	92-11-24	M. A. Frye
B	Changes in accordance with NOR 5962-R205-95.	95-12-15	M. A. Frye
C	Update and make changes to case outline N. Update boilerplate. Editorial changes throughout.	96-06-06	M. A. Frye

REV	C	C	C	C	C	C	C												
SHEET	35	36	37	38	39	40	41												
REV	C	C	C	C	C	C	C	C	C	C	C	C	C	C	C	C	C	C	C
SHEET	15	16	17	18	19	20	21	22	23	24	25	26	27	28	29	30	31	32	33	34

REV STATUS OF SHEETS	REV	C	C	C	C	C	C	C	C	C	C	C	C	C
	SHEET	1	2	3	4	5	6	7	8	9	10	11	12	13	14

PMIC N/A

STANDARD MICROCIRCUIT DRAWING

THIS DRAWING IS AVAILABLE FOR USE BY ALL DEPARTMENTS AND AGENCIES OF THE DEPARTMENT OF DEFENSE

AMSC N/A

PREPARED BY
Rajesh Pithadia

CHECKED BY
Kenneth S. Rice

APPROVED BY
Michael A. Frye

DRAWING APPROVAL DATE
92-03-04

REVISION LEVEL
C

DEFENSE ELECTRONICS SUPPLY CENTER
DAYTON, OHIO 45444

MICROCIRCUIT, MEMORY, DIGITAL, CMOS 1MEG X 4 DRAM, MONOLITHIC SILICON

SIZE	CAGE CODE	
A	67268	5962-90847

SHEET 1 OF 41

DESC FORM 193
JUL 94

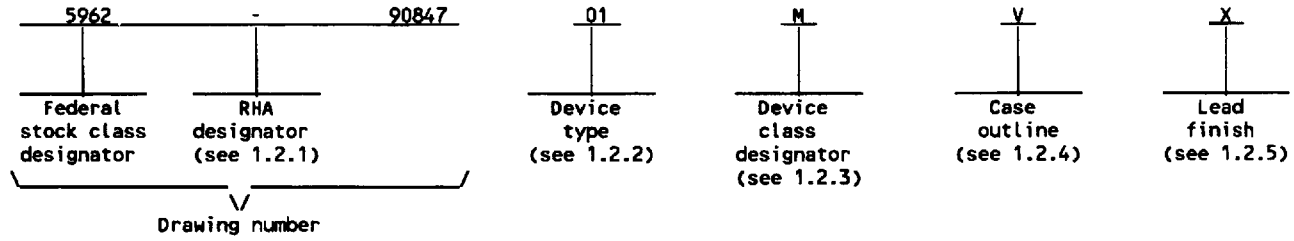
5962-E397-96

DISTRIBUTION STATEMENT A. Approved for public release; distribution is unlimited.

1. SCOPE

1.1 Scope. This drawing documents two product assurance class levels consisting of high reliability (device classes Q and M) and space application (device class V). A choice of case outlines and lead finishes are available and are reflected in the Part or Identifying Number (PIN). When available, a choice of Radiation Hardness Assurance (RHA) levels are reflected in the PIN.

1.2 PIN. The PIN is as shown in the following example:



1.2.1 RHA designator. Device classes Q and V RHA marked devices meet the MIL-PRF-38535 specified RHA levels and are marked with the appropriate RHA designator. Device class M RHA marked devices meet the MIL-PRF-38535, appendix A specified RHA levels and are marked with the appropriate RHA designator. A dash (-) indicates a non-RHA device.

1.2.2 Device type(s). The device type(s) identify the circuit function as follows:

Device type	Generic number 1/	Circuit function	Access time
01		1 M x 4, DYNAMIC RAM	120 ns
02		1 M x 4, DYNAMIC RAM	100 ns
03		1 M x 4, DYNAMIC RAM	80 ns

1.2.3 Device class designator. The device class designator is a single letter identifying the product assurance level as follows:

Device class	Device requirements documentation
M	Vendor self-certification to the requirements for MIL-STD-883 compliant, non-JAN class level B microcircuits in accordance with MIL-PRF-38535, appendix A
Q or V	Certification and qualification to MIL-PRF-38535

1.2.4 Case outline(s). The case outline(s) are as designated in MIL-STD-1835 and as follows:

Outline letter	Descriptive designator	Terminals	Package style
R	GDIP1-T20 or CDIP2-T20	20	dual-in-line
X	See figure 1	20	flat pack
Y	See figure 1	26/20	leadless ceramic chip carrier
Z	See figure 1	26/20	J-leaded chip carrier
U	See figure 1	20	dual-in-line
T	See figure 1	26/20	leadless ceramic chip carrier
M	See figure 1	20	flat pack
N	See figure 1	20	zig-zag in-line

1.2.5 Lead finish. The lead finish is as specified in MIL-PRF-38535 for device classes Q and V or MIL-PRF-38535, appendix A for device class M.

1/ Generic numbers are listed on the Standard Microcircuit Drawing Source Approval Bulletin at the end of this document and will also be listed in MIL-HDBK-103.

1.3 Absolute maximum ratings. 2/

Voltage range on any pin	-1 V dc to 7 V dc
Voltage range on V_{CC}	-1 V dc to 7 V dc
Short circuit output current	50 mA
Maximum power dissipation (P_D)	1 W
Storage temperature range	-65°C to +150°C
Lead temperature (soldering, 10 seconds)	+300°C
Thermal resistance, junction-to-case (θ_{JC})	
Case outline R	See MIL-STD-1835
Case outlines X, Y, Z, U, T, M, and N	20°C/W 3/
Junction temperature (T_J) 4/	+175°C

1.4 Recommended operating conditions.

Supply voltage range (V_{CC}) 5/	+4.5 V dc to +5.5 V dc
High-level input voltage (V_{IH})	2.4 V dc minimum to 6.5 V dc maximum
Low-level input voltage (V_{IL}) 6/	-1.0 V dc minimum to 0.8 V dc maximum
Case operating temperature range (T_C)	-55°C to +125°C

1.5 Digital logic testing for device classes Q and V.

Fault coverage measurement of manufacturing logic tests (MIL-STD-883, test method 5012)	7/ percent

2. APPLICABLE DOCUMENTS

2.1 Government specification, standards, and handbooks. The following specification, standards, and handbooks form a part of this drawing to the extent specified herein. Unless otherwise specified, the issues of these documents are those listed in the issue of the Department of Defense Index of Specifications and Standards (DoDISS) and supplement thereto, cited in the solicitation.

SPECIFICATION

MILITARY

MIL-PRF-38535 - Integrated Circuits, Manufacturing, General Specification for.

STANDARDS

MILITARY

MIL-STD-883 - Test Methods and Procedures for Microelectronics.
MIL-STD-973 - Configuration Management.
MIL-STD-1835 - Microcircuit Case Outlines.

HANDBOOKS

MILITARY

MIL-HDBK-103 - List of Standard Microcircuit Drawings (SMD's).
MIL-HDBK-780 - Standard Microcircuit Drawings.

(Unless otherwise indicated, copies of the specification, standards, and handbooks are available from the Standardization Document Order Desk, 700 Robbins Avenue, Building 4D, Philadelphia, PA 19111-5094.)

2/ Stresses above the absolute maximum rating may cause permanent damage to the device. Extended operation at the maximum levels may degrade performance and affect reliability.
3/ When the thermal resistance for this case is specified in MIL-STD-1835, that value shall supersede the value indicated herein.
4/ Maximum junction temperature shall not be exceeded except for allowable short duration burn-in screening conditions in accordance with method 5004 of Mil-STD-883.
5/ All voltage values in this drawing are with respect to V_{SS}.
6/ The algebraic convention, where the more negative (less positive) limit is designated as a minimum, is used in this drawing for logic voltage levels only.
7/ When a QML source exists, a value shall be provided.

2.2 Non-Government publications. The following documents form a part of this document to the extent specified herein. Unless otherwise specified, the issues of the documents which are DoD adopted are those listed in the issue of the DODISS cited in the solicitation. Unless otherwise specified, the issues of documents not listed in the DODISS are the issues of the documents cited in the solicitation.

ELECTRONICS INDUSTRIES ASSOCIATION (EIA)

JEDEC Standard No. 17 - A Standardized Test Procedure for the characterization of LATCH-UP in CMOS Integrated Circuits.

(Applications for copies should be addressed to the Electronics Industries Association, 2500 Wilson Blvd., Arlington, VA 22201.)

AMERICAN SOCIETY FOR TESTING AND MATERIALS (ASTM)

ASTM Standard F1192-88 - Standard Guide for the Measurement of Single Event Phenomena from Heavy Ion Irradiation of Semiconductor Devices.

(Applications for copies of ASTM publications should be addressed to the American Society for Testing and Materials, 1916 Race Street, Philadelphia, Pennsylvania 19103).

2.3 Order of precedence. In the event of a conflict between the text of this drawing and the references cited herein, the text of this drawing takes precedence. Nothing in this document, however, supersedes applicable laws and regulations unless a specific exemption has been obtained.

3. REQUIREMENTS

3.1 Item requirements. The individual item requirements for device classes Q and V shall be in accordance with MIL-PRF-38535 and as specified herein or as modified in the device manufacturer's Quality Management (QM) plan. The modification in the QM plan shall not affect the form, fit, or function as described herein. The individual item requirements for device class M shall be in accordance with MIL-PRF-38535, appendix A for non-JAN class level B devices and as specified herein.

3.2 Design, construction, and physical dimensions. The design, construction, and physical dimensions shall be as specified in MIL-PRF-38535 and herein for device classes Q and V or MIL-PRF-38535, appendix A and herein for device class M.

3.2.1 Case outline. The case outline shall be in accordance with 1.2.4 herein and figure 1.

3.2.2 Terminal connections. The terminal connections shall be as specified on figure 2.

3.2.3 Truth table. The truth table shall be as specified on figure 3.

3.2.4 Functional tests. Various functional tests used to test this device are contained in the appendix. If the test patterns cannot be implemented due to test equipment limitations, alternate test patterns to accomplish the same results shall be allowed. For device class M, alternate test patterns shall be maintained under document revision level control by the manufacturer and shall be made available to the preparing or acquiring activity upon request. For device classes Q and V, alternate test patterns shall be under the control of the device manufacturer's Technology Review Board (TRB) in accordance with MIL-PRF-38535 and shall be made available to the preparing or acquiring activity upon request.

3.2.5 Die overcoat. Polyimide and silicone coatings are allowable as an overcoat on the die for alpha particle protection only. Each coated microcircuit inspection lot (see inspection lot as defined in MIL-PRF-38535) shall be subjected to and pass the internal moisture content test at 5000 ppm (see method 1018 of MIL-STD-883). The frequency of the internal water vapor testing may not be decreased unless approved by the preparing activity. Samples may be pulled any time after seal.

3.3 Electrical performance characteristics and postirradiation parameter limits. Unless otherwise specified herein, the electrical performance characteristics and postirradiation parameter limits are as specified in table I and shall apply over the full case operating temperature range.

3.4 Electrical test requirements. The electrical test requirements shall be the subgroups specified in table IIA. The electrical tests for each subgroup are defined in table I.

3.5 Marking. The part shall be marked with the PIN listed in 1.2 herein. In addition, the manufacturer's PIN may also be marked as listed in MIL-HDBK-103. For packages where marking of the entire SMD PIN number is not feasible due to space limitations, the manufacturer has the option of not marking the "5962-" on the device. For RHA product using this option, the RHA designator shall still be marked. Marking for device classes Q and V shall be in accordance with MIL-PRF-38535. Marking for device class M shall be in accordance with MIL-PRF-38535, appendix A.

3.5.1 Certification/compliance mark. The certification mark for device classes Q and V shall be a "QML" or "Q" as required in MIL-PRF-38535. The compliance mark for device class M shall be a "C" as required in MIL-PRF-38535, appendix A.

3.6 Certificate of compliance. For device classes Q and V, a certificate of compliance shall be required from a QML-38535 listed manufacturer in order to supply to the requirements of this drawing (see 6.6.1 herein). For device class M, a certificate of compliance shall be required from a manufacturer in order to be listed as an approved source of supply in MIL-HDBK-103 (see 6.6.2 herein). The certificate of compliance submitted to DESC-EC prior to listing as an approved source of supply for this drawing shall affirm that the manufacturer's product meets, for device classes Q and V, the requirements of MIL-PRF-38535 and herein or for device class M, the requirements of MIL-PRF-38535, appendix A and herein.

3.7 Certificate of conformance. A certificate of conformance as required for device classes Q and V in MIL-PRF-38535 or for device class M in MIL-PRF-38535, appendix A shall be provided with each lot of microcircuits delivered to this drawing.

3.8 Notification of change for device class M. For device class M, notification to DESC-EC of change of product (see 6.2 herein) involving devices acquired to this drawing is required for any change as defined in MIL-STD-973.

3.9 Verification and review for device class M. For device class M, DESC, DESC's agent, and the acquiring activity retain the option to review the manufacturer's facility and applicable required documentation. Offshore documentation shall be made available onshore at the option of the reviewer.

3.10 Microcircuit group assignment for device class M. Device class M devices covered by this drawing shall be in microcircuit group number 41 (see MIL-PRF-38535, appendix A).

4. QUALITY ASSURANCE PROVISIONS

4.1 Sampling and inspection. For device classes Q and V, sampling and inspection procedures shall be in accordance with MIL-PRF-38535 or as modified in the device manufacturer's Quality Management (QM) plan. The modification in the QM plan shall not affect the form, fit, or function as described herein. For device class M, sampling and inspection procedures shall be in accordance with MIL-PRF-38535, appendix A.

4.2 Screening. For device classes Q and V, screening shall be in accordance with MIL-PRF-38535, and shall be conducted on all devices prior to qualification and technology conformance inspection. For device class M, screening shall be in accordance with method 5004 of MIL-STD-883, and shall be conducted on all devices prior to quality conformance inspection.

4.2.1 Additional criteria for device class M.

a. Delete the sequence specified as initial (preburn-in) electrical parameters through interim (postburn-in) electrical parameters of method 5004 and substitute lines 1 through 6 of table IIA herein.

b. The test circuit shall be maintained by the manufacturer under document revision level control and shall be made available to the preparing or acquiring activity upon request. The test circuit shall specify the inputs, outputs, biases, and power dissipation, as applicable, in accordance with the intent specified in test method 1015.

(1) Dynamic burn-in for device class M (method 1015 of MIL-STD-883, test condition D; for circuit, see 4.2.1b herein).

c. Interim and final electrical parameters shall be as specified in table IIA herein.

TABLE I. Electrical performance characteristics.

Test	Symbol	Conditions 1/ 2/ $-55°C \le T_C \le +125°C$, $4.5\ V \le V_{CC} \le 5.5\ V$ unless otherwise specified	Group A subgroups	Device type	Limits		Unit
					Min	Max	
High-level output voltage	V_{OH}	$I_{OH} = -5$ mA, $V_{IL} = 0.8$ V, $V_{IH} = 2.4$ V	1,2,3	All	2.4		V
Low-level output voltage	V_{OL}	$I_{OL} = 4.2$ mA, $V_{IL} = 0.8$ V, $V_{IH} = 2.4$ V	1,2,3	All		0.4	V
Input leakage current	I_I	$V_I = 0$ V to 6.5 V, $V_{CC} = 5.5$ V, All other pins = 0 V to VCC	1,2,3	All		±10	µA
Output leakage current	I_O	$V_{CC} = 5.5$ V, $\overline{CAS}$ high, $V_O = V_{CC}$ to 0 V,	1,2,3	All		±10	µA
Average operating power supply current (random read or write cycle) 3/	I_{CC1}	Minimum cycle time, $V_{CC} = 5.5$ V, Addresses, $\overline{RAS}$, $\overline{CAS}$ cycling	1,2,3	01		70	mA
				02		80	
				03		90	
Standby power supply current (TTL)	I_{CC2}	$V_{CC} = 5.5$ V, $V_{IH} = 2.4$ V, $\overline{RAS}$ and $\overline{CAS}$ high	1,2,3	All		4	mA
Average operating power supply current (RAS-only refresh, or CBR refresh) 4/	I_{CC3}	$V_{CC} = 5.5$ V, Minimum cycle, $\overline{RAS}$ cycling, $\overline{CAS} = 2.4$ V (RAS only refresh) RAS, CAS, addresses cycling (CBR refresh)	1,2,3	01		70	mA
				02		80	
				03		90	
Average operating power supply current (Page mode) 3/	I_{CC4}	$\overline{RAS} = 0.8$ V, CAS, addresses cycling, t_{PC} = minimum, $V_{CC} = 5.5$ V	1,2,3	01		40	mA
				02		50	
				03		60	
Input capacitance, address inputs	$C_I(A)$	f = 1 MHz See 4.4.1d, Bias on pins under test = 0 V, $V_{CC} = 5.0$ V nominal, $T_A = 25°C$	4	All		7	pF
Input capacitance, RAS, CAS, W, OE	$C_I(S)$		4	All		10	pF
I/O capacitance, DQ's	C_{DQ}		4	All		10	pF

See footnotes at end of table.

TABLE IA. Electrical performance characteristics - continued.

Test	Symbol	Conditions 1/ 2/ $-55°C \le T_C \le +125°C$ $4.5\ V \le V_{CC} \le 5.5\ V$ unless otherwise specified	Group A subgroups	Device type	Limits		Unit
					Min	Max	
Access time from column address	t_{AA}	(See figures 4 and 5) 1/ 2/ 5/ 6/ 7/ 8/	9,10,11	01		55	ns
				02		45	
				03		40	
Access time from CAS low 9/	t_{CAC}		9,10,11	01		30	ns
				02		25	
				03		20	
Access time from column precharge	t_{CPA}		9,10,11	01		55	ns
				02		50	
				03		45	
Access time from RAS low 10/	t_{RAC}		9,10,11	01		120	ns
				02		100	
				03		80	
Access time from OE low 11/	t_{OEA} or t_{OE}		9,10,11	01		30	ns
				02		25	
				03		20	
Output disable time after CAS high 12/	t_{OFF}		9,10,11	01		30	ns
				02		25	
				03		20	
Output disable time after OE high 12/	t_{OEZ} or t_{OD}		9,10,11	01		30	ns
				02		25	
				03		20	
Cycle time, random read or write 13/	t_{RC}		9,10,11	01	210		ns
				02	180		
				03	150		
Cycle time, read-write	t_{RWC}		9,10,11	01	285		ns
				02	245		
				03	205		

See footnotes at end of table.

TABLE I. Electrical performance characteristics - continued.

Test	Symbol	Conditions $-55°C \le T_C \le +125°C$ $4.5\ V \le V_{CC} \le 5.5\ V$ unless otherwise specified	Group A subgroups	Device type	Limits		Unit
					Min	Max	
Cycle time, page-mode read or write 14/	t_{PC}	(See figures 4 and 5) 1/ 2/ 5/ 6/ 7/ 8/	9,10,11	01	65		ns
				02	60		
				03	50		
Cycle time, page-mode read-write	t_{PRWC}		9,10,11	01	135		ns
				02	120		
				03	105		
Pulse duration, page mode, RAS low 15/	t_{RASP}		9,10,11	01	120		ns
				02	100		
				03	80		
				All		100	µs
Pulse duration, non-page--mode, RAS low 15/	t_{RAS}		9,10,11	01	120		ns
				02	100		
				03	80		
				All		10	µs
Pulse duration, $\overline{CAS}$ low 16/	t_{CAS}		9,10,11	01	30		ns
				02	25		
				03	20		
				All		10	µs
Pulse duration, $\overline{CAS}$ high (Page- mode and non- page-mode) 17/	t_{CP} or t_{CPN}		9,10,11	01	15		ns
				02	12		
				03	12		
Pulse duration, $\overline{RAS}$ high (precharge)	t_{RP}		9,10,11	01	80		ns
				02	70		
				03	60		
Pulse duration, write	t_{WP}		9,10,11	01	25		ns
				02	20		
				03	15		

See footnotes at end of table.

TABLE I. Electrical performance characteristics - continued.

Test	Symbol	Conditions $-55°C \le T_C \le +125°C$ $4.5\ V \le V_{CC} \le 5.5\ V$ unless otherwise specified	Group A subgroups	Device type	Limits		Unit
					Min	Max	
Setup time, column-address before CAS low	t_{ASC}	(See figures 4 and 5) 1/ 2/ 5/ 6/ 7/ 8/	9,10,11	All	0		ns
Setup time, row-address before RAS low	t_{ASR}		9,10,11	All	0		ns
Setup time, data 18/	t_{DS}		9,10,11	All	0		ns
Setup time, read before CAS low	t_{RCS}		9,10,11	All	0		ns
Setup time, W low before $\overline{CAS}$ high	t_{CWL}		9,10,11	01	30		ns
				02	25		
				03	20		
Setup time, W low before $\overline{RAS}$ high	t_{RWL}		9,10,11	01	30		ns
				02	25		
				03	20		
Setup time, $\overline{W}$ low before $\overline{CAS}$ low (Early write operation only) 19/	t_{WCS}		9,10,11	All	0		ns
Setup time, W high (CAS before RAS refresh only)	t_{WSR} or t_{WRP}		9,10,11	All	10		ns
Hold time, column-address after CAS low	t_{CAH}		9,10,11	01	20		ns
				02	20		
				03	15		
Hold time, data after RAS low	t_{DHR}		9,10,11	01	90		ns
				02	75		
				03	60		
Hold time, data 18/	t_{DH}		9,10,11	01	25		ns
				02	20		
				03	15		

See footnotes at end of table.

TABLE I. Electrical performance characteristics - continued.

Test	Symbol	Conditions $-55°C \le T_C \le +125°C$, $4.5\ V \le V_{CC} \le 5.5\ V$, unless otherwise specified	Group A subgroups	Device type	Limits		Unit
					Min	Max	
Hold time, column address after RAS low 16/	t_{AR}	(See figures 4 and 5) 1/ 2/ 5/ 6/ 7/ 8/	9,10,11	01	90		ns
				02	75		
				03	60		
Hold time, row-address after RAS low	t_{RAH}		9,10,11	01	15		ns
				02	15		
				03	10		
Hold time, read after $\overline{CAS}$ high 20/	t_{RCH}		9,10,11	All	0		ns
Hold time, read after $\overline{RAS}$ high 20/	t_{RRH}		9,10,11	All	0		ns
Hold time, write after $\overline{CAS}$ low (Early write operation only)	t_{WCH}		9,10,11	01	25		ns
				02	20		
				03	15		
Hold time, write after $\overline{RAS}$ low 16/	t_{WCR}		9,10,11	01	90		ns
				02	75		
				03	60		
Hold time, $\overline{W}$ high ($\overline{CAS}$ before RAS refresh only	t_{WHR} or t_{WRH}		9,10,11	All	10		ns
Delay time, column address to W low (Read write operation only) 19/	t_{AWD}		9,10,11	01	90		ns
				02	80		
				03	70		
Delay time, $\overline{RAS}$ low to $\overline{CAS}$ high (CAS-before RAS refresh only) 21/	t_{CHR}		9,10,11	01	25		ns
				02	20		
				03	20		
Delay time, $\overline{CAS}$ high to $\overline{RAS}$ low	t_{CRP}		9,10,11	01	10		ns
				02	5		
				03	5		

See footnotes at end of table.

TABLE I. Electrical performance characteristics - continued.

Test	Symbol	Conditions $-55°C \le T_C \le +125°C$ $4.5\ V \le V_{CC} \le 5.5\ V$ unless otherwise specified	Group A subgroups	Device type	Limits		Unit
					Min	Max	
Delay time, $\overline{RAS}$ low to $\overline{CAS}$ high	t_{CSH}	(See figures 4 and 5) 1/ 2/ 5/ 6/ 7/ 8/	9,10,11	01	120		
				02	100		
				03	80		
Delay time, $\overline{CAS}$ low to $\overline{RAS}$ low (CAS before RAS refresh only) 21/	t_{CSR}		9,10,11	All	10		ns
Delay time, $\overline{CAS}$ low to $\overline{W}$ low (Read-write operation only) 19/	t_{CWD}		9,10,11	01	70		ns
				02	60		
				03	50		
Hold time, $\overline{OE}$ command 22/	t_{OEH}		9,10,11	01	30		ns
				02	25		
				03	20		
Delay time, $\overline{OE}$ to data 23/	t_{OED}		9,10,11	01	30		ns
				02	25		
				03	20		
Hold time, $\overline{RAS}$ referenced to to OE 24/	t_{ROH}		9,10,11	01	30		ns
				02	25		
				03	20		
Delay time, $\overline{RAS}$ low to column-address 25/	t_{RAD}		9,10,11	01	20	65	ns
				02	20	50	
				03	15	40	
Delay time, column-address to RAS high	t_{RAL}		9,10,11	01	55		ns
				02	50		
				03	40		
Delay time, colmn-address to CAS high 23/	t_{CAL}		9,10,11	01	55		ns
				02	50		
				03	40		

See footnotes at end of table.

TABLE I. Electrical performance characteristics - continued.

Test	Symbol	Conditions $-55°C \le T_C \le +125°C$, $4.5\ V \le V_{CC} \le 5.5\ V$, unless otherwise specified	Group A subgroups	Device type	Limits		Unit
					Min	Max	
Delay time, $\overline{RAS}$ low to $\overline{CAS}$ low 26/	t_{RCD}	(See figures 4 and 5) 1/ 2/ 5/ 6/ 7/ 8/	9,10,11	01	25	90	ns
				02	25	75	
				03	20	60	
Delay time, $\overline{RAS}$ high to $\overline{CAS}$ low	t_{RPC}		9,10,11	All	0		ns
Delay time, $\overline{CAS}$ low to $\overline{RAS}$ high	t_{RSH}		9,10,11	01	30		ns
				02	25		
				03	20		
Delay time $\overline{RAS}$ low to $\overline{W}$ low (Read-write operation only) 19/	t_{RWD}		9,10,11	01	160		ns
				02	135		
				03	110		
$\overline{CAS}$ to output in low Z 23/	t_{CLZ}		9,10,11	All	0	27/	ns
Refresh time interval	t_{REF}		9,10,11	All		16	ms
Setup time, $\overline{OE}$ prior to $\overline{RAS}$ during hidden refresh cycle 23/	t_{ORD}		9,10,11	All	0		ns

1/ V_{SS} is common for all voltages.

2/ An initial pause of 200 µs is required after power-up followed by a minimum of 8 initialization cycles after full V_{CC} level is achieved. The 8 initialization cycles need to be RAS only refresh or CBR with W high to assure proper device operation. The 8 initialization cycles should be repeated any time the 16 ms refresh requirement is exceeded.

3/ I_{CC} is dependent on output loading and cycle rates. Specified values are obtained with minimum cycle time and the outputs open.

4/ I_{CC} is dependent on cycle rates.

5/ AC characteristics assume transition time $t_T = 5$ ns.

6/ V_{IL} (max) and V_{IH} (min) are reference levels for measuring timing of input signals. Transition times are measured between V_{IL} and V_{IH}.

7/ In addition to meeting the transition rate specification, all input signals must make the transition between V_{IL} and V_{IH} (or V_{IH} and V_{IL}) in a monotonic manner.

8/ When operating the device, transition times (rise and fall) for all input signals are to be a minimum of 3 ns and a maximum of 50 ns.

9/ Assumes that $t_{RCD} > t_{RCD}$ (max).

10/ Assumes that $t_{RCD} < t_{RCD}$ (max). If t_{RCD} is greater than the maximum recommended value shown in this table, t_{RAC} will increase by the amount that t_{RCD} exceeds the value shown.

11/ During a read cycle, if $\overline{OE}$ is low and then taken high, DQs go high impedance. If $\overline{OE}$ is permanently held low, a late-write or read-modify-write operation is not possible.

12/ t_{OFF} and t_{OEZ} or t_{OD} are specified when the output is no longer driven. The output is disabled (high impedance) by bringing either OE or CAS high and it is not referenced to V_{OH} or V_{OL}.

13/ The minimum specifications are used only to indicate cycle time at which proper operation over the full temperature range ($-55°C \le T_C \le +125°C$) is assured.

14/ To guarantee t_{PC} min, t_{ASC} should be greater than or equal to t_{CP}.

15/ In a read-write cycle, t_{RWD} and t_{RWL} must be observed.

16/ In a read-write cycle, t_{CWD} and t_{CWL} must be observed.

17/ If $\overline{CAS}$ is low at the falling edge of $\overline{RAS}$, DQs will be maintained from the previous cycle. To initiate a new cycle and clear the data out buffer, CAS must be pulsed high for t_{CPN}.

18/ These parameters are referenced to $\overline{CAS}$ leading edge in early-write cycles and $\overline{W}$ leading edge in late-write or read-modify-write cycles.

19/ t_{WCS}, t_{RWD}, t_{AWD} and t_{CWD} are restrictive operating parameters in late-write and read-modify-write cycles only. If $t_{WCS} > t_{WCS}$ (min), the cycle is an early-write cycle and the data outputs will remain open circuit throughout the entire cycle. If $t_{RWD} > t_{RWD}$ (min), $t_{AWD} > t_{AWD}$ (min) and $t_{CWD} > t_{CWD}$ (min), the cycle is a read-write and the data outputs will contain data read from the selected cells. If neither of the above conditions are met, the state of the data outputs (at access time and until CAS goes back to V_{IH}) is indeterminate.

20/ Either t_{RRH} or t_{RCH} must be satisfied for a read cycle.

21/ Enables on-chip refresh and address counters.

22/ Late-write and read-modify-write cycles must have both t_{OD} and t_{OEH} met ($\overline{OE}$ high during write cycle) in order to ensure that the output buffers will be open during the write cycle. The DQs will provide the previously read data if CAS remains low and OE is taken back low after t_{OEH} is met. If CAS goes high prior to OE going back low, then the DQs will remain open.

23/ This parameter may not be tested, but shall be guaranteed to the limits specified in table I and is included to help with device application.

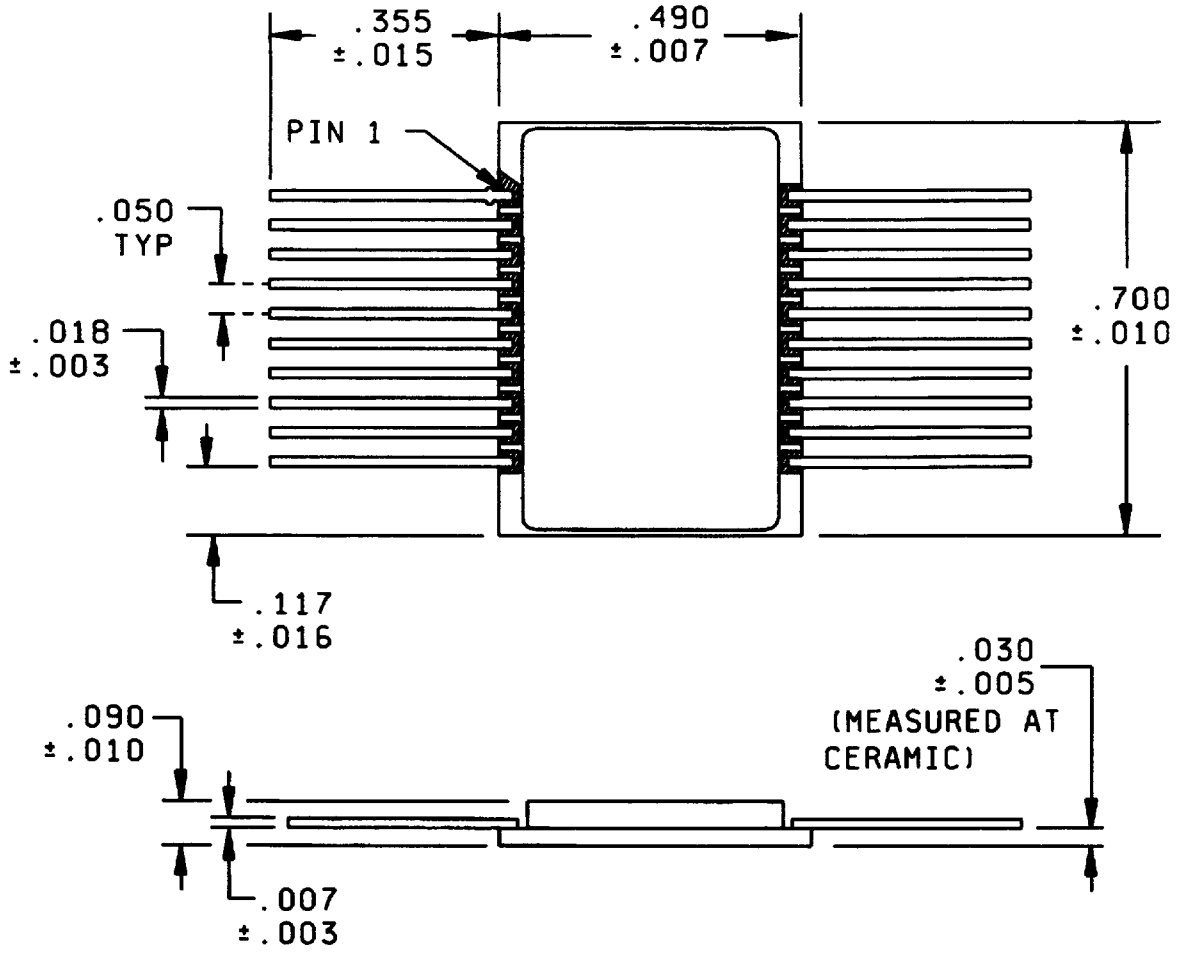
24/ This parameter does not apply where $\overline{OE}$ is not related to $\overline{RAS}$ in device design.

25/ Maximum value specified only to guarantee access time. Operation within the t_{RAD} (max) limit ensures that t_{RCD} (max) can be met. t_{RAD} (max) is specified as a reference point only; if t_{RAD} is greater than the specified t_{RAD} (max) limit, then access time is controlled exclusively by t_{AA}.

26/ Maximum value specified only to guarantee access time. Operation within the t_{RCD} (max) limit ensures that t_{RAC} (max) can be met. t_{RCD} (max) is specified as a reference point only; if t_{RCD} is greater than the specified t_{RCD} (max) limit, then access time is controlled exclusively by t_{CAC}.

27/ Valid data is presented at the output after all access times are satisfied but may go from three-state to an invalid data state prior to the specified access times as the outputs are driven when CAS goes low.

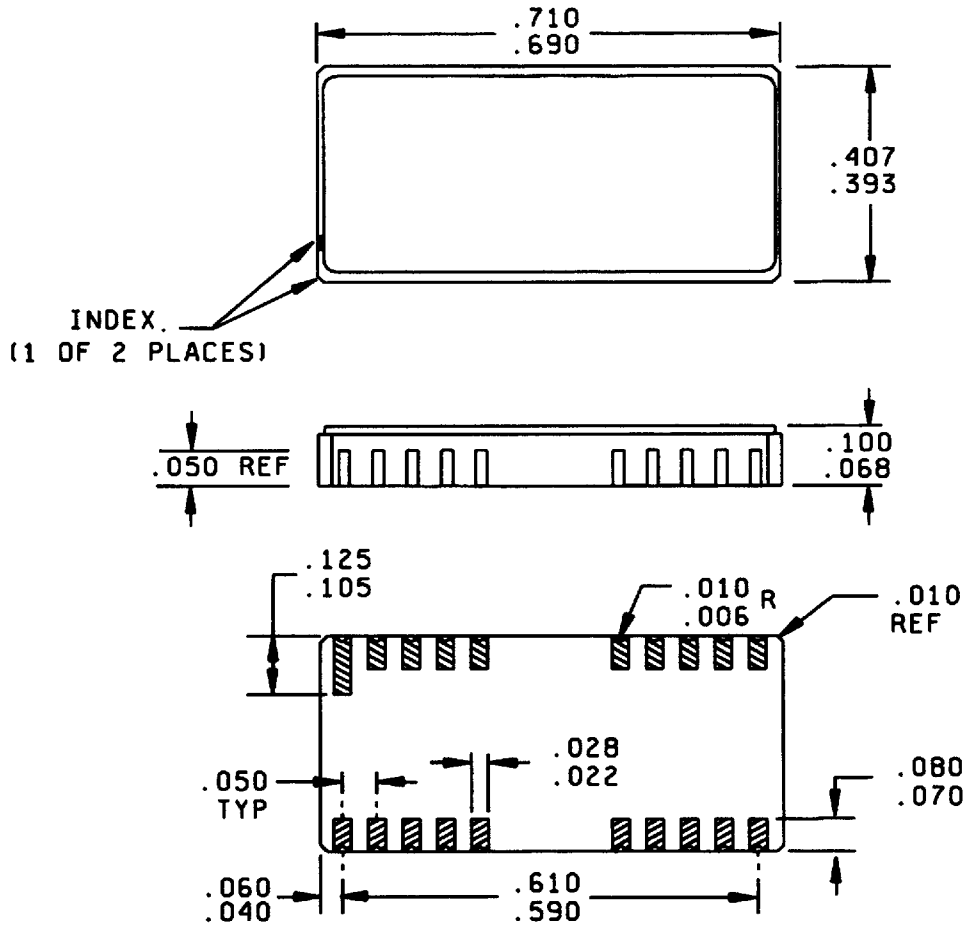
Case X



Inches	mm	Inches	mm
.003	0.08	.030	0.76
.005	0.13	.050	1.27
.007	0.18	.090	2.29
.010	0.25	.117	2.97
.015	0.38	.355	9.02
.016	0.41	.490	12.45
.018	0.46	.700	17.78

FIGURE 1. Case outlines.

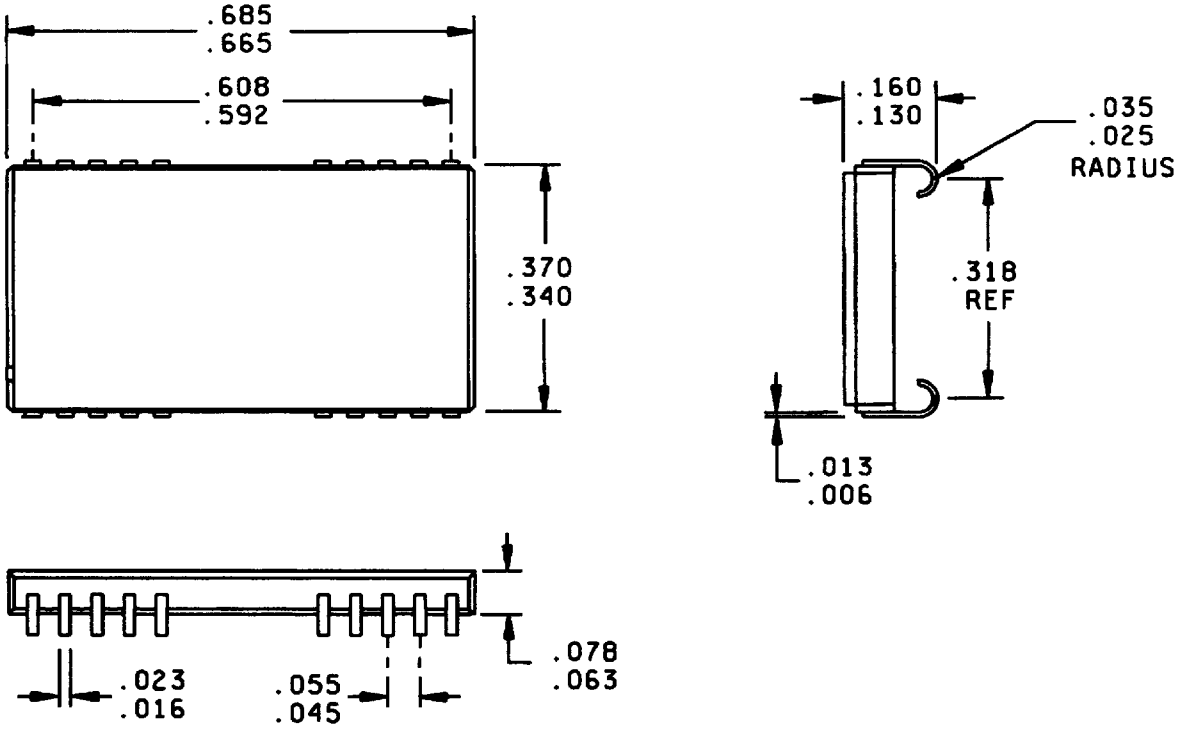
Case Y



Inches	mm	Inches	mm
.006	0.15	.080	2.03
.010	0.25	.100	2.54
.022	0.56	.105	2.68
.028	0.71	.125	3.18
.040	1.02	.393	9.98
.050	1.27	.407	10.34
.060	1.52	.590	14.98
.068	1.72	.610	15.49
.070	1.78	.690	17.52
		.710	18.03

FIGURE 1. Case outlines - Continued.

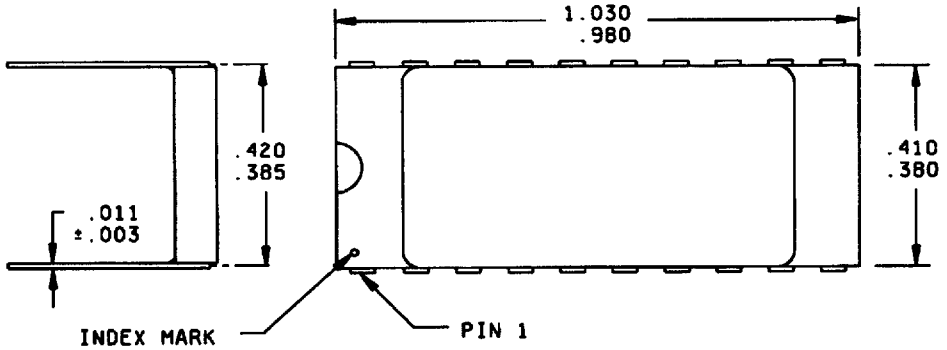
Case Z

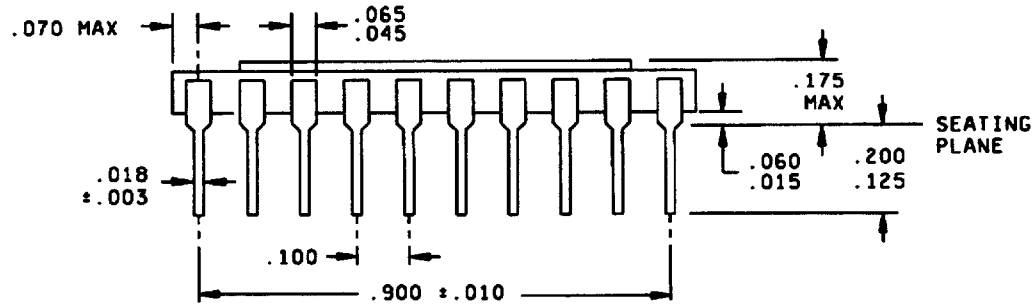


Inches	mm	Inches	mm
.006	0.15	.130	3.30
.013	0.33	.160	4.06
.016	0.41	.318	8.08
.023	0.58	.340	8.64
.025	0.64	.370	9.40
.035	0.89	.592	15.04
.045	1.14	.608	15.44
.055	1.40	.665	16.89
.063	1.60	.685	17.40
.078	1.98		

FIGURE 1. Case outlines - Continued.

Case U

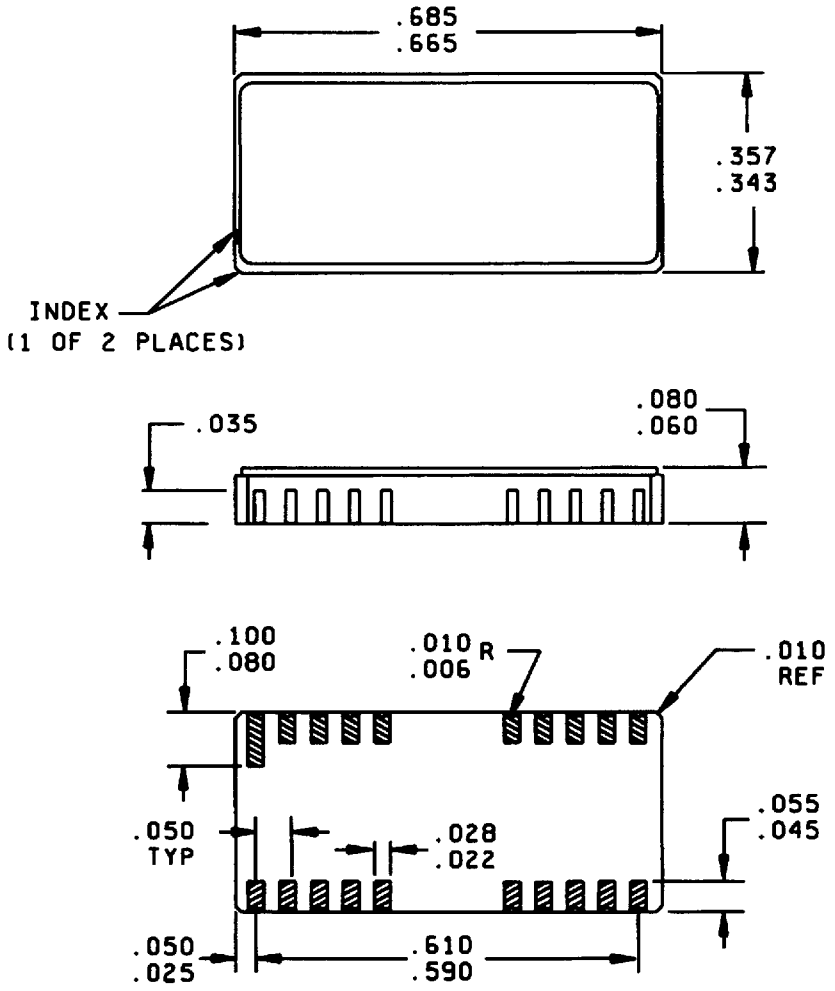




Inches	mm	Inches	mm
.003	0.08	.125	3.18
.010	0.25	.175	4.44
.011	0.28	.200	5.08
.015	0.38	.380	9.65
.018	0.46	.385	9.78
.045	1.14	.410	10.41
.060	1.52	.420	10.67
.065	1.65	.900	22.86
.070	1.78	.980	24.89
.100	2.54	1.030	26.16

FIGURE 1. Case outlines - Continued.

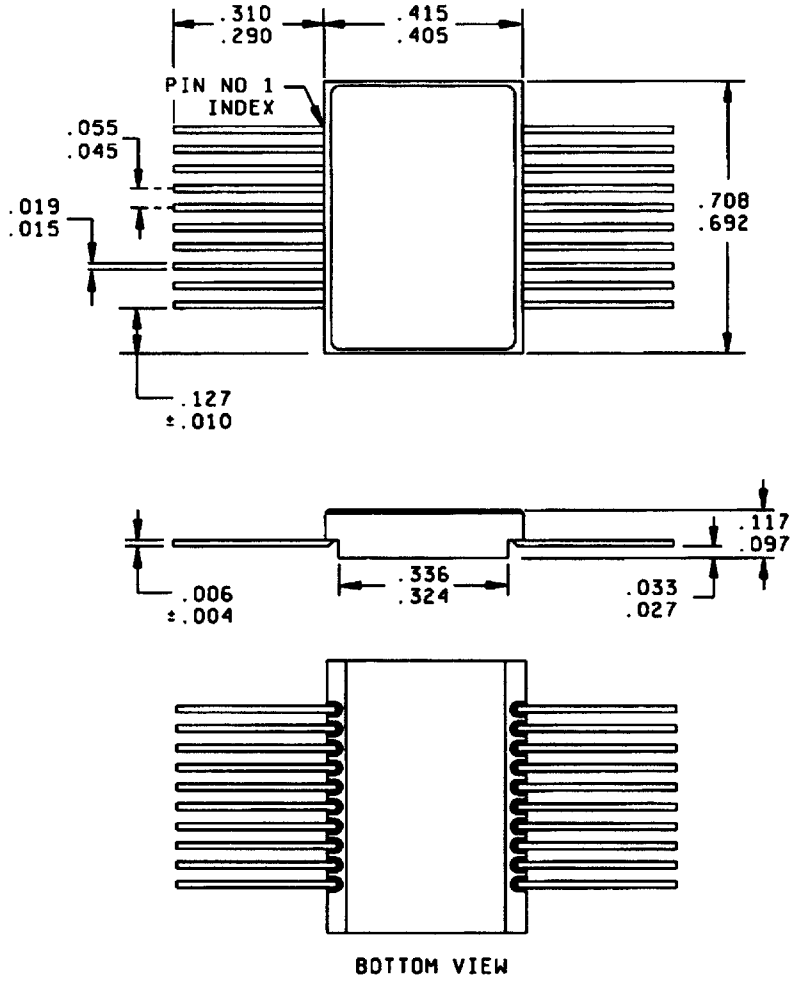
Case T



Inches	mm	Inches	mm
.006	0.15	.060	1.52
.010	0.25	.080	2.03
.022	0.56	.100	2.54
.025	0.64	.343	8.71
.028	0.71	.357	9.07
.035	0.89	.590	14.99
.045	1.14	.610	15.49
.050	1.27	.665	16.89
.055	1.40	.685	17.40

FIGURE 1. Case outlines - Continued.

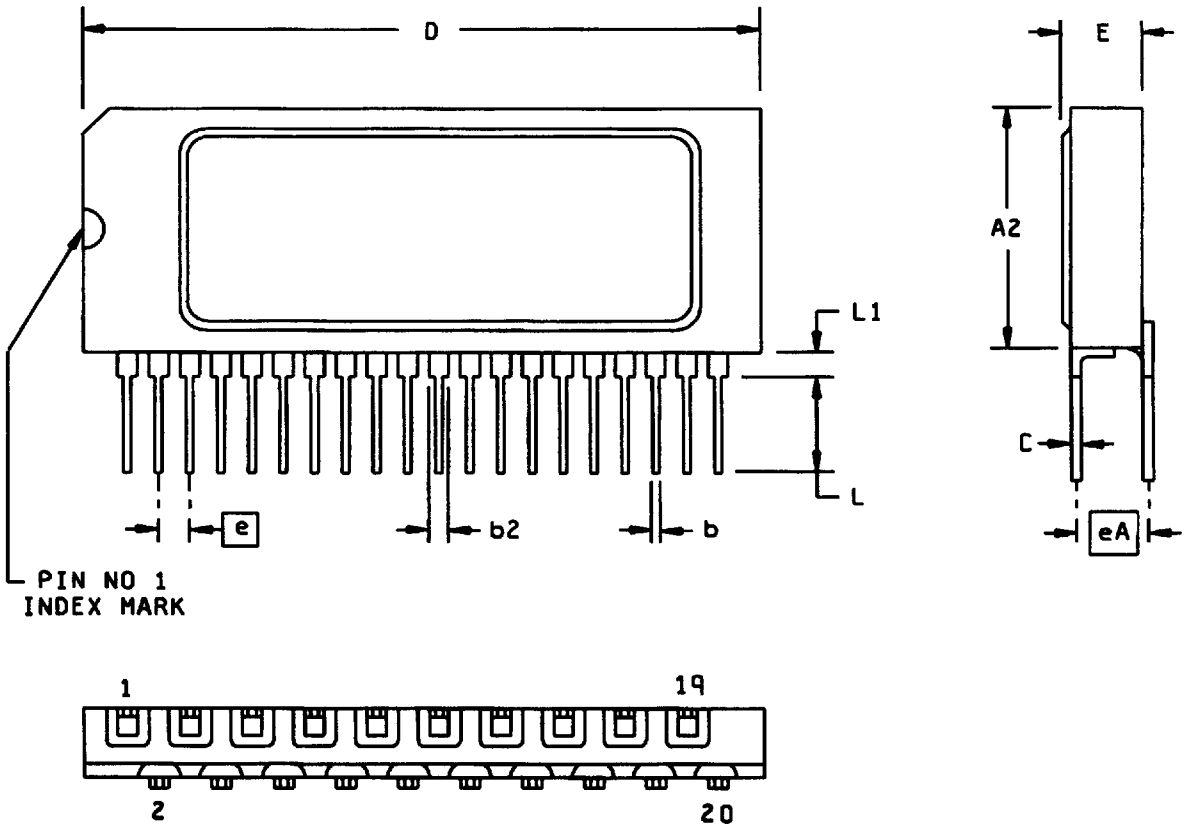
Case M



Inches	mm	Inches	mm
.004	0.10	.117	2.97
.006	0.15	.127	3.23
.010	0.25	.290	7.37
.015	0.38	.310	7.87
.019	0.48	.324	8.23
.027	0.69	.336	8.53
.033	0.84	.405	10.29
.045	1.14	.415	10.54
.055	1.40	.692	17.58
.097	2.46	.708	17.98

FIGURE 1. Case outlines - Continued.

Case N



Symbol	Millimeters		Inches	
	Min	Max	Min	Max
A2	9.02	10.29	.355	.405
b	0.41	0.58	.016	.023
b2	0.89	1.14	.035	.045
c	0.20	0.38	.008	.015
e	1.14	1.40	.045	.055
eA	2.16	2.92	.085	.115
D	26.29	27.05	1.035	1.065
E	2.54	3.30	.100	.130
L	3.18	5.08	.125	.200
L1	0.38	1.27	.015	.050

Figure 1. Case outlines - Continued.

Device types	01, 02, 03		
Case outlines	R, X, U M	Y, Z, T	N
Terminal number	Terminal symbol		
1	DQ1	DQ1	$\overline{OE}$
2	DQ2	DQ2	CAS
3	$\overline{W}$	$\overline{W}$	DQ3
4	RAS	RAS	DQ4
5	A9	A9	V_{SS}
6	A0	NP	DQ1
7	A1	NP	DQ2
8	A2	NP	$\overline{W}$
9	A3	A0	RAS
10	V_{CC}	A1	A9
11	A4	A2	A0
12	A5	A3	A1
13	A6	Vcc	A2
14	A7	A4	A3
15	$\overline{A8}$	A5	V_{CC}
16	$\overline{OE}$	A6	A4
17	CAS	A7	A5
18	DQ3	A8	A6
19	DQ4	NP	A7
20	V_{SS}	NP	A8
21	--	$\overline{NP}$	--
22	--	$\overline{OE}$	--
23	--	CAS	--
24	--	DQ3	--
25	--	DQ4	--
26	--	V_{SS}	--

NP=NO PIN
NC=NO CONNECT

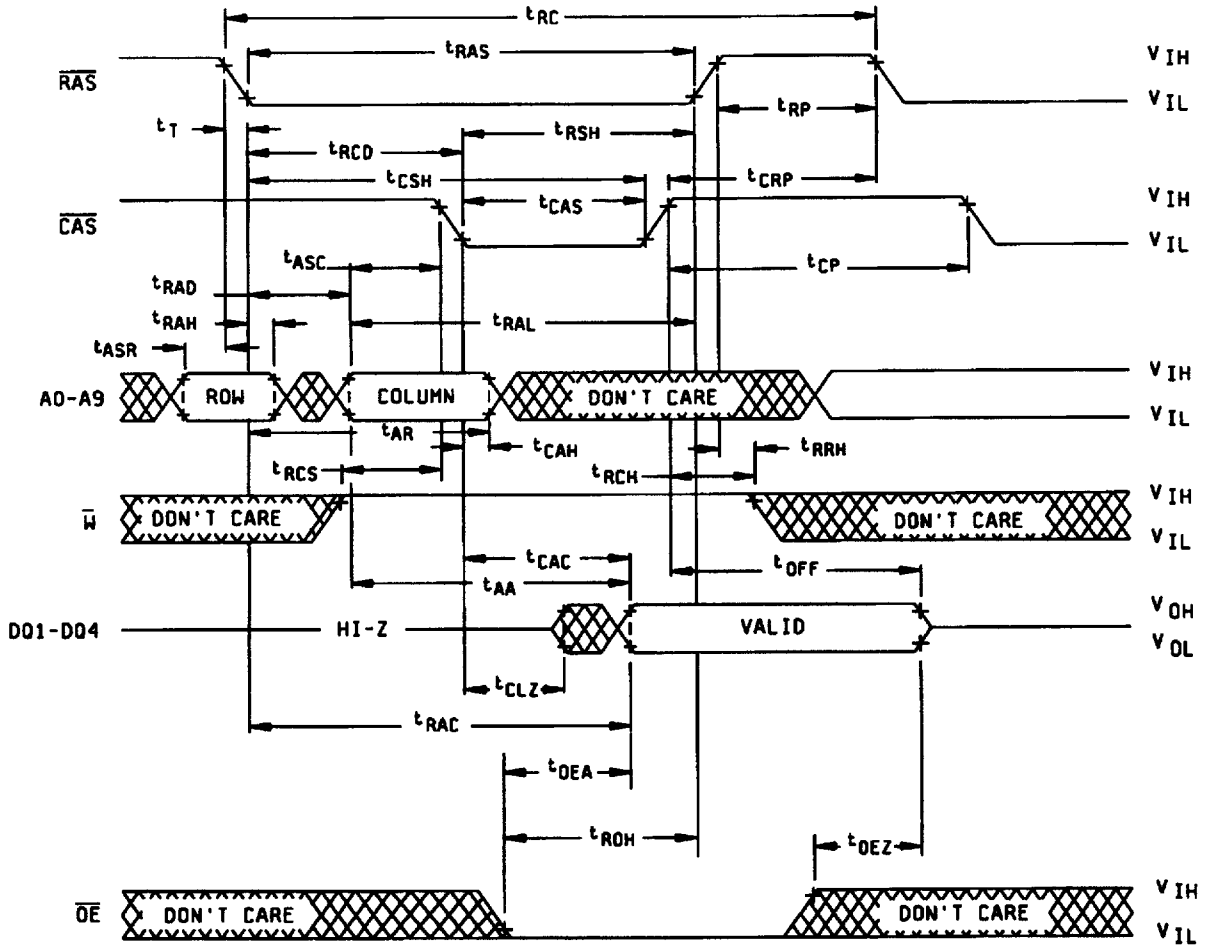
FIGURE 2. Terminal connections.

Operation	Inputs						Input/Output	
	$\overline{RAS}$	$\overline{CAS}$	$\overline{W}$	$\overline{OE}$	Row address	Column address	D	Q
Read	ACT	ACT	NAC	ACT	APD	APD	DNC	VLD
Write (early write)	ACT	ACT	ACT	DNC	APD	APD	VLD	DNC
Write (late write)	ACT	ACT	ACT	NAC	APD	APD	VLD	OPN
Read-modify-write	ACT	ACT	ACT	ACT	APD	APD	VLD	VLD
$\overline{RAS}$-only refresh	ACT	NAC	DNC	DNC	APD	DNC	DNC	OPN
Hidden refresh (read)	ACT	ACT	NAC	ACT	APD	APD	DNC	VLD
Hidden refresh (write)	ACT	ACT	ACT	DNC	APD	APD	VLD	DNC
$\overline{CAS}$ before $\overline{RAS}$ refresh	ACT	ACT	NAC	DNC	DNC	DNC	DNC	OPN
Standby	NAC	NAC	DNC	DNC	DNC	DNC	DNC	OPN

ACT = active
NAC = nonactive
DNC = don't care
VLD = valid
ILD = invalid
APD = applied
OPN = open

FIGURE 3. Truth table.

Read cycle timing



Note: Output may go from three-state to an invalid state prior to the specified access time.

FIGURE 4. Timing waveform diagrams.

Early write cycle timing

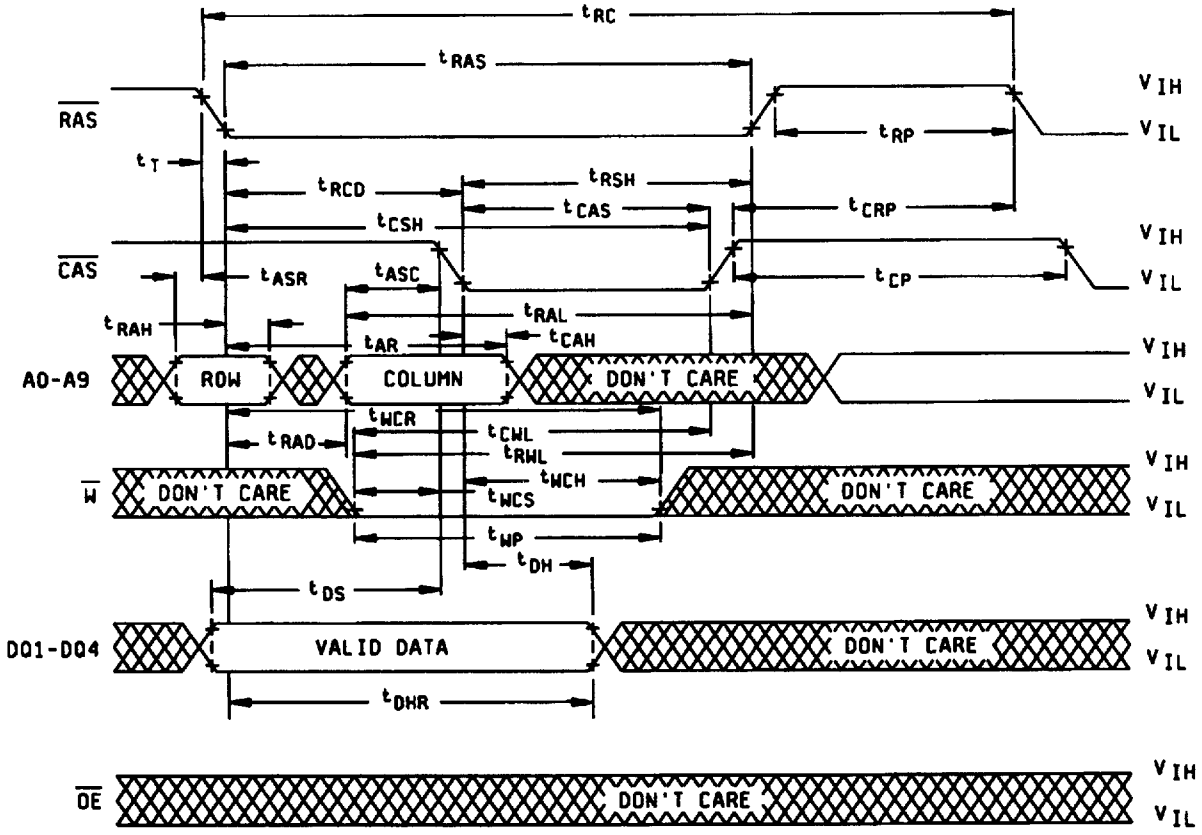


FIGURE 4. Timing waveform diagrams - Continued.

Write cycle timing

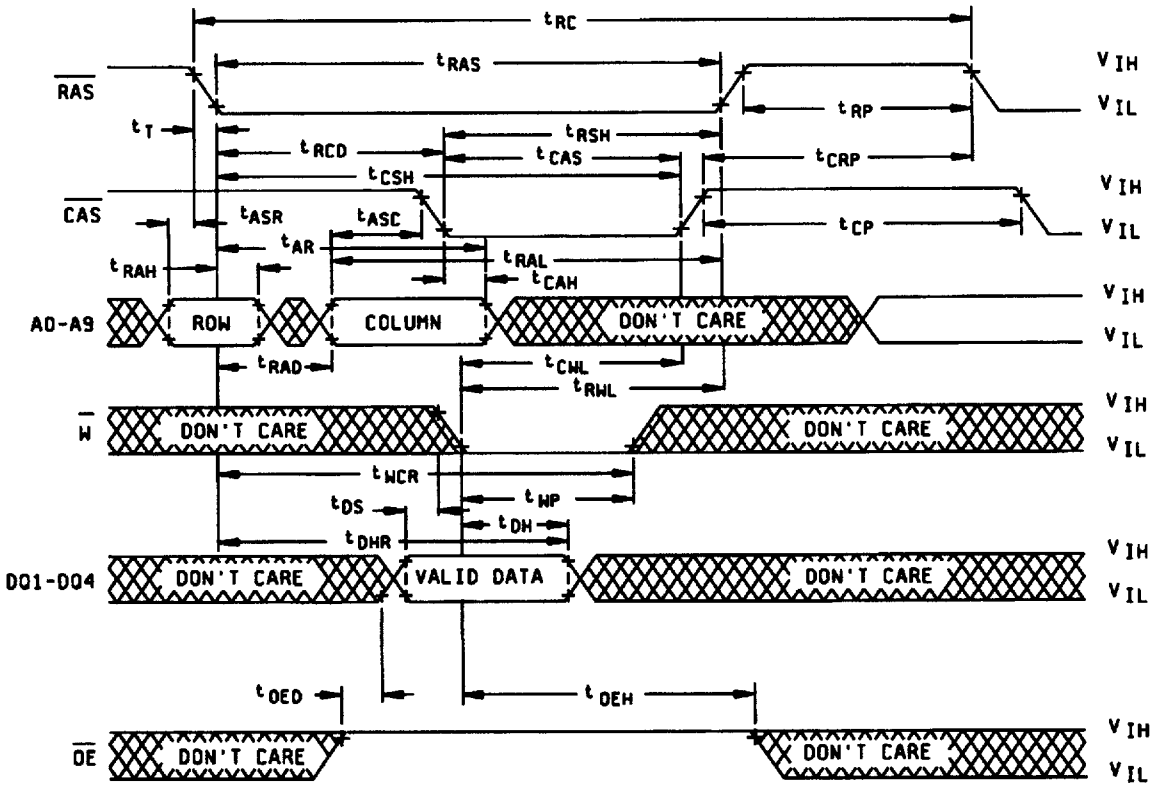
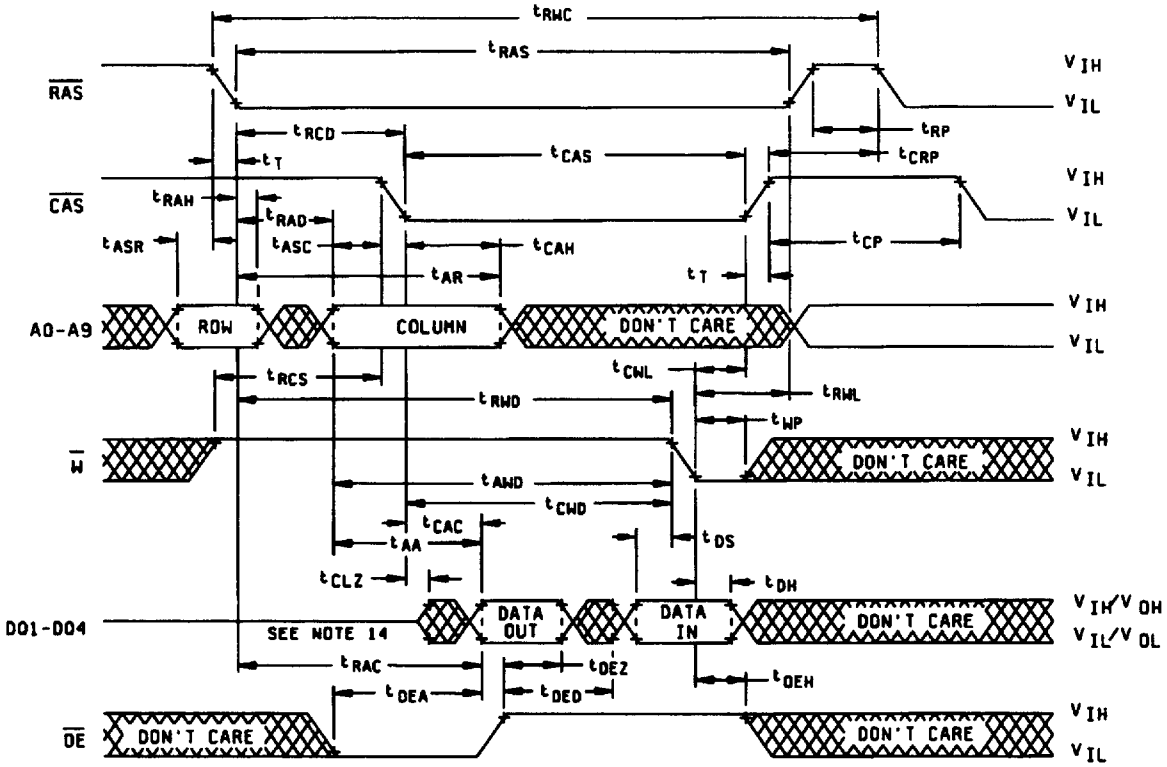


FIGURE 4. Timing waveform diagrams - Continued.

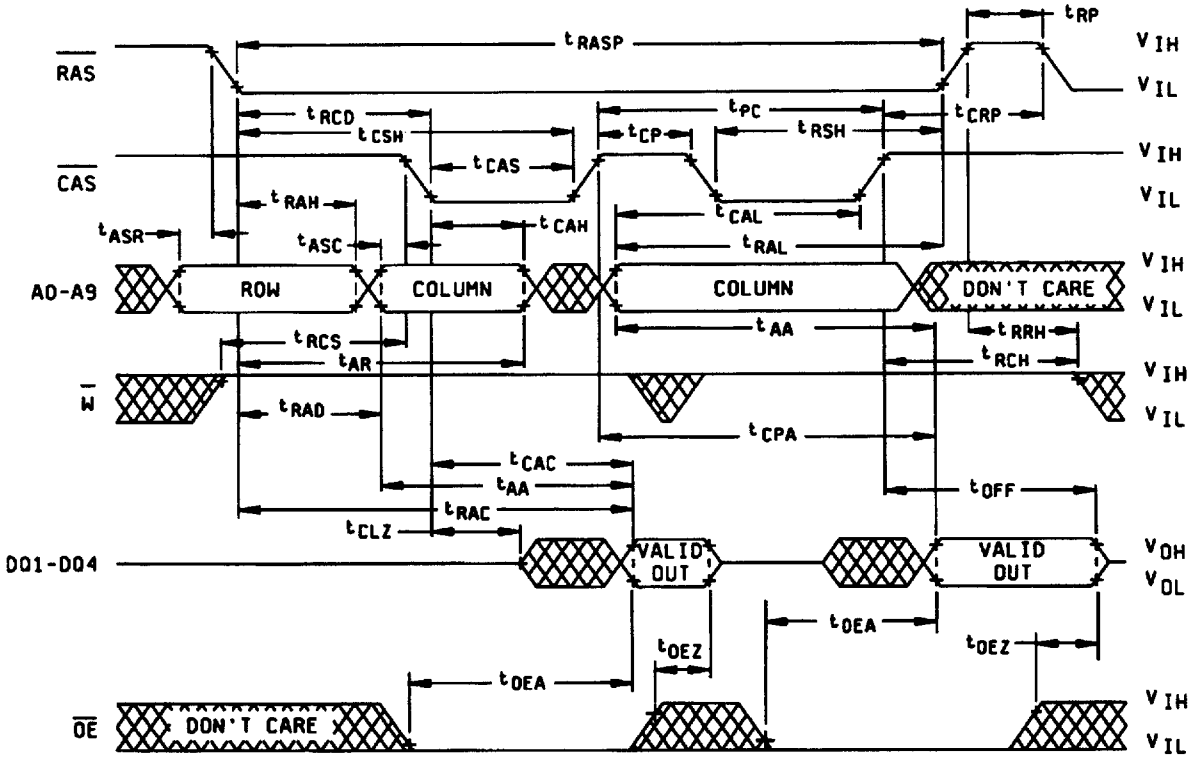
Read-write cycle timing



Note: Output may go from three-state to an invalid data state prior to the specified time.

FIGURE 4. Timing waveform diagrams - Continued.

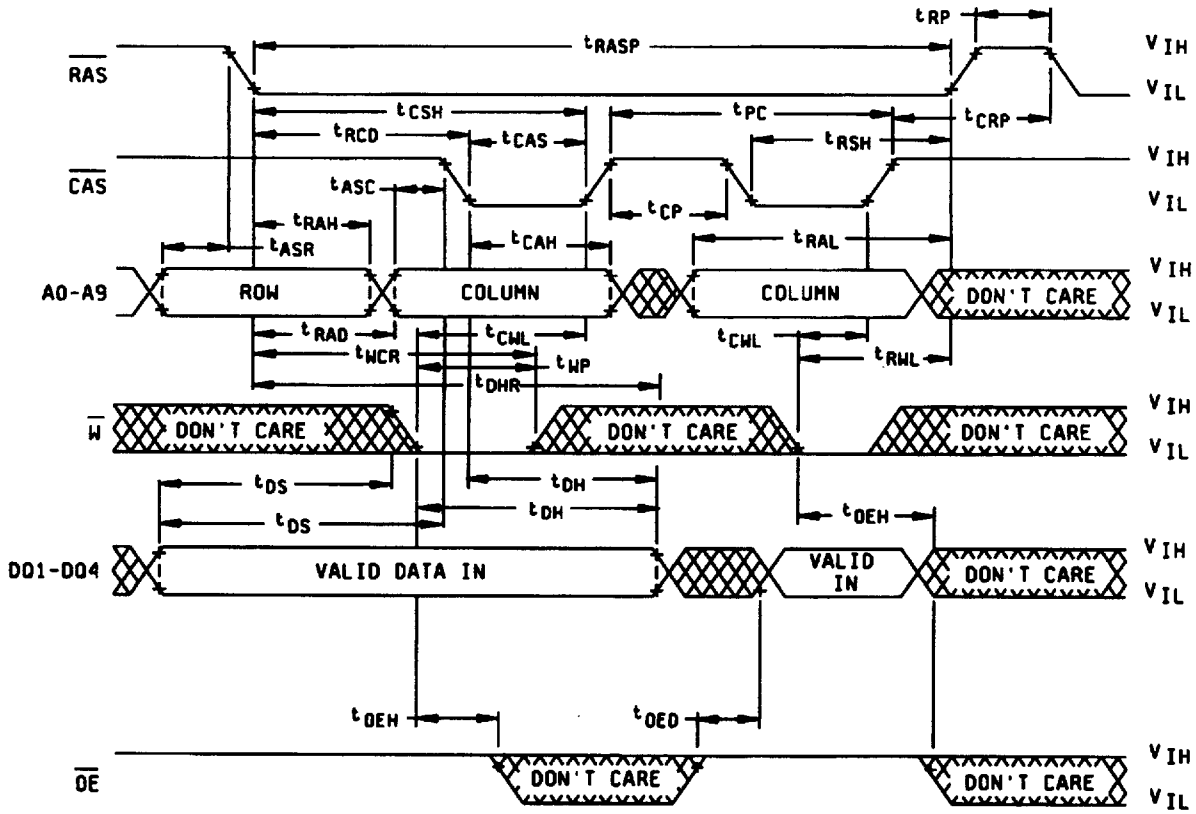
Enhanced page-mode read cycle timing



Notes: 1. Output may go from three-state to an invalid state prior to the specified access time.
2. Access time is t_{CPA} or t_{AA} dependent.

FIGURE 4. Timing waveform diagrams - Continued.

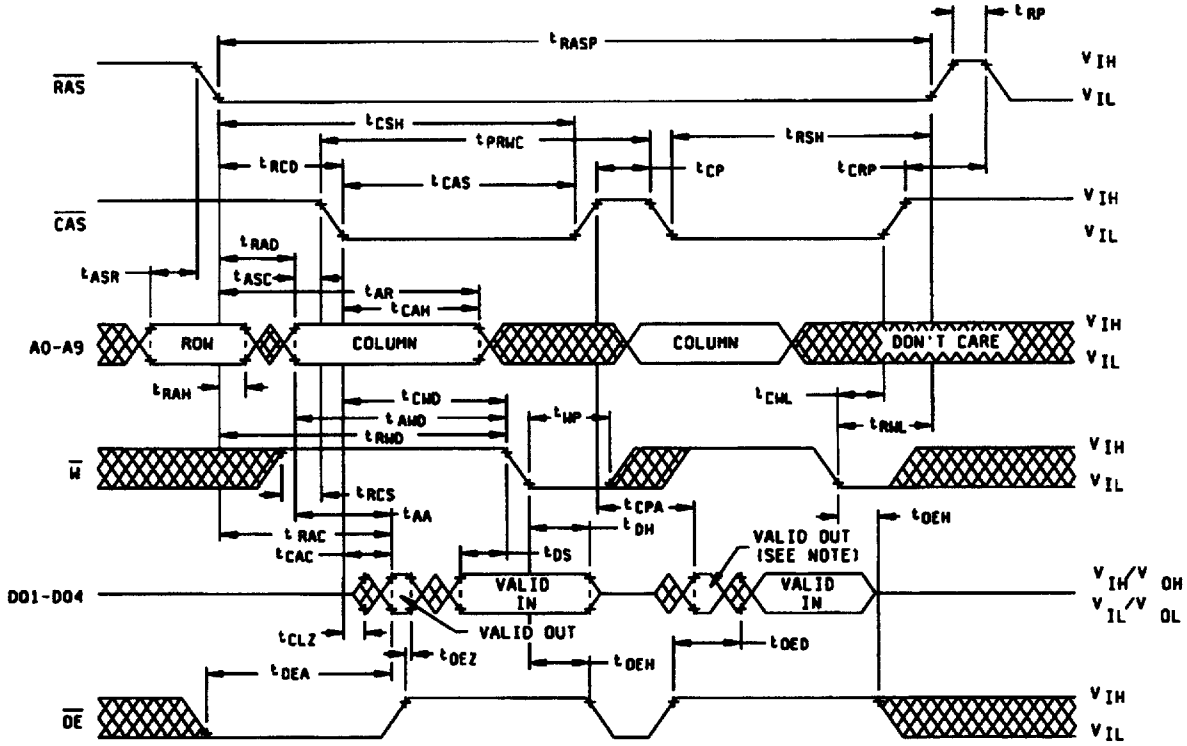
Enhanced page-mode write cycle timing



Notes: 1. t_{DS} and t_{DH} are referenced to $\overline{CAS}$ or $\overline{W}$, which ever occurs last.
2. A read cycle or a read-write cycle can be intermixed with a write cycle as long as read and read-write timing specifications are not violated.

FIGURE 4. Timing waveform diagrams - Continued.

Enhanced page-mode read-write cycle timing



Notes: 1. Output may go from three-state to an invalid data state prior to the specified time.
2. A read or write cycle can be intermixed with read-write cycles as long as the read and write timing specifications are not violated.

FIGURE 4. Timing waveform diagrams - Continued.

$\overline{\text{RAS}}$-only refresh timing

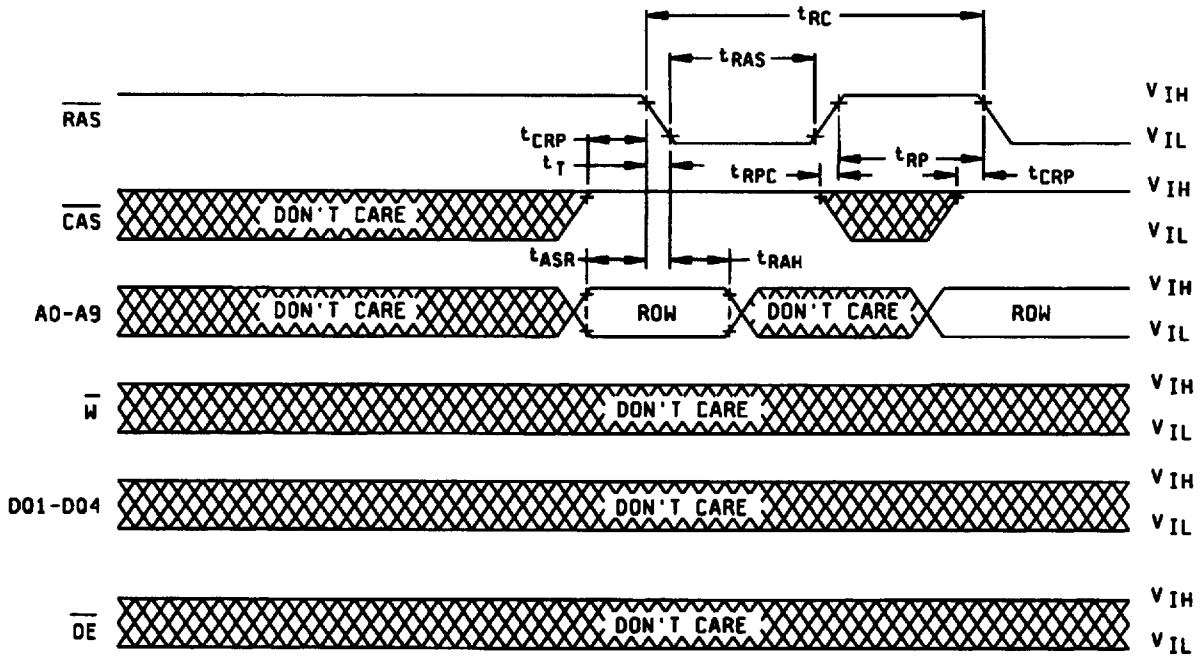


FIGURE 4. Timing waveform diagrams - Continued.

Automatic ($\overline{CAS}$-before-$\overline{RAS}$)
refresh cycle timing

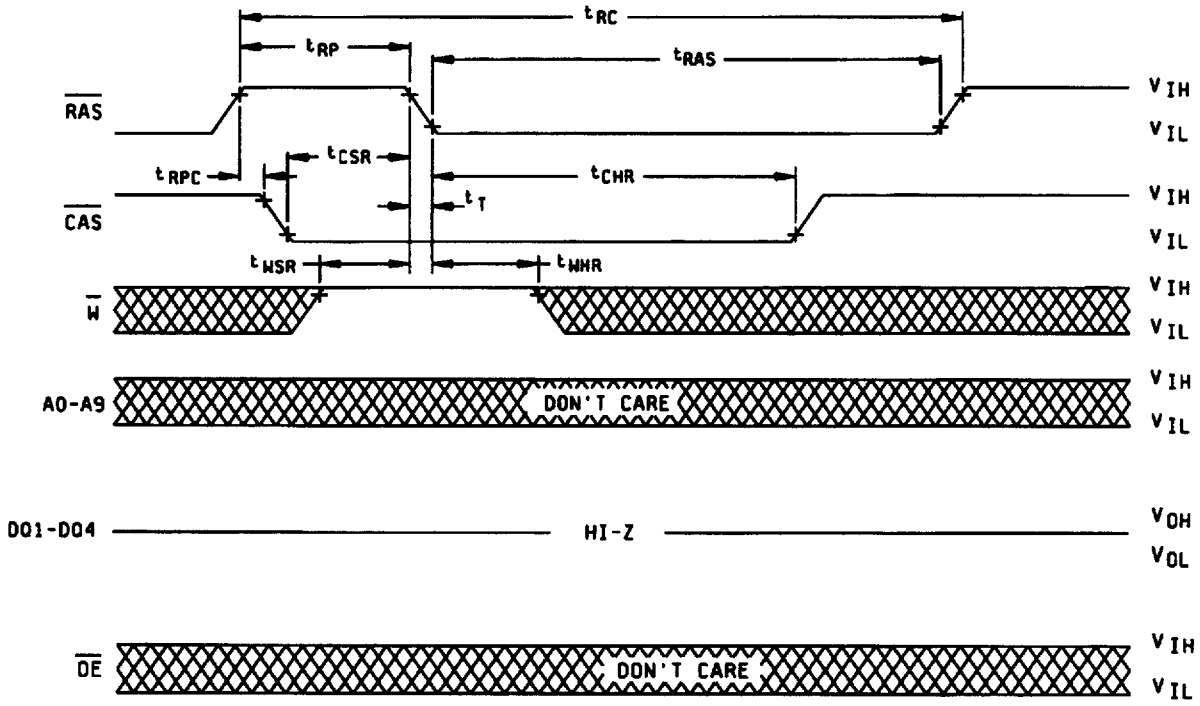


FIGURE 4. Timing waveform diagrams - Continued.

Hidden refresh cycle (read)

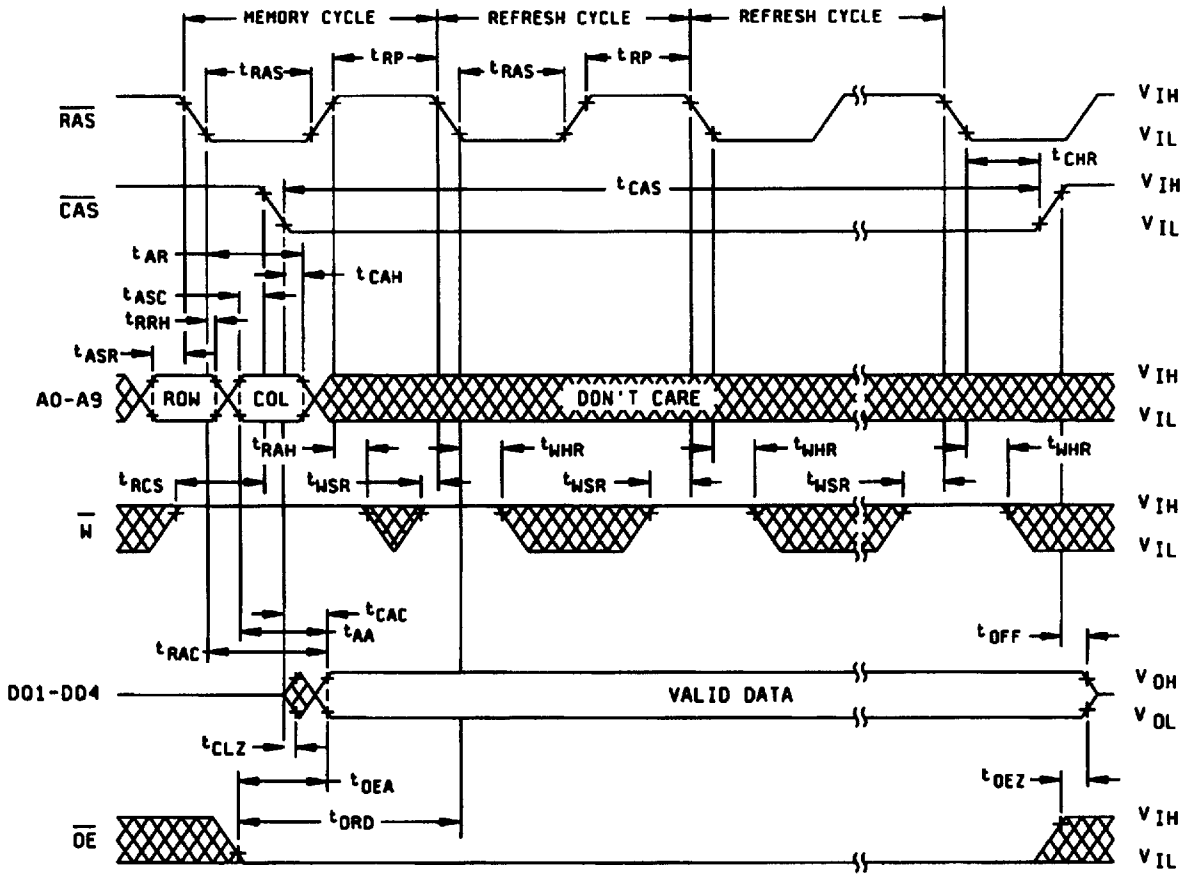


FIGURE 4. Timing waveform diagrams - Continued.

STANDARD MICROCIRCUIT DRAWING DEFENSE ELECTRONICS SUPPLY CENTER DAYTON, OHIO 45444	SIZE A		5962-90847
		REVISION LEVEL C	SHEET 32

Hidden refresh cycle (write)

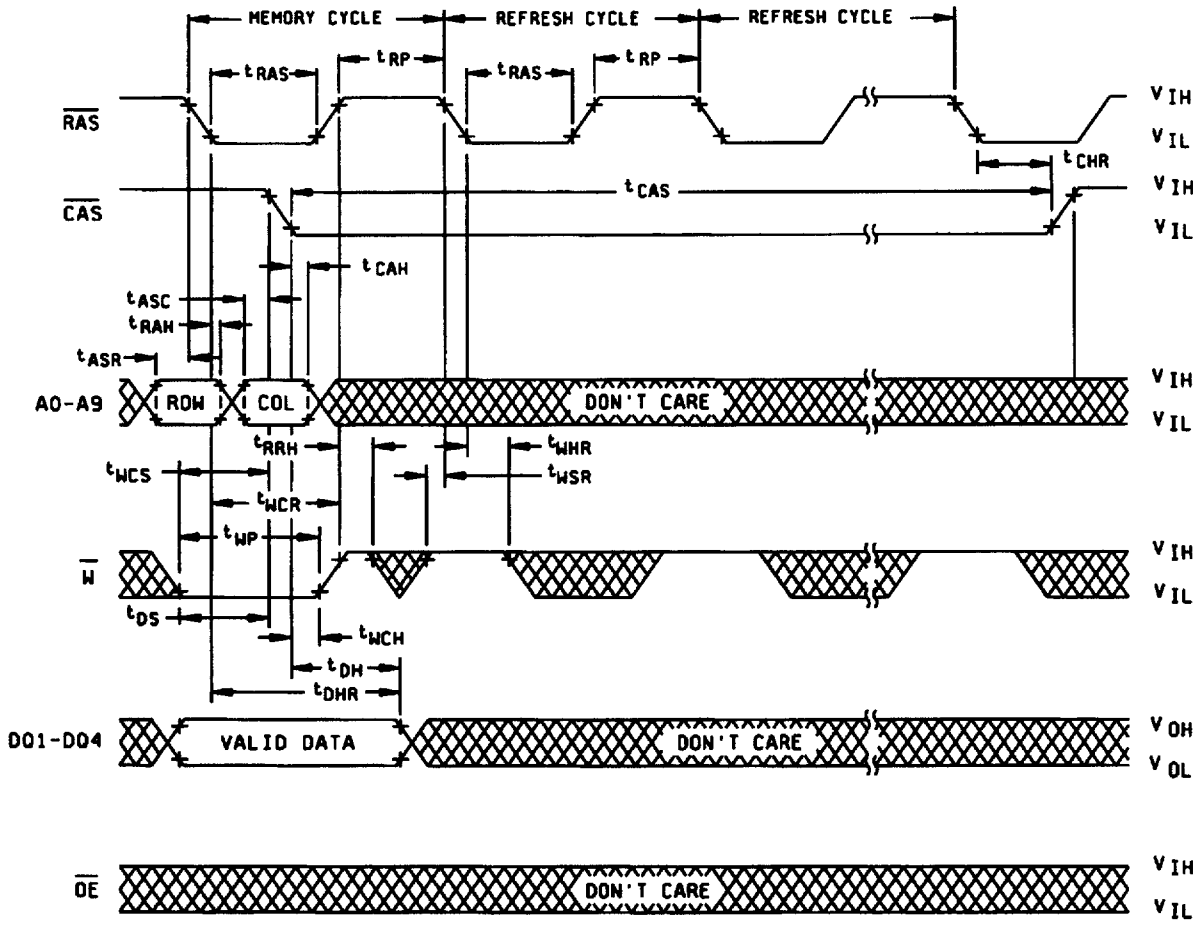
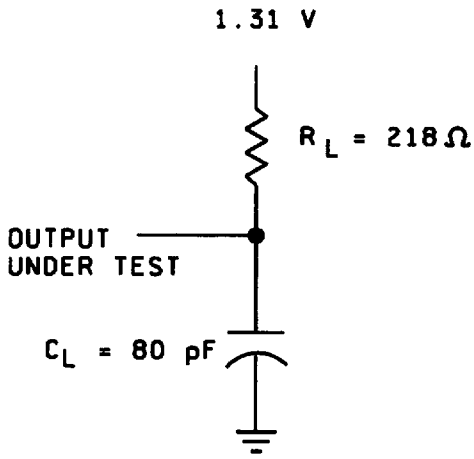
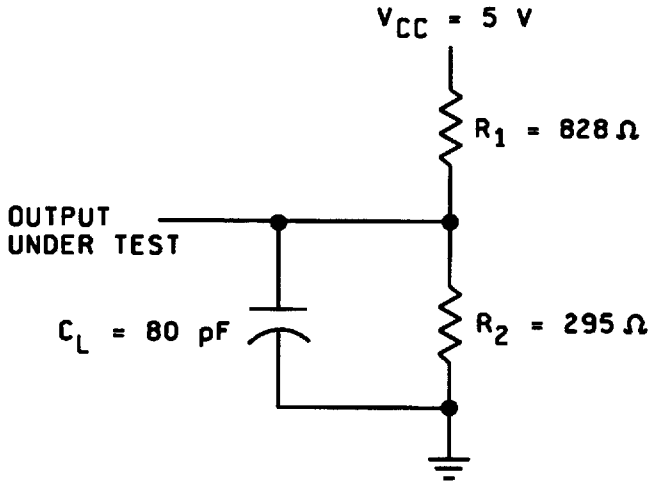


FIGURE 4. Timing waveform diagrams - Continued.



(A) LOAD CIRCUIT



(B) ALTERNATE LOAD CIRCUIT

FIGURE 5. Load circuits.

TABLE IIA. Electrical test requirements. 1/ 2/ 3/ 4/ 5/ 6/ 7/

Line no.	Test requirements	Subgroups (in accordance with MIL-STD-883, method 5005, table I)	Subgroups (in accordance with MIL-PRF-38535, table III)	
		Device class M	Device class Q	Device class V
1	Interim electrical parameters (see 4.2)			1,7,9
2	Static burn-in I and II (method 1015)	Not required	Not required	Required
3	Same as line 1			1*,7* Δ
4	Dynamic burn-in (method 1015)	Required	Required	Required
5	Same as line 1			1*,7* Δ
6	Final electrical parameters	1*,2,3,7*, 8A,8B,9,10, 11	1*,2,3,7*, 8A,8B,9,10, 11	1*,2,3,7*, 8A,8B,9, 10,11
7	Group A test requirements	1,2,3,4**,7, 8A,8B,9,10, 11	1,2,3,4**,7, 8A,8B,9,10, 11	1,2,3,4**,7, 8A,8B,9,10, 11
8	Group C end-point electrical parameters	2,3,7, 8A,8B	1,2,3,7, 8A,8B	1,2,3,7, 8A,8B,9, 10,11 Δ
9	Group D end-point electrical parameters	2,3, 8A,8B	2,3, 8A,8B	2,3, 8A,8B
10	Group E end-point electrical parameters	1,7,9	1,7,9	1,7,9

1/ Blank spaces indicate tests are not applicable.
2/ Any or all subgroups may be combined when using high-speed testers.
3/ Subgroups 7 and 8 functional tests shall verify the truth table.
4/ * indicates PDA applies to subgroup 1 and 7.
5/ ** see 4.4.1e.
6/ Δ indicates delta limit (see table IIB) shall be required where specified, and the delta values shall be computed with reference to the previous interim electrical parameters (see line 1).
7/ See 4.4.1d.

TABLE IIB. Delta limits at +25°C

Parameter 1/	Device types
	All
I_{CC2} standby	±10% of before value
I_{IH}, I_{IL}	±10% of before value
I_{OHZ}, I_{OLZ}	±10% of before value

1/ The above parameter shall be recorded before and after the required burn-in and life tests to determine the delta.

4.2.2 Additional criteria for device classes Q and V.

a. The burn-in test duration, test condition and test temperature, or approved alternatives shall be as specified in the device manufacturer's QM plan in accordance with MIL-PRF-38535. The burn-in test circuit shall be maintained under document revision level control of the device manufacturer's Technology Review Board (TRB) in accordance with MIL-PRF-38535 and shall be made available to the acquiring or preparing activity upon request. The test circuit shall specify the inputs, outputs, biases, and power dissipation, as applicable, in accordance with the intent specified in test method 1015 of MIL-STD-883.

b. Interim and final electrical test parameters shall be as specified in table IIA herein.

c. Additional screening for device class V beyond the requirements of device class Q shall be as specified in MIL-PRF-38535, appendix B.

4.3 Qualification inspection for device classes Q and V. Qualification inspection for device classes Q and V shall be in accordance with MIL-PRF-38535. Inspections to be performed shall be those specified in MIL-PRF-38535 and herein for groups A, B, C, D, and E inspections (see 4.4.1 through 4.4.4).

4.4 Conformance inspection. Technology conformance inspection for classes Q and V shall be in accordance with MIL-PRF-38535 including groups A, B, C, D, and E inspections and as specified herein except where option 2 of MIL-PRF-38535 permits alternate in-line control testing. Quality conformance inspection for device class M shall be in accordance with MIL-PRF-38535, appendix A and as specified herein. Inspections to be performed for device class M shall be those specified in method 5005 of MIL-STD-883 and herein for groups A, B, C, D, and E inspections (see 4.4.1 through 4.4.4).

4.4.1 Group A inspection.

a. Tests shall be as specified in table IIA herein.

b. Subgroups 5 and 6 of table I of method 5005 of MIL-STD-883 shall be omitted.

c. For device class M, subgroups 7 and 8 tests shall include verifying the functionality of the device. For device classes Q and V, subgroups 7 and 8 shall include verifying the functionality of the device; these tests shall have been fault graded in accordance with MIL-STD-883, test method 5012 (see 1.5 herein).

d. O/V (latch-up) tests shall be measured only for initial qualification and after any design or process changes which may affect the performance of the device. For device class M, procedures and circuits shall be maintained under document revision level control by the manufacturer and shall be made available to the preparing activity or acquiring activity upon request. For device classes Q and V, the procedures and circuits shall be under the control of the device manufacturer's TRB in accordance with MIL-PRF-38535 and shall be made available to the preparing activity or acquiring activity upon request. Testing shall be on all pins, on five devices with zero failures. Latch-up test shall be considered destructive. Information contained in JEDEC Standard number 17 may be used for reference.

e. Subgroup 4 (C_{IN} and C_{OUT} measurements) shall be measured only for initial qualification and after any process or design changes which may affect input or output capacitance. Capacitance shall be measured between the designated terminal and GND at a frequency of 1 MHz. Sample size is 15 devices with no failures, and all input and output terminals tested.

4.4.2 Group C inspection. The group C inspection end-point electrical parameters shall be as specified in table IIA herein. Delta limits shall apply only to subgroup 1 of group C inspection and shall consist of tests specified in table IIB herein.

4.4.2.1 Additional criteria for device class M. Steady-state life test conditions, method 1005 of MIL-STD-883:

a. Test condition D. The test circuit shall be maintained by the manufacturer under document revision level control and shall be made available to the preparing or acquiring activity upon request. The test circuit shall specify the inputs, outputs, biases, and power dissipation, as applicable, in accordance with the intent specified in test method 1005.

b. T_A = +125°C, minimum.

c. Test duration: 1,000 hours, except as permitted by method 1005 of MIL-STD-883.

4.4.2.2 Additional criteria for device classes Q and V. The steady-state life test duration, test condition and test temperature, or approved alternatives shall be as specified in the device manufacturer's QM plan in accordance with MIL-PRF-38535. The test circuit shall be maintained under document revision level control by the device manufacturer's TRB in accordance with MIL-PRF-38535 and shall be made available to the acquiring or preparing activity upon request. The test circuit shall specify the inputs, outputs, biases, and power dissipation, as applicable, in accordance with the intent specified in test method 1005 of MIL-STD-883.

4.4.3 Group D inspection. The group D inspection end-point electrical parameters shall be as specified in table IIA herein.

4.4.4 Group E inspection. Group E inspection is required only for parts intended to be marked as radiation hardness assured (see 3.5 herein).

a. End-point electrical parameters shall be as specified in table IIA herein.

b. For device classes Q and V, the devices or test vehicle shall be subjected to radiation hardness assured tests as specified in MIL-PRF-38535 for the RHA level being tested. For device class M, the devices shall be subjected to radiation hardness assured tests as specified in MIL-PRF-38535, appendix A for the RHA level being tested. All device classes must meet the postirradiation end-point electrical parameter limits as defined in table I at T_A = +25°C ±5°C, after exposure, to the subgroups specified in table IIA herein.

c. When specified in the purchase order or contract, a copy of the RHA delta limits shall be supplied.

4.5 Delta measurements for device class V. Delta measurements, as specified in table IIA, shall be made and recorded before and after the required burn-in screens and steady-state life tests to determine delta compliance. The electrical parameters to be measured, with associated delta limits are listed in table IIB. The device manufacturer may, at his option, either perform delta measurements or within 24 hours after burn-in perform final electrical parameter tests, subgroups 1, 7, and 9.

5. PACKAGING

5.1 Packaging requirements. The requirements for packaging shall be in accordance with MIL-PRF-38535 for device classes Q and V or MIL-PRF-38535, appendix A for device class M.

6. NOTES

6.1 Intended use. Microcircuits conforming to this drawing are intended for use for Government microcircuit applications (original equipment), design applications, and logistics purposes.

6.1.1 Replaceability. Microcircuits covered by this drawing will replace the same generic device covered by a contractor-prepared specification or drawing.

6.1.2 Substitutability. Device class Q devices will replace device class M devices.

6.2 Configuration control of SMD's. All proposed changes to existing SMD's will be coordinated with the users of record for the individual documents. This coordination will be accomplished in accordance with MIL-STD-973 using DD Form 1692, Engineering Change Proposal.

6.3 Record of users. Military and industrial users should inform Defense Electronics Supply Center when a system application requires configuration control and which SMD's are applicable to that system. DESC will maintain a record of users and this list will be used for coordination and distribution of changes to the drawings. Users of drawings covering microelectronic devices (FSC 5962) should contact DESC-EC, telephone (513) 296-6047.

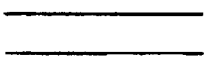
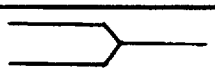
6.4 Comments. Comments on this drawing should be directed to DESC-EC, Dayton, Ohio 45444-5270, or telephone (513) 296-5377.

6.5 Abbreviations, symbols, and definitions. The abbreviations, symbols, and definitions used herein are defined in MIL-PRF-38535, MIL-HDBK-1331, and as follows:

C_{IN} C_{OUT}	Input and bidirectional output, terminal-to-GND capacitance.
GND	Ground zero voltage potential.
I_{CC}	Supply current.
I_{IL}	Input current low
I_{IH}	Input current high
T_C	Case temperature.
T_A	Ambient temperature
V_{CC}	Positive supply voltage.
V_{IC}	Positive input clamp voltage
O/V	Latch-up over-voltage
O/I	Latch-up over-current

6.5.1 Timing limits. The table of timing values shows either a minimum or a maximum limit for each parameter. Input requirements are specified from the external system point of view. Thus, address setup time is shown as a minimum since the system must supply at least that much time (even though most devices do not require it). On the other hand, responses from the memory are specified from the device point of view. Thus, the access time is shown as a maximum since the device never provides data later than that time.

6.5.2 Waveforms.

Waveform symbol	Input	Output
	MUST BE VALID	WILL BE VALID
	CHANGE FROM H TO L	WILL CHANGE FROM H TO L
	CHANGE FROM L TO H	WILL CHANGE FROM L TO H
	DON'T CARE ANY CHANGE PERMITTED	CHANGING STATE UNKNOWN
		HIGH IMPEDANCE

6.6 Sources of supply.

6.6.1 Sources of supply for device classes Q and V. Sources of supply for device classes Q and V are listed in QML-38535. The vendors listed in QML-38535 have submitted a certificate of compliance (see 3.6 herein) to DESC-EC and have agreed to this drawing.

6.6.2 Approved sources of supply for device class M. Approved sources of supply for class M are listed in MIL-HDBK-103. The vendors listed in MIL-HDBK-103 have agreed to this drawing and a certificate of compliance (see 3.6 herein) has been submitted to and accepted by DESC-EC.

APPENDIX

FUNCTIONAL ALGORITHMS

10. SCOPE

10.1 Scope. Functional algorithms are test patterns which define the exact sequence of events used to verify proper operation of a random access memory (RAM). Each algorithm serves a specific purpose for the testing of the device. It is understood that all manufacturers do not have the same test equipment; therefore, it becomes the responsibility of each manufacturer to guarantee that the test patterns described herein are followed as closely as possible, or equivalent patterns be used that serve the same purpose. Each manufacturer should demonstrate that this condition will be met. Algorithms shall be applied to the device in a topologically pure fashion. This appendix is a mandatory part of the specification. The information contained herein is intended for compliance.

20. APPLICABLE DOCUMENTS

This section is not applicable to this appendix.

30. ALGORITHMS

30.1 Algorithm A (pattern 1).

30.1.1 Output High Impedance (t_{off}). This pattern verifies the output buffer switches to high impedence (tri-state) within the specified t_{OFF} after the rise of CAS. It is performed in the following manner.

Step 1 Perform 8 pump cycles.
Step 2 Load address location with data.
Step 3 Raise CAS and read address location and guarantee $V_{OL} < V_{OUT} < V_{OH}$ after T_{OFF} delay.

30.2 Algorithm B (pattern 2).

30.2.1 Vcc Slew. This pattern indicates sense amplifier margin by slewing the supply voltage between memory writing and reading. It is performed in the following manner:

Step 1 Perform 8 pump cycles.
Step 2 Load memory with background data with V_{CC} at 4.5 V.
Step 3 Change V_{CC} to 5.5 V.
Step 4 Read data from memory.
Step 5 Write memory with data complement.
Step 6 Change V_{CC} to 4.5 V.
Step 7 Read data complement from memory.

30.3 Algorithm C (pattern 3).

30.3.1 March data. This pattern tests for address uniqueness and multiple selection. It is performed in the following manner:

Step 1 Perform 8 pump cycles.
Step 2 Write memory with data.
Step 3 Read location 0.
Step 4 Write location 0 with data complement.
Step 5 Repeat step 3 and 4 for all other locations in the memory (sequentially).
Step 6 Read data complement in maximum address location.
Step 7 Write data in maximum address location.
Step 8 Repeat step 6 and 7 for all other locations in the memory from maximum to minimum address.
Step 9 Read data in maximum address location.
Step 10 Write data complement in maximum address location.
Step 11 Repeat steps 9 and 10 for all other locations in the memory from maximum to minimum address.
Step 12 Read data complement from memory.

30.4 Algorithm D (pattern 4).

30.4.1 Refresh test (cell retention) +125°C only. This test is used to check the retention time of the memory cells. It is performed in the following manner:

Step 1 Perform 8 pump cycles.
Step 2 Load memory with background data.
Step 3 Pause T_{REF} (stop all clocks).
Step 4 Read memory with background data.
Step 5 Repeat steps 2, 3, and 4 with data complement.

30.5 Algorithm E (pattern 5).

30.5.1 Read-modify-write (RMW). This pattern verifies the Read-modify-write mode for the memory. It is performed in the following manner:

Step 1 Perform 8 pump cycles.
Step 2 Write memory with data.
Step 3 Read location 0 and write location 0 with data complement using RMW cycle.
Step 4 Repeat step 3 for all other locations in the memory.
Step 5 Repeat steps 3 and 4 using invert data.

30.6 Algorithm F (pattern 6).

30.6.1 Page mode. This pattern verifies the Page mode for the memory. It is performed in the following manner:

Step 1 Perform 8 pump cycles.
Step 2 Load first page of memory with background data using page mode cycle.
Step 3 Read first page of memory with data and load with data complement using page mode cycle.
Step 4 Read first page of memory with data complement and load with data using page mode cycle.
Step 5 Repeat steps 2, 3, and 4 for remaining memory locations.

30.6.2 Page mode (alternate). This pattern verifies the page mode for the memory. It is performed in the following manner:

Step 1 Perform 8 pump cycles.
Step 2 Write memory with data using row fast addressing.
Step 3 Read data from first page of memory and write it with data complement using page mode cycle.
Step 4 Repeat for rest of memory pages.
Step 5 Read data complement from memory using row fast addressing.
Step 6 Repeat steps 3, 4, and 5 using data.

30.7 Algorithm G (pattern 7).

30.7.1 $\overline{\text{CAS}}$-Before-$\overline{\text{RAS}}$ refresh test. This test is used to verify the functionality of the $\overline{\text{CAS}}$ before $\overline{\text{RAS}}$ mode of cell refreshing. It is done at +125°C only and is performed in the following manner:

Step 1 Perform 8 pump cycles.
Step 2 Load memory with background data for 16ms.
Step 3 Perform 1024 CAS-before-RAS cycles, while attempting to modify data.
Step 4 Repeat steps 2 and 3 until all address locations have been loaded.
Step 5 Read memory with data for 16 ms.
Step 6 Perform 1024 CAS-before-RAS cycles.
Step 7 Repeat steps 5 and 6 until all address locations have been loaded.
Step 8 Repeat steps 2 through 7 with data complement.

30.7.2 $\overline{\text{CAS}}$-Before-$\overline{\text{RAS}}$ refresh test (alternate). This test is used to verify the functionality of the $\overline{\text{CAS}}$ before RAS mode of cell refreshing. It is done at +125°C only and is performed in the following manner:

Step 1 Perform 8 pump cycles.
Step 2 Write memory data.
Step 3 Pause for t_{REF} (stop all clocks high).
Step 4 Perform 1024 CAS-before-RAS cycles.
Step 5 Repeat steps 3 and 4 for 250 ms.
Step 6 Read data from memory.
Step 7 Repeat steps 2 through 6 with data complement.

30.8 Algorithm H (pattern 8).

30.8.1 $\overline{\text{RAS}}$-Only refresh test. This test is used to verify the functionality of the $\overline{\text{RAS}}$-only mode of cell refreshing. It is done at +125°C only and is performed in the following manner:

Step 1 Perform 8 pump cycles.
Step 2 Load memory with background data for 16 ms.
Step 3 Perform 1024 RAS-only cycles.
Step 4 Repeat steps 2 and 3 until all address locations have been loaded.
Step 5 Read memory with data for 16ms.
Step 6 Perform 1024 RAS-only cycles.
Step 7 Repeat steps 5 and 6 until all address locations have been loaded.
Step 8 Repeat steps 2 through 7 with data complement.

30.8.2 $\overline{\text{RAS}}$-Only refresh test (cell retention) +125°C only (alternate). This test is used to verify the functionality of the RAS-only mode of cell refreshing. It is done at +125°C only and is performed in the following manner:

Step 1 Perform 8 pump cycles.
Step 2 Write memory with data.
Step 3 Pause for t_{REF} (stop all clocks high).
Step 4 Perform 1024 RAS-only cycles.
Step 5 Repeat steps 3 and 4 for 250 ms.
Step 6 Read data from memory.
Step 7 Repeat steps 2 through 6 with data complement.

30.9 Algorithm I (pattern 9).

30.9.1 Refresh test (periphery retention) +125°C only. This test is used to check the minimum periphery retention time and is optional at the discretion of the manufacturer. It is performed in the following manner:

Step 1 Perform 8 pump cycles.
Step 2 Write memory with data.
Step 3 Read data from memory.
Step 4 Pause for T_{REF} (stop all clocks high).
Step 5 Load memory with data complement.
Step 6 Read data complement from memory.
Step 7 Pause for T_{REF} (stop all clocks high).
Step 8 Write memory with data.
Step 9 Read data from memory.