REVISIONS			
LTR	DESCRIPTION	DATE (YR-MO-DA)	APPROVED

REV																								
SHEET																								
REV																								
SHEET	22	23	24	25	26	27	29																	
REV STATUS OF SHEETS	REV																							
	SHEET	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21		

PMIC N/A

STANDARDIZED MILITARY DRAWING

THIS DRAWING IS AVAILABLE FOR USE BY ALL DEPARTMENTS AND AGENCIES OF THE DEPARTMENT OF DEFENSE

AMSC N/A

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DRAWING APPROVAL DATE: 29 JANUARY 1991

REVISION LEVEL:

DEFENSE ELECTRONICS SUPPLY CENTER
DAYTON, OHIO 45444

MICROCIRCUIT, MEMORY, DIGITAL, CMOS
64K x 16 STATIC RANDOM ACCESS MEMORY
(SRAM), MONOLITHIC SILICON

SIZE	CAGE CODE	
A	67268	5962-90858

SHEET 1 OF 29

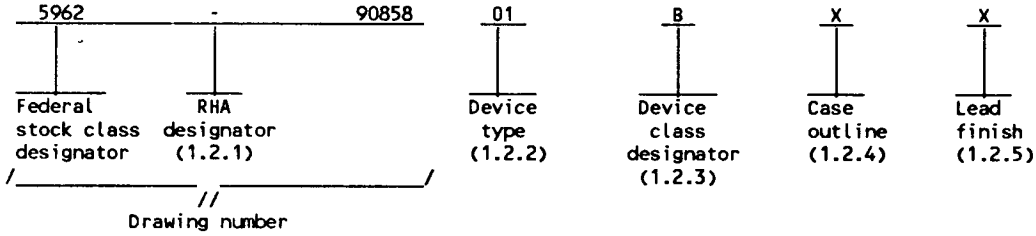
DESC FORM 193
SEP 87

* U.S. GOVERNMENT PRINTING OFFICE: 1987 — 748-129/60911

1. SCOPE

1.1 Scope. This drawing forms a part of a one part - one part number documentation system (see 6.6 herein). Two product assurance classes consisting of military high reliability (device classes B, Q, and M) and space application (device classes S and V), and a choice of case outlines and lead finishes are available and are reflected in the Part or Identifying Number (PIN). Device class M microcircuits represent non-JAN class B microcircuits in accordance with 1.2.1 of MIL-STD-883, "Provisions for the use of MIL-STD-883 in conjunction with compliant non-JAN devices". When available, a choice of radiation hardness assurance (RHA) levels are reflected in the PIN.

1.2 PIN. The PIN shall be as shown in the following example:



1.2.1 Radiation hardness assurance (RHA) designator. Device classes M, B, and S RHA marked devices shall meet the MIL-M-38510 specified RHA levels and shall be marked with the appropriate RHA designator. Device classes Q and V devices shall meet or exceed the electrical performance characteristics specified in table IA herein after exposure to the specified irradiation levels specified in the absolute maximum ratings herein and the RHA marked device shall be marked in accordance with MIL-I-38535. A dash (-) indicates a non-RHA device.

1.2.2 Device type(s). The device type(s) shall identify the circuit function as follows:

Device type	Generic number 1/	Circuit function	Access time
01		64K x 16 CMOS SRAM low power	100 ns
02		64K x 16 CMOS SRAM	100 ns
03		64K x 16 CMOS SRAM low power	85 ns
04		64K x 16 CMOS SRAM	85 ns
05		64K x 16 CMOS SRAM low power	70 ns
06		64K x 16 CMOS SRAM	70 ns
07		64K x 16 CMOS SRAM low power	55 ns
08		64K x 16 CMOS SRAM	55 ns

1.2.3 Device class designator. The device class designator shall be a single letter identifying the product assurance level as follows:

Device class	Device requirements documentation
M	Vendor self certification to the requirements for non-JAN class B microcircuits in accordance with 1.2.1 of MIL-STD-883
B or S	Certification and qualification to MIL-M-38510
Q or V	Certification and qualification to MIL-I-38535

1/ Generic numbers are listed on the Standardized Military Drawing Source Approval Bulletin at the end of this document and will also be listed in MIL-BUL-103.

1.2.4 Case outline(s). For device classes M, B, and S, case outline(s) shall meet the requirements in appendix C of MIL-M-38510 and as listed below. For device classes Q and V, case outline(s) shall meet the requirements of MIL-I-38535, appendix C of MIL-M-38510, and as listed below.

Outline letter	Case outline
Q	D-5 (40-lead, 2.096" x .620" x .225") dual-in-line package

1.2.5 Lead finish. The lead finish shall be as specified in MIL-M-38510 for classes M, B, and S or MIL-I-38535 for classes Q and V. Finish letter "X" shall not be marked on the microcircuit or its packaging. The "X" designation is for use in specifications when lead finishes A, B, and C are considered acceptable and interchangeable without preference.

1.3 Absolute maximum ratings. 2/ 3/

Supply voltage range	-0.5 V dc to +7.0 V dc
Input voltage range	-0.5 V dc to +6.0 V dc
Storage temperature range	-65°C to +150°C
Maximum power dissipation (P_D)	1.0 W
Lead temperature (soldering, 10 seconds)	+260°C
Thermal resistance, junction-to-case (Θ_{JC}):	
Case Q	See Mil-M-38510, appendix C
Junction temperature (T_J)	+150°C 4/

1.4 Recommended operating conditions. 2/

Supply voltage range (V_{CC})	4.5 V dc to 5.5 V dc
Supply voltage (V_{SS})	0.0 V dc
Input high voltage range (V_{IH})	2.2 V dc to V_{CC} + 0.5 V dc
Input low voltage range (V_{IL})	-0.5 V dc to +0.8 V dc
Case operating temperature range (T_C)	-55°C to +125°C

1.5 Digital logic testing for device classes Q and V.

Fault coverage measurement of manufacturing logic tests (MIL-STD-883, test method 5012)	XX percent 5/

2. APPLICABLE DOCUMENTS

2.1 Government specifications, standards, bulletin, and handbook. Unless otherwise specified, the following specifications, standards, bulletin, and handbook of the issue listed in that issue of the Department of Defense Index of Specifications and Standards specified in the solicitation, form a part of this drawing to the extent specified herein.

SPECIFICATIONS

MILITARY

MIL-M-38510	-	Microcircuits, General Specification for.
MIL-I-38535	-	Integrated Circuits, Manufacturing, General Specification for.

2/ All voltages referenced to V_{SS}, unless otherwise specified.
3/ Stresses above the absolute maximum rating may cause permanent damage to the device. Extended operation at the maximum levels may degrade performance and affect reliability.
4/ Maximum junction temperature shall not be exceeded except for allowable short duration burn-in screening conditions in accordance with method 5004 of MIL-STD-883.
5/ When a QML source exists, a value shall be provided.

STANDARDS

MILITARY

MIL-STD-480 - Configuration Control-Engineering Changes, Deviations and Waivers.
MIL-STD-883 - Test Methods and Procedures for Microelectronics.

BULLETIN

MILITARY

MIL-BUL-103 - List of Standardized Military Drawings (SMD's).

HANDBOOK

MILITARY

MIL-HDBK-780 - Standardized Military Drawings.

(Copies of the specifications, standards, bulletin, and handbook required by manufacturers in connection with specific acquisition functions should be obtained from the contracting activity or as directed by the contracting activity.)

2.2 Non-Government publications. The following document(s) form a part of this document to the extent specified herein. Unless otherwise specified, the issues of the documents which are DoD adopted are those listed in the issue of the DODISS cited in the solicitation. Unless otherwise specified, the issues of documents not listed in the DODISS are the issues of the documents cited in the solicitation.

ELECTRONICS INDUSTRIES ASSOCIATION (EIA)

JEDEC Standard No. 17 - A Standardized Test Procedure for the characterization of LATCH-UP in CMOS Integrated Circuits.

(Applications for copies should be addressed to the Electronics Industries Association, 2001 Pennsylvania Street, N.W., Washington, DC 20006.)

AMERICAN SOCIETY FOR TESTING AND MATERIALS (ASTM)

ASTM Standard F1192-88 - Standard Guide for the Measurement of Single Event Phenomena from Heavy Ion Irradiation of Semiconductor Devices.

(Applications for copies of ASTM publications should be addressed to the American Society for Testing and Materials, 1916 Race Street, Philadelphia, Pennsylvania 19103).

2.3 Order of precedence. In the event of a conflict between the text of this drawing and the references cited herein, the text of this drawing shall take precedence.

3. REQUIREMENTS

3.1 Item requirements. The individual item requirements for device class M shall be in accordance with 1.2.1 of MIL-STD-883, "Provisions for the use of MIL-STD-883 in conjunction with compliant non-JAN devices" and as specified herein. The individual item requirements for device classes B and S shall be in accordance with MIL-M-38510 and as specified herein. For device classes B and S, a full electrical characterization table for each device type shall be included in this SMD. The individual item requirements for device classes Q and V shall be in accordance with MIL-I-38535 and as specified herein.

3.2 Design, construction, and physical dimensions. The design, construction, and physical dimensions shall be as specified in MIL-M-38510 for device classes M, B, and S and MIL-I-38535 for device classes Q and V and herein.

3.2.1 Case outline(s). The case outline(s) shall be in accordance with 1.2.4 herein.

3.2 Design, construction, and physical dimensions. The design, construction, and physical dimensions shall be as specified in MIL-M-38510 for device classes M, B, and S and MIL-I-38535 for device classes Q and V and herein.

3.2.1 Case outline(s). The case outline(s) shall be in accordance with 1.2.4 herein.

3.2.2 Terminal connections. The terminal connections shall be as specified on figure 1.

3.2.3 Truth table. The truth table shall be as specified on figure 2.

3.2.4 Radiation exposure circuit. The radiation exposure circuit shall be as specified in 4.4.5e.

3.2.5 Functional tests. Various functional tests used to test this device are contained in appendix A. If the test patterns cannot be implemented due to test equipment limitations, alternate test patterns to accomplish the same results shall be submitted to DESC-ECS for device class M. For device classes B and S the test patterns shall be submitted to the qualifying activity for approval. For device classes Q and V the test patterns shall be submitted to DESC-ECS and shall also be under the control of the device manufacturer's technical review board (TRB) in accordance with MIL-I-38535.

3.3 Electrical performance characteristics and postirradiation parameter limits. Unless otherwise specified herein, the electrical performance characteristics and postirradiation parameter limits are as specified in table IA and shall apply over the full case operating temperature range.

3.4 Electrical test requirements. The electrical test requirements shall be the subgroups specified in table IIA. The electrical tests for each subgroup are defined in table IA.

3.5 Marking. The part shall be marked with the PIN listed in 1.2 herein. Marking for device class M shall be in accordance with MIL-STD-883 (see 3.1 herein). In addition, the manufacturer's PIN may also be marked as listed in MIL-BUL-103. Marking for device classes B and S shall be in accordance with MIL-M-38510. Marking for device classes Q and V shall be in accordance with MIL-I-38535.

3.5.1 Certification/compliance mark. The compliance mark for device class M shall be a "C" as required in MIL-STD-883 (see 3.1 herein). The certification mark for device classes B and S shall be a "J" or "JAN" as required in MIL-M-38510. The certification mark for device classes Q and V shall be a "QML" as required in MIL-I-38535.

3.6 Certificate of compliance. For device class M, a certificate of compliance shall be required from a manufacturer in order to be listed as an approved source of supply in MIL-BUL-103 (see 6.7.3 herein). For device classes Q and V, a certificate of compliance shall be required from a QML-38535 listed manufacturer in order to supply to the requirements of this drawing (see 6.7.2 herein). The certificate of compliance submitted to DESC-ECS prior to listing as an approved source of supply for this drawing shall affirm that the manufacturer's product meets, for device class M the requirements of MIL-STD-883 (see 3.1 herein), or for device classes Q and V, the requirements of MIL-I-38535 and the requirements herein.

3.7 Certificate of conformance. A certificate of conformance as required for device class M in MIL-STD-883 (see 3.1 herein) or device classes B and S in MIL-M-38510 or for device classes Q and V in MIL-I-38535 shall be provided with each lot of microcircuits delivered to this drawing.

3.8 Notification of change for device class M. For device class M, notification to DESC-ECS of change of product (see 6.2 herein) involving devices acquired to this drawing is required for any change as defined in MIL-STD-480.

3.9 Verification and review for device class M. For device class M, DESC, DESC's agent, and the acquiring activity retain the option to review the manufacturer's facility and applicable required documentation. Offshore documentation shall be made available onshore at the option of the reviewer.

TABLE IA. Electrical performance characteristics.

Test	Symbol	Conditions $-55°C \le T_C \le +125°C$ $V_{SS} = 0$ V; 4.5 V $\le V_{CC} \le 5.5$ V unless otherwise specified	Group A subgroups (Test method)	Device types	Limits		Unit
					Min	Max	
Output high voltage	V_{OH}	$I_{OH} = -4.0$ mA, $V_{CC} = 4.5$ V $V_{IL} = 0.8$ V, $V_{IH} \ge 2.2$ V	1, 2, 3 (3006)	All	2.4		V
Output low voltage	V_{OL}	$I_{OL} = 8.0$ mA, $V_{CC} = 4.5$ V $V_{IL} = 0.8$ V, $V_{IH} = 2.2$ V	1, 2, 3 (3007)	All		0.4	V
Input high voltage	V_{IH}	$V_{CC} = 5.5$ V	1, 2, 3 (3008)	All	2.2	6.0	V
Input low voltage	V_{IL}	$V_{CC} = 4.5$ V	1, 2, 3 (3008)	All	-0.5	0.8	V
High level input current	I_{IH}	$V_{CC} = 5.5$ V, $V_{IN} = 5.5$ V	1, 2, 3 (3010)	All		10	µA
Low level input current	I_{IL}	$V_{CC} = 5.5$ V, $V_{IN} = 0.0$ V	1, 2, 3 (3009)	All	-10		µA
High impedance output leakage current	I_{OZH}	$V_{CC} = 5.5$ V, $V_O = 5.5$ V $V_{IL} = 0.0$ V, $V_{IH} = 5.0$ V $V_{IH} \le \overline{OE} \le V_{CC}$	1, 2, 3 (3021)	All		10	µA
	I_{OZL}	$V_{CC} = 5.5$ V, $V_O = 0.0$ V $V_{IL} = 0.0$ V, $V_{IH} = 5.0$ V $V_{IH} \le \overline{OE} \le V_{CC}$	1, 2, 3 (3020)		-10		
Operating supply current	I_{CC1}	$V_{CC} = 5.5$ V, $\overline{CE} = V_{IL}$ max $\overline{OE}$ and $\overline{WE} = V_{IH}$ $f = 1/t_{AVAV}$ 1/	1, 2, 3 (3005)	01,03, 05,07		160	mA
				02,04, 06,08		175	
Standby supply current TTL Inputs	I_{CC2}	$V_{CC} = 5.5$ V, $\overline{CE} = V_{IH}$ $f = 0$ Inputs=V_{IH} or V_{IL}	1, 2, 3 (3005)	01,03, 05,07		10	mA
				02,04, 06,08		20	
Standby supply current CMOS Inputs	I_{CC3}	$V_{CC} = 5.5$ V, $f = 0$ Hz $\overline{CE}$, $\overline{UB}$, $\overline{LB} \ge V_{CC}-0.2$ V Inputs =0V+/-.2V or VCC+/-.2V	1, 2, 3 (3005)	All		6	mA

See footnotes at end of table.

TABLE IA. Electrical performance characteristics - Continued.

Test	Symbol	Conditions $-55°C \le T_C \le +125°C$ $V_{SS} = 0$ V; 4.5 V $\le V_{CC} \le 5.5$ V unless otherwise specified	Group A subgroups	Device types	Limits		Unit
					Min	Max	
Data retention current	I_{CC4}	$\overline{CE}$, $\overline{UB}$, $\overline{LB} \ge 2.0 \pm 0.2$ V $V_{CC} = 2.0$ V, f = 0	1, 2, 3 (3005)	01,03, 05,07		1.5	mA
Input capacitance 1/ (A0 - A15)	C_{IN}	$V_{IN} = 0$ V, $t_{AVAV} = 1.0$ MHz $T_C = +25°C$, see 4.4.1e	4 (3012)	All		15.0	pF
Input capacitance 1/ ($\overline{CE}$, $\overline{WE}$, $\overline{OE}$, $\overline{UB}$, $\overline{LB}$)	C_{CLK}	$V_{OUT} = 0$ V, $t_{AVAV} = 1.0$ MHz $T_C = +25°C$, see 4.4.1e	4 (3012)	All		20.0	pF
Output capacitance 1/	C_{OUT}	$V_{OUT} = 0$ V, $t_{AVAV} = 1.0$ MHz $T_C = +25°C$, see 4.4.1e	4 (3012)	All		20.0	pF
Functional tests		See 4.4.1c	7, 8 (3014)	All			
Read cycle time	t_{AVAV}	See figures 3 and 4, as applicable	9, 10, 11 (3003)	01,02	100		ns
				03,04	85		
				05,06	70		
				07,08	55		
Address access time	t_{AVQV}		9, 10, 11 (3003)	01,02		100	ns
				03,04		85	
				05,06		70	
				07,08		55	
Chip enable access time	t_{ELQV}		9, 10, 11 (3003)	01,02		100	ns
				03,04		85	
				05,06		70	
				07,08		55	
Output enable to output valid	t_{OLQV}		9, 10, 11 (3003)	01,02		50	ns
				03,04		35	
				05,06		25	
				07,08		20	

See footnotes at end of table.

TABLE IA. Electrical performance characteristics - Continued.

Test	Symbol	Conditions $-55°C \le T_C \le +125°C$, $V_{SS} = 0$ V; 4.5 V $\le V_{CC} \le 5.5$ V unless otherwise specified	Group A subgroups	Device types	Limits		Unit
					Min	Max	
Output hold after address change	t_{AVQX}	See figures 3 and 4, as applicable	9, 10, 11 (3003)	All	5		ns
Chip enable to output in low Z 1/ 2/	t_{ELQX}		9, 10, 11 (3003)	All	5		ns
Chip disable to output in high Z 1/ 2/	t_{EHQZ}		9, 10, 11 (3003)	All		35	ns
Output enable to output in low Z 1/ 2/	t_{OLQX}		9, 10, 11 (3003)	All	0		ns
Output disable to output in high Z 1/ 2/	t_{OHQZ}		9, 10, 11 (3003)	All		35	ns
Write cycle time	t_{AVAV}		9, 10, 11 (3003)	01,02	100		ns
				03,04	85		
				05,06	70		
				07,08	55		
Write pulse width	t_{WLWH}		9, 10, 11 (3003)	01,02	45		ns
				03,04	40		
				05,06	35		
				07,08	35		
Write enable to output disable 1/ 2/	t_{WLQZ}		9, 10, 11 (3003)	All	0	35	ns
Output active after end of write 1/ 2/	t_{WHQV}		9, 10, 11 (3003)	All	5		ns
Chip select to end of write	t_{ELWH}		9, 10, 11 (3003)	01-04	75		ns
				05,06	60		
				07,08	45		

See footnotes at end of table.

TABLE IA. Electrical performance characteristics - Continued.

Test	Symbol	Conditions $-55°C \le T_C \le +125°C$, $V_{SS} = 0$ V; 4.5 V $\le V_{CC} \le 5.5$ V unless otherwise specified	Group A subgroups	Device types	Limits Min	Limits Max	Unit
Data setup to end of write	t_{DVWH} t_{DVEH}	See figures 3 and 4, as applicable	9, 10, 11 (3003)	01,02	40		ns
				03,04	35		
				05,06	30		
				07,08	25		
Data hold after end of write	t_{WHDX} t_{EHDX}		9, 10, 11 (3003)	All	3		ns
Address setup to end of write	t_{AVWH}		9, 10, 11 (3003)	01,02	75		ns
				03,04	75		
				05,06	60		
				07,08	45		
Address setup to beginning of write	t_{AVWL} t_{AVEL}		9, 10, 11 (3003)	All	0		ns
Address hold after end of write	t_{WHAX} t_{EHAX}		9, 10, 11 (3003)	All	5		ns
UB/LB byte enable access time	t_{AB}		9, 10, 11 (3003)	01,02		100	ns
				03,04		85	
				05,06		70	
				07,08		55	
UB/LB byte enable to end of write	t_{BW}		9, 10, 11 (3003)	01-04	75		ns
				05,06	60		
				07,08	45		
UB/LB byte enable to output in low Z 2/	t_{BLZ}		9, 10, 11 (3003)	All	5		ns
UB/LB byte enable to output in high Z 2/	t_{BHZ}		9, 10, 11 (3003)	All	0	35	ns

See footnotes at end of table.

TABLE IA. Electrical performance characteristics - Continued.

Test	Symbol	Conditions $-55°C \le T_C \le +125°C$ $V_{SS} = 0$ V; 4.5 V $\le V_{CC} \le 5.5$ V unless otherwise specified	Group A subgroups	Device types	Limits Min	Limits Max	Unit
Retention time 1/	t_{CDR}	See figures 3 and 4, as applicable	9, 10, 11 (3003)	All	0		ns
Operation recovery time 1/	t_R		9, 10, 11 (3003)	01,02	100		ns
				03,04	85		
				05,06	70		
				07,08	55		

1/ This parameter is tested initially and after any design or process change which could affect this parameter, and therefore shall be guaranteed to the limits specified in table IA.

2/ Transition is measured ±500 mV from steady state voltage.

Table IB. Single Event Phenomena (SEP) test limits. 1/ 2/

Device type	Temperature (±10°C)	Memory pattern	V_{CC} = 4.5 V Effective LET no upsets (MeV/(mg/cm^2))	V_{CC} = 4.5 V Maximum device cross section (cm^2) (LET =)	Bias for latchup test V_{CC} = 5.5 V no latchup LET

1/ This table blank, table will be filled in when a qualified vendor exsists.
2/ For SEP test conditions see 4.4.5 herein.

TABLE IIA. Electrical test requirements. 1/ 2/ 3/ 4/ 5/ 6/

Line no.	Test requirements	Subgroups (per method 5005 table I)			Subgroups (per MIL-I-38535, table III)	
		Device class M	Device class B	Device class S	Device class Q	Device class V
1	Interim electrical parameters (see 4.2)		1,7,9 or 2,8A,10	1,7,9 or 1,2,8A,10	1,7,9 or 2,8A,10	1,7,9 or 1,2,8A,10
2	Static burn-in I method 1015	Not required	Not required	Required	Not required	Required
3	Same as line 1			1*,7* △		1*,7* △
4	Dynamic burn-in (method 1015)	Required	Required	Required	Required	Required
5	Same as line 1			1*,7* △		1*,7* △
6	Final electrical parameters	1*,2,3,7*, 8A,8B,9,10, 11	1*,2,3,7*, 8A,8B,9,10, 11	1*,2,3,7*, 8A,8B,9, 10,11	1*,2,3,7*, 8A,8B,9,10, 11	1*,2,3,7*, 8A,8B,9, 10,11
7	Group A test requirements	1,2,3,4**, 7,8A,8B,9, 10,11	1,2,3,4**, 7,8A,8B,9, 10,11	1,2,3,4**, 7,8A,8B,9, 10,11	1,2,3,4**, 7,8A,8B,9, 10,11	1,2,3,4**, 7,8A,8B,9, 10,11
8	Group B end-point electrical parameters			1,2,3,7, 8A,8B,9, 10,11 △		1,2,3,7, 8A,8B,9, 10,11 △
9	Group C end-point electrical parameters	2,3,7, 8A,8B	1,2,3,7, 8A,8B △		1,2,3,7, 8A,8B △	
10	Group D end-point electrical parameters	2,3,7, 8A,8B	2,3,7, 8A,8B	2,3,7, 8A,8B	2,3,7, 8A,8B	2,3,7, 8A,8B
11	Group E end-point electrical parameters	1, 7, 9	1, 7, 9	1, 7, 9	1, 7, 9	1, 7, 9

1/ Blank spaces indicate tests are not applicable.
2/ Any or all subgroups may be combined when using high-speed testers.
3/ Subgroups 7 and 8 functional tests shall verify the truth table.
4/ * indicates PDA applies to subgroups 1 and 7.
5/ ** see 4.4.1e.
6/ Δ indicates delta limit (see table IIC) shall be required where specified, and the delta values shall be computed with reference to the previous electrical parameters. See table IIC.

TABLE IIB. Additional screening for device class V.

Test	MIL-STD-883, test method	Lot requirement
Particle impact noise detection	2020	100%
Internal visual	2010, condition A or approved alternate	100%
Nondestructive bond pull	2023 or approved alternate	100%
Reverse bias burn-in	1015	100%
Burn-in	1015, total of 240 hours at +125°C	100%
Radiographic	2012	100%

TABLE IIC. Delta limits at +25°C.

Test 1/	Device types
	All
I_{CC3} standby	±10% of specified value in table IA
V_{OL}	±10% of specified value in table IA
V_{OH}	±10% of specified value in table IA
I_{IH}, I_{IL}	±10% of specified value in table IA
I_{OHZ}, I_{OLZ}	±10% of specified value in table IA

1/ The above parameter shall be recorded before and after the required burn-in and life tests to determine the delta Δ.

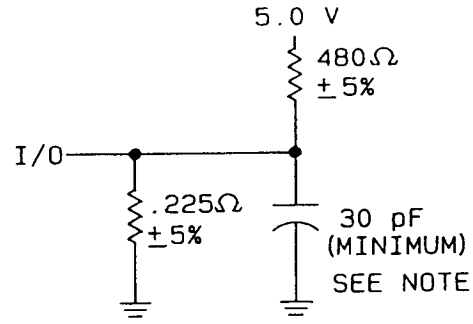
Device types	01 through 08	Device types	01 through 08
Case outline	Q	Case outline	Q
Terminal number	Terminal symbol	Terminal number	Terminal symbol
1	A_{15}	21	A_0
2	$\overline{CE}$	22	A_1
3	I/O_{15}	23	A_2
4	I/O_{14}	24	A_3
5	I/O_{13}	25	A_4
6	I/O_{12}	26	A_5
7	I/O_{11}	27	A_6
8	I/O_{10}	28	A_7
9	I/O_9	29	A_8
10	I/O_8	30	V_{SS}
11	V_{SS}	31	A_9
12	I/O_7	32	A_{10}
13	I/O_6	33	A_{11}
14	I/O_5	34	A_{12}
15	I/O_4	35	A_{13}
16	I/O_3	36	A_{14}
17	I/O_2	37	$\overline{LB}$
18	I/O_1	38	$\overline{UB}$
19	I/O_0	39	$\overline{WE}$
20	$\overline{OE}$	40	V_{CC}

FIGURE 1. Terminal connections.

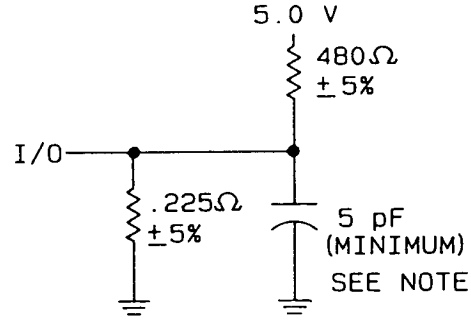
$\overline{UB}$	$\overline{LB}$	$\overline{CE}$	$\overline{WE}$	$\overline{OE}$	I/O	Function
H	H	L	X	X	High Z	Standby (I_{CC2})
X	X	H	X	X	High Z	Standby (I_{CC2})
$\geq V_{CC}$ -0.2 V	$\geq V_{CC}$ -0.2 V	$\geq V_{CC}$ -0.2 V	X	X	High Z	Standby (I_{CC3})
L	L	L	H	H	High Z	Output disable
L	L	L	H	L	Data out	Read
L	L	L	L	X	Data in	Write

H = High logic, "1" state; L = Low logic, "0" state.
X = logic don't care state; High Z = high impedance state.

FIGURE 2. Truth table.



Circuit A or equivalent



Circuit B or equivalent
for (t_{ELQX}, t_{OLQX}, t_{EHQZ}, t_{OHQZ}, t_{WLQZ}, t_{WHQX}, t_{BLZ}, t_{BHZ})

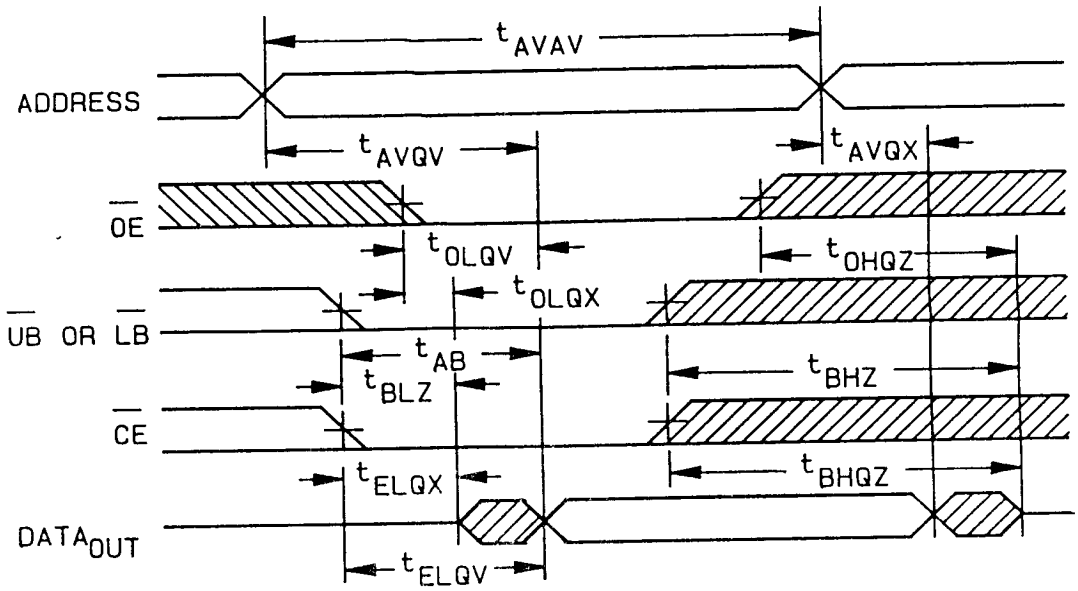
AC test conditions

Input pulse levels	GND to 3.0 V
Input rise and fall times	5 ns
Input timing reference levels	1.5 V
Output reference levels	1.5 V

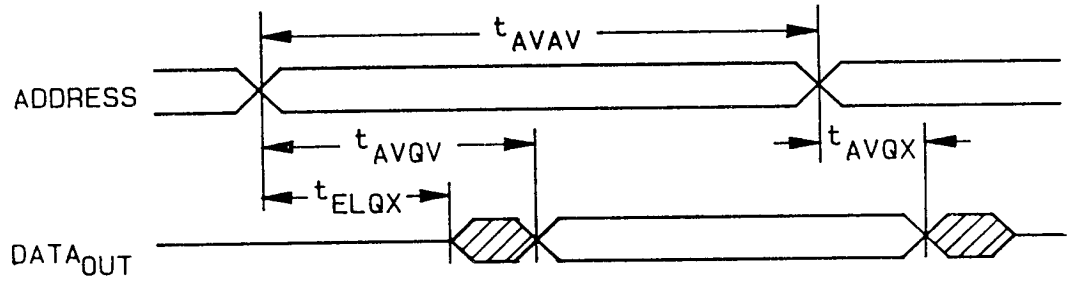
NOTE: Including scope and jig

FIGURE 3. Output load circuit.

TIMING WAVEFORM OF READ CYCLE NUMBER 1. (See note 1)



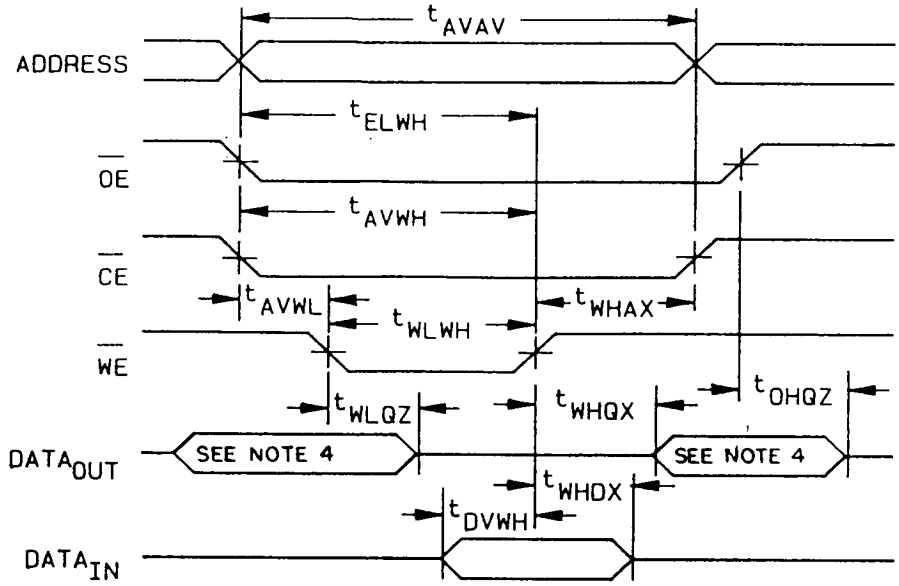
TIMING WAVEFORM OF READ CYCLE NUMBER 2. (See notes 1, 2, 3, and 4)



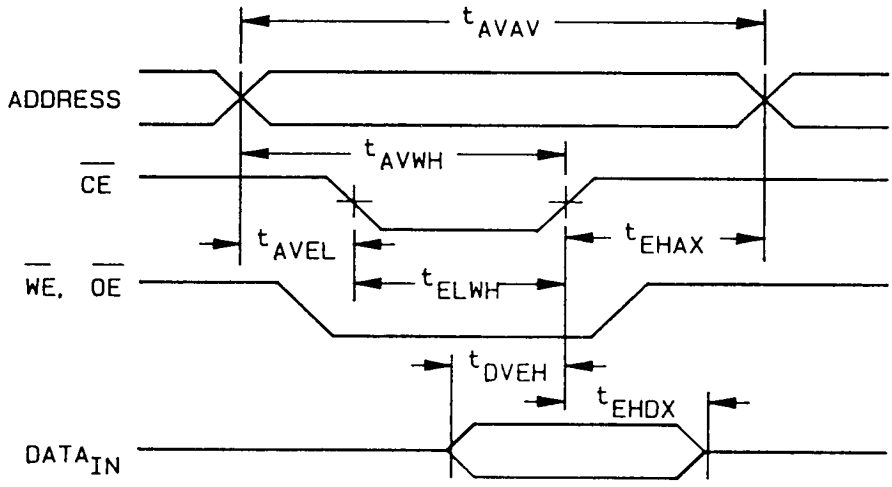
NOTES:
1. $\overline{WE}$ is high for Read cycles.
2. Device is continuosly selected, $\overline{CE}$ = V_{IL} and $\overline{UB}$, $\overline{LB}$ = V_{IL} for 16 outputs active.
3. $\overline{OE}$ = V_{IL}.
4. $\overline{UB}$ or $\overline{LB}$ = V_{IL}.

FIGURE 4. Timing waveforms.

TIMING WAVEFORM OF WRITE CYCLE NUMBER 1. ($\overline{WE}$ CONTROLLED TIMING). (See notes 1, 2, 3, and 6)



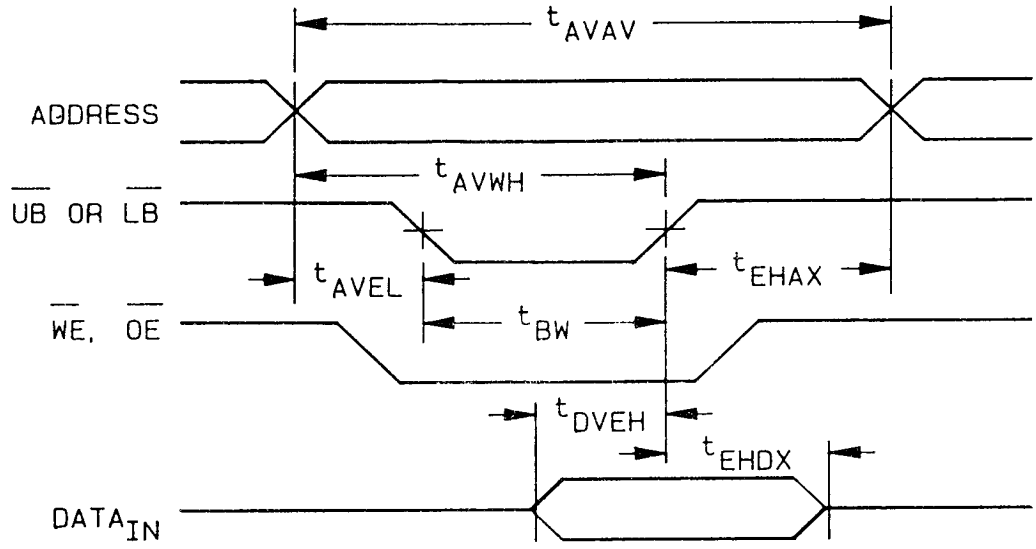
TIMING WAVEFORM OF WRITE CYCLE NUMBER 2 ($\overline{CE}$ CONTROLLED TIMING). (See notes 1, 2, 3, and 5)



See notes on page 18.

FIGURE 4. Timing waveforms - Continued.

TIMING WAVEFORM OF WRITE CYCLE NUMBER 3 ($\overline{UB}$ OR $\overline{LB}$ CONTROLLED TIMING). (See notes 1, 2, 3, and 5)



NOTES:
1. $\overline{WE}$ or $\overline{CE}$ must be high during all address transitions.
2. A write occurs during the overlap (t_{ELWH} or t_{WLWH}) of a low $\overline{CE}$ and a low $\overline{WE}$.
3. t_{WHAX} is measured from the earlier of CE or WE going high to the end of the Write cycle.
4. During this period, I/O pins are in the output state, and input signals must not be applied.
5. If the $\overline{CE}$ low transition occurs simultaneously with or after the $\overline{WE}$ low transition, the outputs remain in high impedance state.
6. During a $\overline{WE}$ controlled write cycle, write pulse low is $\geq t_{DVWH} + t_{WLQZ}$ to allow the I/O drivers to turn off and data to be placed on the bus for the required t_{DVWH}. If OE is high during a WE controlled write cycle, this requirement does not apply and the write pulse can be as short as the specified t_{WLWH}.

FIGURE 4. Timing waveforms - Continued.

Low V_{CC} data retention waveform

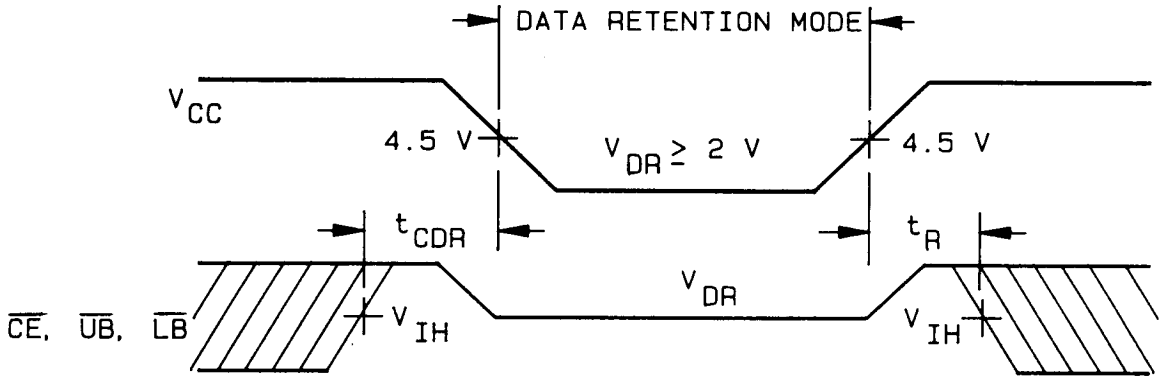


FIGURE 4. Timing waveforms - Continued.

When a qualified source exists, circuit shall be provided and placed on this page.

FIGURE 6. Radiation Hardness bias circuit.

3.10 Microcircuit group assignment for device classes M, B, and S. Device classes M, B, and S devices covered by this drawing shall be in microcircuit group number 41 (see MIL-M-38510, appendix E).

3.11 Serialization for device class S. All device class S devices shall be serialized in accordance with MIL-M-38510.

4. QUALITY ASSURANCE PROVISIONS

4.1 Sampling and inspection. For device class M, sampling and inspection procedures shall be in accordance with section 4 of MIL-M-38510 to the extent specified in MIL-STD-883 (see 3.1 herein). For device classes B and S, sampling and inspection procedures shall be in accordance with MIL-M-38510 and method 5005 of MIL-STD-883, except as modified herein. For device classes Q and V, sampling and inspection procedures shall be in accordance with MIL-I-38535.

4.2 Screening. For device class M, screening shall be in accordance with method 5004 of MIL-STD-883, and shall be conducted on all devices prior to quality conformance inspection. For device classes B and S, screening shall be in accordance with method 5004 of MIL-STD-883, and shall be conducted on all devices prior to qualification and quality conformance inspection. For device classes Q and V, screening shall be in accordance with MIL-I-38535, and shall be conducted on all devices prior to qualification and technology conformance inspection. The following additional criteria shall apply.

4.2.1 Additional criteria for devices M, B, and S.

a. Delete the sequence specified as 3.1.9 - 3.1.13 (preburn-in electrical parameters through interim postburn-in) electrical parameters of method 5004 and substitute lines 1 through 6 of table IIA herein.

b. For device class M the burn-in test circuit shall be submitted to DESC-ECS for review with the certificate of compliance. For device classes B and S the burn-in test circuit shall be submitted to the qualifying activity. For device classes Q and V the burn-in test circuit shall be submitted to DESC-ECS with the certificate of compliance and under the control of the device manufacturer's technical review board (TRB) in accordance with MIL-I-38535.

(1) Static burn-in for device classes S and V (method 1015 of MIL-STD-883, test condition A).

(a) All inputs shall be connected to GND. Outputs may be open or connected to 4.5 V minimum. Resistors R1 are optional on both inputs and outputs, and required on outputs connected to V_{CC}±0.5 V. R1 = 220 ohms to 47 kohms. For static II burn-in, reverse all input connections (i.e. V_{SS} to V_{CC}).

(b) V_{CC} = 4.5 V minimum.

(c) Ambient temperature (T_A) shall be +125°C minimum.

(d) Test duration for the static test shall be 48 hours minimum. The 48 hour burn-in shall be broken into two sequences of 24 hours each (Static I and Static II) followed by interim electrical measurements.

(2) Dynamic burn-in for device classes M, B, S, Q, and V (method 1015 of MIL-STD-883, test condition D) using the circuit submitted (see 4.2b herein).

c. Interim and final electrical parameters shall be as specified in table IIA herein.

d. For classes S and B devices, post dynamic burn-in electrical parameter measurements may, at the manufacturer's option, be performed separately or included in the final electrical parameter requirements.

4.2.2 Additional criteria for device classes Q and V.

a. The burn-in test duration, test condition and test temperature or approved alternatives shall be as specified in the device manufacturer's QM plan in accordance with MIL-I-38535. The burn-in test circuit shall be submitted to DESC-ECS with the certificate of compliance and shall be under the control of the device manufacturer's Technology Review Board (TRB) in accordance with MIL-I-38535.

b. Interim and final electrical test parameters shall be as specified in table IIA herein.

c. Additional screening for device class V beyond the requirements of device class Q shall be as specified in appendix B of MIL-I-38535 and as detailed in table IIB herein.

4.2.3 Percent defective allowable (PDA).

a. The PDA for class S devices shall be 5 percent for static burn-in and 5 percent for dynamic burn-in, based on the exact number of devices submitted to each seperate burn-in.

b. The PDA for class B devices shall be in accordance with MIL-M-38510 for dynamic burn-in.

c. Static burn-in I and II failures shall be cumalative for determining PDA.

d. Those devices whose measured characteristics, after burn-in, exceed the specified delta (Δ) limits or electrical parameter limits specified in table I, subgroup 1, are defective and shall be removed from the lot. The verified failures divided by the total number of devices in the lot initially submitted to burn-in shall be used to determine the percent defective for the lot and the lot shall be accepted or rejected based on the specifed PDA.

e. The PDA for device classes Q and V shall be in accordance with MIL-I-38535 for dynamic burn-in.

4.3 Qualification inspection.

4.3.1 Qualification inspection for device classes B and S. Qualification inspection for device classes B and S shall be in accordance with MIL-M-38510. Inspections to be performed shall be those specified in method 5005 of MIL-STD-883 and herein for groups A, B, C, D, and E inspections (see 4.4.1 through 4.4.5).

4.3.1.1 Qualification extension for device classes B and S. When authorized by the qualifying activity, if a manufacturer qualifies one device type which is identical (i.e., same die), to other device types on this specification, the slsower device types may be part I qualified, upon the request of the manufacturer, without any further testing. The faster device types may be part I qualified by performing only group A qualification testing.

4.3.2 Qualification inspection for device classes Q and V. Qualification inspection for device classes Q and V shall be in accordance with MIL-I-38535. Inspections to be performed shall be those specified in MIL-I-38535 and herein for groups A, B, C, D, and E inspections (see 4.4.1 through 4.4.5).

4.3.3 Electrostatic discharge sensitivity inspection. Electrostatic discharge sensitivity (ESDS) testing shall be performed in accordance with MIL-STD-883, method 3015. ESDS testing shall be measured only for initial qualification and after process or design changes which may affect ESDS classification.

4.4 Conformance inspection. Quality conformance inspection for device class M shall be in accordance with MIL-STD-883 (see 3.1 herein) and as specified herein. Quality conformance inspection for device classes B and S shall be in accordance with MIL-M-38510 and as specified herein. Inspections to be performed for device classes M, B, and S shall be those specified in method 5005 of MIL-STD-883 and herein for groups A, B, C, D, and E inspections (see 4.4.1 through 4.4.5). Technology conformance inspection for classes Q and V shall be in accordance with MIL-I-38535 including groups A, B, C, D, and E inspections and as specified herein.

4.4.1 Group A inspection.

a. Tests shall be as specified in table IIA herein.

b. Subgroups 5 and 6 of table I of method 5005 of MIL-STD-883 shall be omitted.

c. For device class M subgroups 7 and 8 tests shall be sufficient to verify the truth table. For device classes B and S subgroups 7 and 8 tests shall be sufficient to verify the truth table as approved by the qualifying activity. For device classes Q and V subgroups 7 and 8 shall include verifying the functionality of the device, these tests shall have been fault graded in accordance with MIL-STD-883, test method 5012 (see 1.5 herein).

d. O/V (latch-up) tests shall be measured only for initial qualification and after any design or process changes which may affect the performance of the device. Procedures and circuits shall be submitted to DESC-ECS for class M devices. For classes B and S the procedures and circuits shall be submitted to the qualifying activity. For classes Q and V the procedures and circuits shall be submitted to DESC-ECS and will be under the control of the device manufacturer's technical review board (TRB). Testing shall be on all pins, on 5 devices with zero failures. Latch-up test shall be considered destructive. JEDEC standard No. 17 should be used as a guideline for latch-up testing.

e. Subgroup 4 (C_{IN} and C_{OUT} measurements) shall be measured only for initial qualification and after any process or design changes which may affect input or output capacitance. Capacitance shall be measured between the designated terminal and GND at a frequency of 1 MHz. Sample size is fifteen devices with no failures, and all input and output terminals tested.

4.4.2 Group B inspection. The group B inspection end-point electrical parameters shall be as specified in table IIA herein.

a. For device class S steady-state life test circuits shall be conducted using test condition D and the circuit described in 4.2b herein, or equivalent as approved by the qualifying activity.

b. For device class S only, end-point electrical parameters shall be as specified in table IIA herein. Delta limits shall apply only to subgroup 5 of group B inspections and shall consist of tests specified in table IIC herein.

4.4.3 Group C inspection. The group C inspection end-point electrical parameters shall be as specified in table IIA herein. Delta limits shall apply only to subgroup 1 of group C inspection and shall consist of tests specified in table IIC herein.

4.4.3.1 Additional criteria for device classes M, B, and S. Steady-state life test conditions, method 1005 of MIL-STD-883:

a. Test condition D. For device class M the test circuit shall be submitted to DESC-ECS for review with the certificate of compliance. For device classes B and S the test circuit shall be submitted to the qualifying activity. For device classes Q and V the test circuit shall be submitted to DESC-ECS with the certificate of compliance and under the control of the device manufacturer's TRB in accordance with MIL-I-38535.

b. T_A = +125°C, minimum.

c. Test duration: 1,000 hours, except as permitted by method 1005 of MIL-STD-883.

4.4.3.2 Additional criteria for device classes Q and V. The steady-state life test duration, test condition and test temperature or approved alternatives shall be as specified in the device manufacturer's QM plan in accordance with MIL-I-38535. The steady-state life test circuit shall be submitted to DESC-ECS with the certificate of compliance and shall be under the control of the device manufacturer's TRB in accordance with MIL-I-38535. After the completion of all testing, the devices shall be erased and verified prior to delivery.

4.4.4 Group D inspection. For group D inspection end-point electrical parameters shall be as specified in table IIA herein.

4.4.5 Group E inspection. Group E inspection is required only for parts intended to be marked as radiation hardness assured (see 3.6 herein). RHA levels for device classes B, S, Q, and V shall be M, D, R, and H and for device class M shall be M and D. RHA quality conformance inspection sample tests shall be performed at the RHA level specified in the acquisiton document or to a higher qualified level. RHA tests for device classes Q and V shall be performed in accordance with MIL-I-38535 and 1.2.1 herein.

a. RHA tests for device classes B and S for levels M, D, R, and H or for device class M for levels M and D shall be performed through each level to determine at what levels the devices meet the RHA requirements. These RHA tests shall be performed for initial characterization and after design or process changes which may affect the RHA performance of the device.

b. End-point electrical parameters shall be as specified in table IA herein. RHA samples need not be tested at -55°C or +125°C prior to total dose irradiation.

c. Prior to total dose irradiation, each selected sample shall be assembled in its qualified package. The samples shall pass the specified group A electrical parameters for subgroups specified in table II herein.

d. The devices shall be subjected to radiation hardness assurance tests as specified in MIL-M-38510, (device classes M, B, and S) and MIL-I-38535, (device classes Q and V) for the RHA level being tested, and meet the postirradiation end-point electrical parameter limits as defined in table IA at T_A = 25°C ±5°C, after exposure.

e. Prior to and during, total dose irradiation, the devices shall be biased to the worst case conditions established during characterization, (see figure 5) herein.

f. Single Event Phenomena (SEP) testing, shall be performed on all class S and V devices, and shall be optional on all classes M, B, and Q devices. SEP testing shall be performed at initial qualification and after any design or process changes which may affect the upset or latchup characteristics of the device. Test four devices with zero failures. ASTM standard F1192-88 may be used as a guideline when performing SEP testing. The test conditions for SEP are as follows:

(1) The ion beam angle of incidence shall be between normal to the die surface and 60° to the normal, inclusive (i.e. 0° ≤ angle ≤ 60°).

(2) The fluence shall be $\geq 10^7$ ions/cm^2.

(3) The flux shall be between 10^2 and 10^5 ion/cm^2/s. The cross section shall be verified to be flux independent by measuring the cross section at two flux rates which differ by at least an order of magnitude.

(4) The particle range shall be ≥ 20 microns in silicon.

(5) The test temperature shall be +25°C and the maximum rated operating temperature ±10°C.

(6) Bias conditions shall be V_{CC} = 4.5 V dc for the upset measurements and V_{CC} =5.5 V dc for the latchup measurements.

(7) For SEP test limits see table IB herein.

g. For device classes M, B, and S subgroups 1 and 2 of table V method 5005 of MIL-STD-883 shall be tested as appropriate for device construction.

h. When specified in the purchase order or contract, a copy of the following additional data shall be supplied.

(1) RHA delta limits.

(2) RHA upset levels.

(3) Test conditions (SEP).

(4) Number of upsets (SEP).

(5) Number of transients.

(6) Occurence of latchup.

4.5 Delta measurements for device classes B, S, Q, and V. Delta measurements, as specified in table IIA, shall be made and recorded before and after the required burn-in screens and steady-state life tests to determine delta compliance. The electrical parameters to be measured, with associated delta limits are listed in table IIC.

5. PACKAGING

5.1 Packaging requirements. The requirements for packaging shall be in accordance with MIL-M-38510 for device classes M, B, and S and MIL-I-38535 for device classes Q and V.

6. NOTES

(This section contains information of a general or explanatory nature that may be helpful, but is not mandantory.)

6.1 Intended use. Microcircuits conforming to this drawing are intended for use for Government microcircuit applications (original equipment), design applications, and logistics purposes.

6.1.1 Replaceability. Microcircuits covered by this drawing will replace the same generic device covered by a contractor-prepared specification or drawing.

6.1.2 Substitutability. Device classes B and Q devices will replace device class M devices.

6.2 Configuration control of SMD's. All proposed changes to existing SMD's will be coordinated with the users of record for the individual documents. This coordination will be accomplished in accordance with MIL-STD-481 using DD Form 1693, Engineering Change Proposal (Short Form).

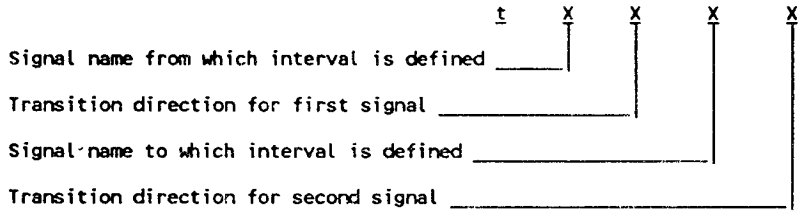
6.3 Record of users. Military and industrial users shall inform Defense Electronics Supply Center when a system application requires configuration control and which SMD's are applicable to that system. DESC will maintain a record of users and this list will be used for coordination and distribution of changes to the drawings. Users of drawings covering microelectronic devices (FSC 5962) should contact DESC-ECS, telephone (513) 296-6022.

6.4 Comments. Comments on this drawing should be directed to DESC-ECS, Dayton, Ohio 45444, or telephone (513) 296-5375.

6.5 Abbreviations, symbols, and definitions. The abbreviations, symbols, and definitions used herein are defined in MIL-M-38510, MIL-STD-1331, and as follows:

C_{IN} C_{OUT}	Input and bidirectional output, terminal-to-GND capacitance.
GND	Ground zero voltage potential.
I_{CC}	Supply current.
I_{IL}	Input current low
I_{IH}	Input current high
T_C	Case temperature.
T_A	Ambient temperature
V_{CC}	Positive supply voltage.
OVV	Latch-up over-voltage

6.5.1 Timing parameter abbreviations. All timing abbreviations use lower case characters with upper case character subscripts. The initial character is always "t" and is followed by four descriptors. These characters specify two signal points arranged in a "from-to" sequence that define a timing interval. The two descriptors for each signal specify the signal name and the signal transition. Thus the format is:



a. Signal definitions:

A = Address
D = Data in
Q = Data out
W = Write enable
E = Chip enable

b. Transition definitions:

H = Transition to high
L = Transition to low
V = Transition to valid
X = Transition to invalid or don't care
Z = Transition to off (high impedance)

6.5.2 Timing limits. The table of timing values shows either a minimum or a maximum limit for each parameter. Input requirements are specified from the external system point of view. Thus, address setup time is shown as a minimum since the system must supply at least that much time (even though most devices do not require it). On the other hand, responses from the memory are specified from the device point of view. Thus, the access time is shown as a maximum since the device never provides data later than that time.

6.5.3 Waveforms.

WAVEFORM SYMBOL	INPUT	OUTPUT
	MUST BE VALID	WILL BE VALID
	CHANGE FROM H TO L	WILL CHANGE FROM H TO L
	CHANGE FROM L TO H	WILL CHANGE FRON L TO H
	DON'T CARE ANY CHANGE PERMITTED	CHANGING STATE UNKOWN
		HIGH IMPEDANCE

6.6 One part - one part number system. The one part - one part number system described below has been developed to allow for transitions between identical generic devices covered by the four major microcircuit requirements documents (MIL-M-38510, MIL-H-38534, MIL-I-38535, and 1.2.1 of MIL-STD-883) without the necessity for the generation of unique PIN's. The four military requirements documents represent different class levels, and previously when a device manufacturer upgraded military product from one class level to another, the benefits of the upgraded product were unavailable to the Original Equipment Manufacturer (OEM), that was contractually locked into the original unique PIN. By establishing a one part number system covering all four documents, the OEM can aquire to the highest class level available for a given generic device to meet system needs without modifying the original contract parts selection criteria.

Military documentation format	Example PIN under new system	Manufacturing source listing	Document listing
New MIL-M-38510 Military Detail Specifications (in the SMD format)	5962-XXXXXZZ(B or S)YY	QPL-38510 (Part 1 or 2)	MIL-BUL-103
New MIL-H-38534 Standardized Military Drawings	5962-XXXXXZZ(H or K)YY	QML-38534	MIL-BUL-103
New MIL-I-38535 Standardized Military Drawings	5962-XXXXXZZ(Q or V)YY	QML-38535	MIL-BUL-103
New 1.2.1 of MIL-STD-883 Standardized Military Drawings	5962-XXXXXZZ(M)YY	MIL-BUL-103	MIL-BUL-103

6.7 Sources of supply.

6.7.1 Sources of supply for device classes B and S. Sources of supply for device classes B and S are listed in QPL-38510.

6.7.2 Sources of supply for device classes Q and V. Sources of supply for device classes Q and V are listed in QML-38535. The vendors listed in QML-38535 have submitted a certificate of compliance (see 3.6 herein) to DESC-ECS and have agreed to this drawing.

6.7.3 Approved sources of supply for device class M. Approved sources of supply for class M are listed in MIL-BUL-103. The vendors listed in MIL-BUL-103 have agreed to this drawing and a certificate of compliance (see 3.6 herein) has been submitted to and accepted by DESC-ECS.

APPENDIX A

FUNCTIONAL ALGORITHMS

10. SCOPE

10.1 Scope. Functional algorithms are test patterns which define the exact sequence of events used to verify proper operation of a random access memory (RAM). Each algorithm serves a specific purpose for the testing of the device. It is understood that all manufacturers do not have the same test equipment; therefore, it becomes the responsibility of each manufacturer to guarantee that the test patterns described herein are followed as closely as possible, or equivalent patterns be used that serve the same purpose. Each manufacturer should demonstrate that this condition will be met. Algorithms shall be applied to the device in a topologically pure fashion. This appendix is a mandatory part of the specification. The information contained herein is intended for compliance.

20. APPLICABLE DOCUMENTS. This section is not applicable to this appendix.

30. ALGORITHMS

30.1 Algorithm A (pattern 1).

30.1.1 Checkerboard, checkerboard-bar.

Step 1. Load memory with a checkerboard data pattern by incrementing from location 0 to maximum.
Step 2. Read memory, verifying the output checkerboard pattern by incrementing from location 0 to maximum.
Step 3. Load memory with a checkerboard-bar pattern by incrementing from location 0 to maximum.
Step 4. Read memory, verifying the output checkerboard-bar pattern by incrementing from location 0 to maximum.

30.2 Algorithm B (pattern 2).

30.2.1 March.

Step 1. Load memory with background data, incrementing from minimum to maximum address locations (All "0's").
Step 2. Read data in location 0.
Step 3. Write complement data to location 0.
Step 4. Read complement data in location 0.
Step 5. Repeat steps 2 through 4 incrementing X-fast sequentially, for each location in the array.
Step 6. Read complement data in maximum address location.
Step 7. Write data to maximum address location.
Step 8. Read data in maximum address location.
Step 9. Repeat steps 6 through 8 decrementing X-fast sequentially for each location in the array.
Step 10. Read data in location 0.
Step 11. Write complement data to location 0.
Step 12. Read complement data in location 0.
Step 13. Repeat steps 10 through 12 decrementing X-fast sequentially for each location in the array.
Step 14. Read complement data in maximum address location.
Step 15. Write data to maximum address location.
Step 16. Read data in maximum address location.
Step 17. Repeat steps 14 through 16 incrementing X-fast sequentially for each location in the array.
Step 18. Read background data from memory, decrementing X-fast from maximum to minimum address locations.

30.3 Algorithm C (pattern 3).

30.3.1 XY March.

Step 1. Load memory with background data, incrementing from minimum to maximum address locations (All "0's").
Step 2. Read data in location 0.
Step 3. Write complement data to location 0.
Step 4. Read complement data in location 0.
Step 5. Repeat steps 2 through 4 incrementing Y-fast sequentially, for each location in the array.
Step 6. Read complement data in maximum address location.
Step 7. Write data to maximum address location.
Step 8. Read data in maximum address location.
Step 9. Repeat steps 6 through 8 decrementing X-fast sequentially for each location in the array.
Step 10. Read data in location 0.
Step 11. Write complement data to location 0.
Step 12. Read complement data in location 0.
Step 13. Repeat steps 10 through 12 decrementing Y-fast sequentially for each location in the array.
Step 14. Read complement data in maximum address location.
Step 15. Write data to maximum address location.
Step 16. Read data in maximum address location.
Step 17. Repeat steps 14 through 16 incrementing X-fast sequentially for each location in the array.
Step 18. Read background data from memory, decrementing Y-fast from maximum to minimum address locations.

30.4 Algorithm D (pattern 4).

30.4.1 CEDES - CE deselect checkerboard, checkerboard-bar.

Step 1. Load memory with a checkerboard data pattern by incrementing from location 0 to maximum.
Step 2. Deselect device, attempt to load memory with checkerboard-bar data pattern by incrementing from location 0 to maximum.
Step 3. Read memory, verifying the output checkerboard pattern by incrementing from location 0 to maximum.
Step 4. Load memory with a checkerboard-bar pattern by incrementing from location 0 to maximum.
Step 5. Deselect device, attempt to load memory with checkerboard data pattern by incrementing from location 0 to maximum.
Step 6. Read memory, verifying the output checkerboard-bar pattern by incrementing from location 0 to maximum.